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Analysis and Reduction of Conducted EMI in Power Electronic Modules

Ph. D. Thesis

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Contents

Introduction

The phenomena causing the production and spreading of unwanted electromagnetic emissions arising from electrical or electronic devices, apparatuses and systems have been widely investigated over the last decades and reported in the relevant scientific literature. As a consequence of this, nowadays, the electromagnetic compatibility techniques, which limit the undesirable effects of these emissions, are very popular and of ever-increasing importance both in environmental and industrial contexts.

The present thesis focuses on conducted electromagnetic emissions generated by power electronic modules making use of active devices operating with high switching frequency, which today are commonly utilized in a lot of sectors: aerospace, commercial, industrial, residential, telecommunication, transportation, utility systems. The onerous operating conditions of such modules, caused by high values of voltages and electric currents and very short switching times of active devices, make essential, in order to reach an efficient and economic use of materials and components, as well as a reliable and durable use of devices themselves, to carry out an accurate preliminary analysis of the mechanisms resulting in unwanted electromagnetic couplings between the various module components. Indeed, due to the unavoidable presence of parasitic inductances and capacitances and of extremely steep waveforms, electrical signals frequently originate inside the modules with high peak values and exasperated temporal dynamics, which strongly restrict the field of application of the modules themselves. For the sake of concreteness, the analysis of above described phenomena has been worked out on a power electronic module prototype made kindly available by STMicroelectronics, one of the world-leading companies in such field. After a first phase during of which have been

individuated and computed the values of the most critical parasitic elements, by means of a theoretical investigation supported by suitable software tools, attention has been paid to how to reduce such values and improve the overall performance of the module. In this connection, some useful techniques to reduce significantly the undesirable emissions have been individuate and successfully applied to the prototype, so obtaining an optimized module from the electromagnetic emission point of view.

The present thesis is structured as follows. Chapter 1 provides an introduction to main kinds of power modules used in many areas of electrical and electronic engineering and shows also the most critical features of their operations. Chapter 2 highlights the basic aspects of electromagnetic emissions focusing on the conducted ones. Chapter 3 illustrates the structure and materials of power electronic modules. In the Chapter 4 the fundamental equations of electromagnetism are briefly reviewed and the most powerful numerical methods used to solve them are described; moreover, the simulation tools Q3D Extractor and PSpice utilized in the thesis are synthetically illustrated. Chapter 5 describes in detail the analyses carried out of STMicroelectronics prototype and the original techniques and results which have been obtained. Finally, some concluding remarks complete the work.

Chapter 1

Power electronic systems

1.1 Power electronic

Power Electronic is one of the most important branch of electronics and electrical engineering and its aim is to process and control the flow of electrical energy by supplying voltages and currents suitable for user loads [1].

Fig. 1.1 shows the basic structure of Power Electronic System [2]. In input is given a form of electric energy and the task of the system is to convert it in another form. For example, if the load is a DC motor, then it needs a DC voltage and current, and the power controller converts the AC input into a DC values which are suitable for the motor. Inside a black box could be a controller or converter, which make use of actives devices such as thyristor, GTO, MOSFET, BJT or IGBT.

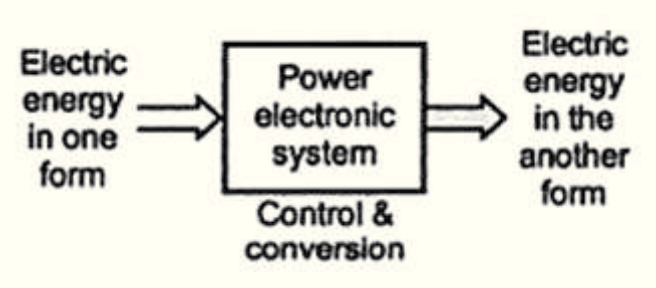


Fig. 1.1 Basic input/output of power electronic systems.

1.2 Applications of power electronics system

There are many applications coming up every day in power electronics. Some of them are mentioned below [3], [5]:

1. *Switch mode power supplies and UPS (Uninterruptible Power Supply)*: advances in microelectronic technology have led to the development of computers, apparatus, communications and consumer electronics devices that require regulated dc power supplies and often continuous supply;
2. *Energy Conservation*: the rising costs of energy and interest in environmental protection led to give priority to energy saving. One of the applications of power electronics regards the fluorescent lamps that operate at high frequency (20 kHz) to obtain a high yield. The power electronics is also found in the motors driving pumps and compressors;
3. *Transportation*: the electric-drive vehicles require battery chargers that use the power electronics;
4. *Electro technical applications*: equipment for welding, electroplating or induction heating;
5. *Utility related applications*: one of these applications is in transmission of electric power with high-voltage dc lines (HVDC: High Voltage Direct Current).

Table 1.1 shows some important applications of power electronics systems. The power ratings range from a few W in the case of lamps to several 100 MW in HVDC transmission systems.

Table 1.1 Some application of power electronic

N.	Area	Application
1	Aerospace	Space shuttle power supplies, Satellite power supplies, Aircraft power system;
2	Commercial	Heating, air-conditioning power supplies, computer, office equipment, elevators, light dimmer, central refrigeration;
3	Industrial	Arc and industrial furnaces, blowers and fans, pumps and compressors, industrial lasers, transformer tap charges, rolling mills, factory automation;
4	Residential	Air conditioning, cooking, lighting, refrigerators, electric-door openers, dryers, fans, personal computers, vacuum cleaners, washing machine, food mixers;
5	Telecommunication	Battery charges, power supplies;
6	Transportation	Battery charges, traction control of electric vehicles, electric locomotives, street cars, trolley buses, subways, automotive electronics;
7	Utility Systems	High voltage DC transmission, excitation systems, VAR compensation, static circuit breakers, fans and boiler feed pumps, Grid interface for alternative energy resources (solar, wind, fuel cells, etc.) and energy storage.

1.3 Power converters

One of the most important typology power system are the electronic converters, by means of which it is possible to control and transform the electric power. The power electronic converters are generally classified into five categories depending on the input, output and job they perform:

1. AC to DC Converters;
2. DC to AC Converters;
3. DC to DC Converters;
4. AC to AC Converters;
5. AC Regulators.

Power converters have many advantages, such as: high efficiency of conversion due to low losses in power semiconductor device, long life, compact size and light weight, fast dynamic response, lower installation costs and high reliability of power electronic components and converter systems.

Power Converters introduce harmonics into supply and load systems, adversely affecting the performance of the load and supply. These harmonics distort the voltage waveform and cause interference with communication lines. To devoid these, it is necessary to insert a filter at the input of a converter [2],[4]. Although these disadvantages power electronic converters are used in large number of applications.

1.4 Power electronic devices

One of the main contributions that led to the growth of the power electronics field has been the unprecedented advancement in semiconductor technology, especially with respect to switching speed and power handling capabilities. The area of power electronics started by the introduction of the silicon controlled rectifier (SCR) in 1958. Since then, the field has grown in parallel with the growth of the power semiconductor device technology. In fact, the history of power electronics is very much connected to the development of switching devices and it emerged as a separate discipline when high-power and MOSFET devices were introduced in the 1960s and 1970s. The introduction of new devices has been ever accompanied by dramatic improvement in power rating and switching performance. Because of their functional importance, drive complexity, fragility, and cost, the power electronic design must be equipped with a thorough understanding of the device operation, limitation, drawbacks, and related reliability and efficiency issues. In the 1980s, the development of power semiconductor devices took an important turn when a new process technology was developed that allowed integration of MOS and bipolar junction transistor (BJT) technologies on the same chip. Thus far, two devices using this new technology have been introduced: insulated bipolar transistor (IGBT) and MOS controlled thyristor (MCT). Even though, most of today's available semiconductor power devices are made of silicon or germanium materials, other materials such as gallium arsenide, diamond and silicon carbide are currently being tested. In fact, there are several technologies emerging that are destined to replace the silicon power MOSFET as the power semiconductor transistor of choice. Currently, the most promising technologies are GaN (gallium nitride) and SiC (silicon carbide). Both

technologies are wide band gap materials that offer the advantages of higher power densities, higher voltages, lower leakage current and the ability to operate at higher temperatures [27]. Power semiconductor devices represent the ‘‘heart’’ of modern power electronics, with two major desirable characteristics of power semiconductor devices guiding their development:

1. switching speed (turn-on and turn-off times);
2. power handling capabilities (voltage blocking and current carrying capabilities).

Improvements in both semiconductor processing technology and manufacturing and packaging techniques have allowed power semiconductor development for high-voltage and high current ratings and fast turn-on and turn-off characteristics. The availability of different devices with different switching speeds, power handling capabilities, size and cost, makes it possible to cover many power electronics applications.

Power semiconductor devices can be classified into various categories according to their degree of controllability (Turn ON and Turn OFF Capability), type of gate signal required, Current Conduction Capability and Voltage withstanding ability [2], [4], [5].

1. Based on Turn ON and Turn OFF capability:

- *Group I*: uncontrollable power semiconductor devices such as *diodes*. These are called uncontrolled devices because their ON and OFF states are not dependent on the control signals but on supply and load circuit conditions;

- *Group II*: partially controllable power semiconductor devices. These include devices that are trigged into conduction by control signals but are turned off by the load circuit or by the supply. Such devices include thyristors such as line commutated SCR, force commutated SCR, light active SCR, TRIAC, DIAC;
- *Group III*: Fully controllable power semiconductor devices. They can be turned on and off by control signals. This group includes: BJTs, MOSFETs, IGBTs; GTOs.

2. Based on Gate signal:

- *Group I*: Pulse gate requirement. To Turn on these devices, pulse voltage is applied as a control signal. Once the device is turned on, the gate pulse is not required and thus removed. This group includes: SCR, GTO, SITH, MCT;
- *Group II:* Continuous gate requirement. For these devices, continuous gate signal is required to maintain them in ON state. This group includes: BJT, MOSFET, IGBT.

3. Based on Current Conduction Capability:

- *Group I:* Unidirectional Current Devices. This group includes: SCR, GTO, BJT, MOSFET, IGBT;
- *Group II:* Bidirectional Current Devices. This group includes: TRIAC, RCT (Reverse Conducting Thyristor).

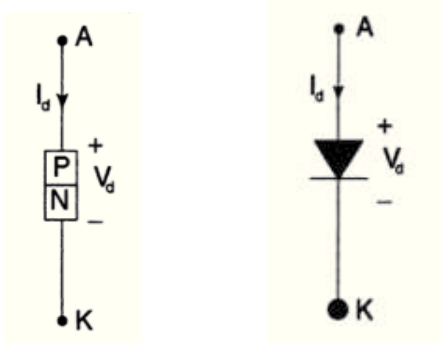
4. Based on Voltage withstanding ability:

- *Group I*: Unipolar voltage withstanding devices. This group includes: BJT, MOSFET, IGBT;

- *Group II:* Bipolar voltage withstanding devices. This group includes: SCR, GTO.

1.4.1 The power diode

Power diodes play a significant role in the operation of power electronic circuits. A power diode behaves as a switch with uncontrolled turn on and turn off characteristics. There are mainly used as uncontrolled rectifiers to convert single-phase or three-phase AC voltage to DC. Diode can be constructed with germanium and silicon, but a silicon material is better because silicon diodes can work at higher current and junction temperatures than germanium diodes [6]. Fig. 1.2 (a) and (b) shows the structure of a diode and the circuit symbol of power diode respectively.



(a) (b)

Fig. 1.2 (a) p-n junction, (b) circuit symbol of power diode

The terminal voltage and current are represented as V_d and I_d respectively. It has two terminals: an anode (A) and a cathode (K).

When anode (A) is positive with respect to cathode (K), the pn-junction becomes forward- biased and the diode starts to conductive. The diode does not conduct when the voltage between anode to cathode is negative, in this case, the diode is reverse biased.

Fig. 1.2 (b) shows the conventional direction of current flow (from anode to cathode) when diode conducts.

The structure of the power diode is little different from the small signal diodes [2].

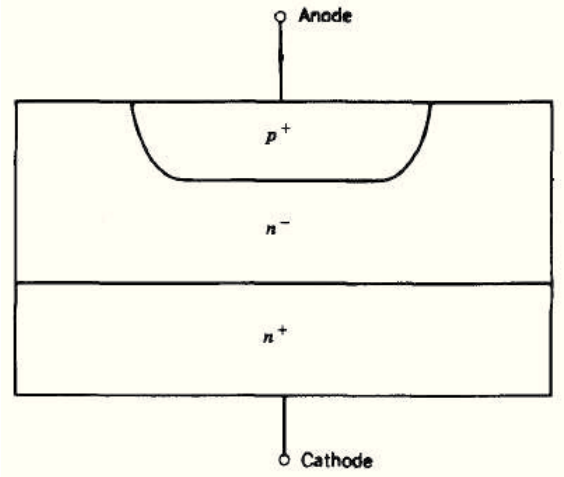


Fig. 1.3 Structure of power diode

As shown in Fig. 1.3, there is heavily doped n+ substrate with doping level of $10^{19}/cm^3$. This substrate forms a cathode of the power diode. On n+ substrate, lightly doped n- epitaxial layer is grown, this layer is also known as drift region. The PN junction is formed by diffusing a heavily doped p+ region, which is the anode of the diode. The thickness of n-drift region determines the breakdown voltage of the diode. Its function is to absorb the depletion layer of the reverse biased p+n- junction. As it is lightly doped, it will add significant ohmic resistance to the diode when it is forward biased. For higher breakdown voltages, the drift region is wide. The n-drift region is absent in low power signal diodes.

When the power diode is forward biased (anode is made positive with respect to cathode), the holes will be injected from the p+ region into the drift region. Some of the holes combine with the electrons in the drift region. Since injected holes are many, they

attract electrons from the n+ layer. Thus holes and electrons are injected in the drift region simultaneously and the resistance of the drift region reduces significantly. Thus diode current goes on increasing, but drift region resistance remains constant. So on-state losses in the diode are reduced. This phenomenon is called Conductivity Modulation of drift region.

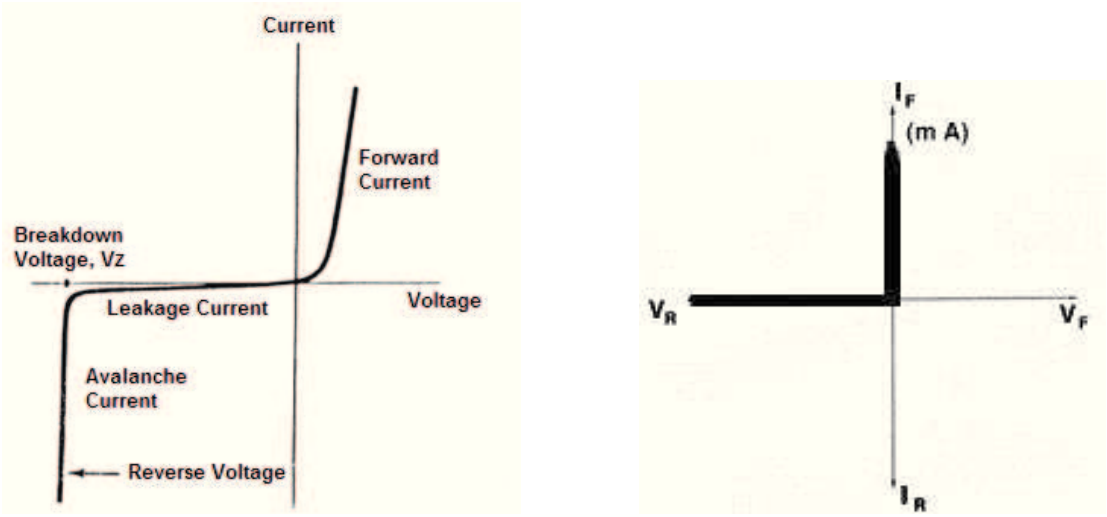


Fig. 1.4 Diode: a) i-v characteristics, b) idealized characteristics

The I-V characteristics of power diode are shown in Fig. 1.4 (a). When the diode is in the forward biased condition (1st quadrant of the voltage versus current plot), it begins to conduct with only a small forward voltage across it (≈ 1 V). In reverse biased, (3th quadrant) only a negligibly small leakage current flows through the device until the reverse break-down voltage is reached [5]. Fig. 1.4 (b) shows the I-V characteristics idealized. At turn-ON, the diode can be considered an ideal switch because it turns on rapidly compared to the transients in the power circuit. At turn-OFF the diode current reverses for a reverse-recovery time t_{rr}, as indicated in Fig. 1.4.

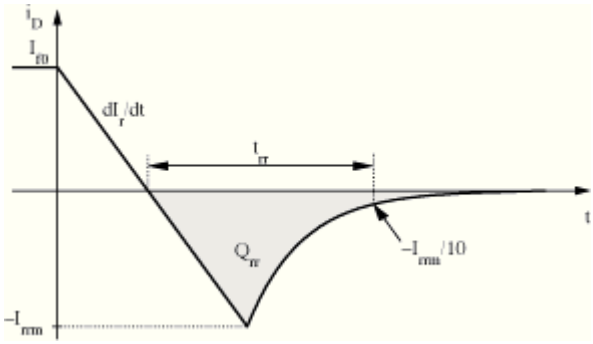


Fig. 1.5 Diode turn-off

Depending on the application requirements, there are various types of diodes:

- *Schottky diode*: this class of diode uses metal-to-semiconductor junction to produce the rectifying effect [7]. They are characterized by very fast reverse recovery time and low forward voltage drop (≈ 0,3 V). Schottky diodes are highly suitable for use in high-frequency applications [7];
- *Fast-recovery diodes*: for these diode is need a small reverse-recovery time. This group of diodes is used in combination with controllable switches [5].
- *Line-frequency diodes*: this group of diodes has an high value of t_{rr}. These diodes are available with blocking voltage ratings of several kV and current ratings of several kA. These diodes can be connected in series and parallel to satisfy any voltage and current requirement.

1.4.2 Control switch devices

As it is mentioned before the control switch can be turned on and off by control signals applied to the control terminal of the device. This kind of devices includes: BJTs, MOSFETs, GTOs and IGBTs.

1.**4.2.1 BJT**

Bipolar Junction Power Transistors are applied to a variety of power electronic functions such as switching mode power supplies, dc motor inverters and PWM inverters but is mostly used in amplifiers [8]. The power BJT (Bipolar Junction Transistor) is a three terminal device and it comes in two different types: the *npn BJT* and the *pnp BJT*. The three terminals are emitter (E), collector (C) and base (B). The structure and the circuit symbol of the BJT are shown in Fig. 1.6.

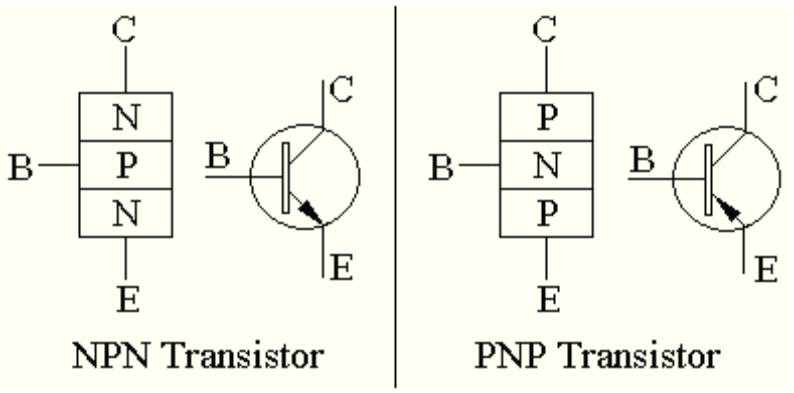


Fig. 1.6 Structures and symbol of *npn BJT* and *pnp BJT*.

The BJT is fabricated with three separately doped regions and has two junctions (boundaries between the n and the p regions) which are similar to the junctions we saw in

the diodes and thus they may be forward biased or reverse biased. Since each junction has two possible states of operation (forward or reverse bias) the BJT with its two junctions has four possible states of operation.

The structure, as shown on Fig. 1.6, is not symmetric; the n and p regions are different both geometrically and in terms of the doping concentration of the regions. For example, the doping concentrations in the collector, base and emitter may be 10^{15}, 10^{17}, and 10^{19} respectively. Therefore the behavior of the device is not electrically symmetric and the two ends cannot be interchanged.

Fig. 1.7 shows the qualitative characteristic curves of a BJT. The collector current I_C is plotted with respect to collector base voltage (V_{CB}) for different values of base current (I_E). Each curve starts at I_C=0 and rises rapidly for a small positive increase in V_{CB}.

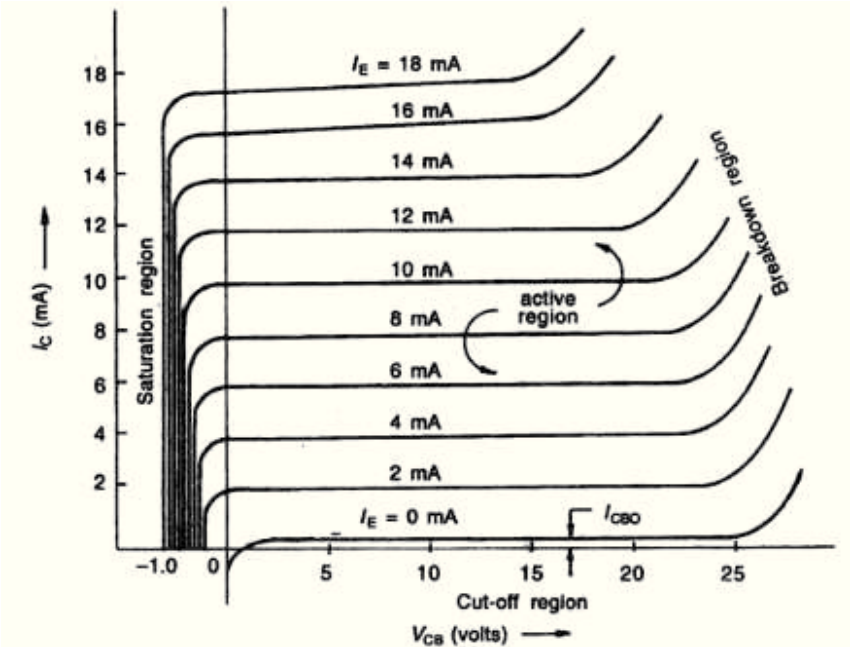


Fig. 1.7 BJT characteristic curves.

The plot indicates the four regions of operation: the saturation, the cutoff, the active and the breakdown.

1. *Cutt-off region*: is the area where base current is almost zero. Hence no current flows and transistors is OFF;
2. *Saturation region*: The portion of the characteristics where V_{CB} is negative; here a BJT is said to be satured when both the C-B and E-B junctions are forward-biased.
3. *Active region*: is defined where flat, horizontal portions of voltage-current curves show ‘‘constant’’ I_C current, because the collector current does not change significantly with V_{CB} for a given I_E. Those portions are used only for small signal transistors operating as linear amplifiers [9];
4. *Breakdown region*: is defined when V_{CB} voltage exceeds certain limits, becoming practically vertical. It is good to avoid getting into this region because the transistor may be damaged or over-current or over-dissipation.

Power BJTs have good on-state characteristics but long switching times especially at turn-off. They are current controlled devices with small current gain because of high level injection effects and wide base width required to prevent reach-through breakdown for high blocking voltage capability. Therefore, they require complex base-drive circuits to provide the base current during on-state, which increases the power loss in the control electrode [9].

1.4.2.2 MOSFET

The power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) belongs to the unipolar device family because it uses only majority carriers in conduction [9]. The device symbol for a p- and n-channel enhancement and depletion types are shown in Fig. 1.8.

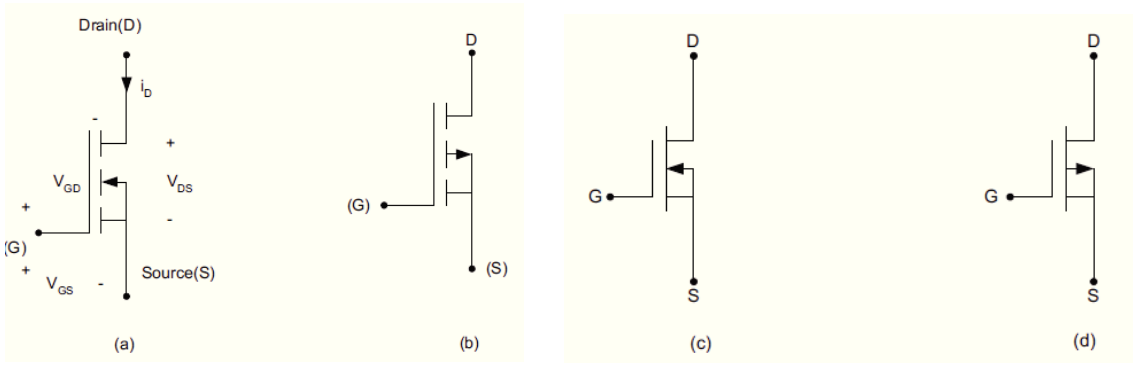


Fig. 1.8 Device symbols: (a) n-channel enhancement-mode; (b) p-channel enhancement-mode; (c) n-channel depletion-mode; and (d) p-channel depletion-mode.

Most MOSFET devices used in power electronics applications are of the n-channel, enhancement type, like that shown in Fig. 1.8 a.

The MOSFET has three terminals: G (gate), D (drain) and S (source). It is a voltage-controlled device [5], in fact to carry drain current, a channel between the drain and the source must be created. This occurs when the gate-to-source voltage (V_{GS}) exceeds the device threshold voltage V_{Th} [9]. When the device is turns on and the current flows from drain to source.

Power MOSFETs use vertical channel structure in order to increase the device power rating [10]. Figure 1.9 shows a structure of n-channel enchancemode MOSFET.

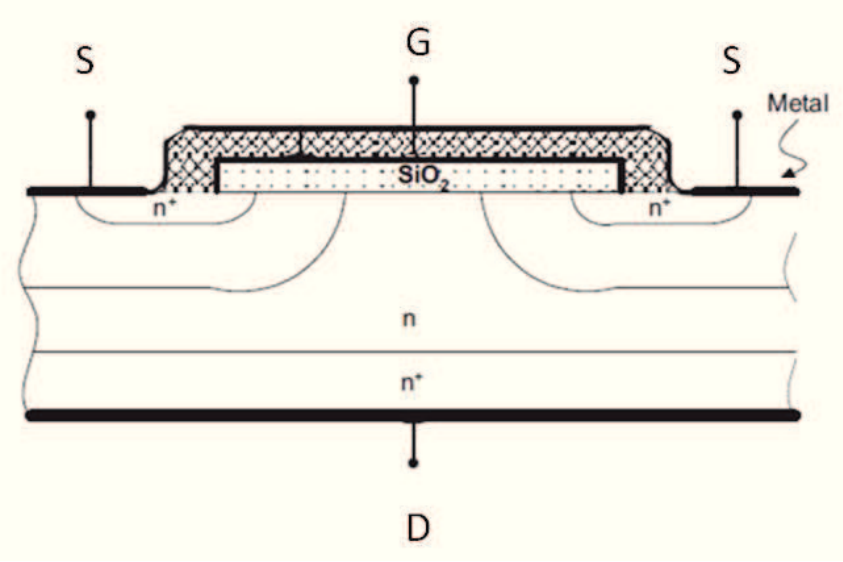


Fig. 1.9: Structure of n-channel enchance mode MOSFET.

Most power MOSFETs feature a vertical structure with Source and Drain on opposite sides of the wafer in order to support higher current and voltage. The p-n junction between the p-base and the n-drift region provide the forward voltage blocking capabilities. The source metal contact is connected directly to the p-base region through a break in the n-source region in order to allow for a fixed potential to the p-base region during normal device operation. When the gate and source terminal are set to the same potential (V_{GS}=0), no channel is established in the p-base region that is, the channel region remains unmodulated. The lower doping in the n-drift region is needed in order to achieve higher drain voltage blocking capabilities.

Fig. 1.10 shows the V-I characteristics of n-channel power MOSFET. The drain current i_D is plotted with respect to drain source voltage V_{DS}. These characteristics are plotted for various values of gate source voltage (V_{GS}).

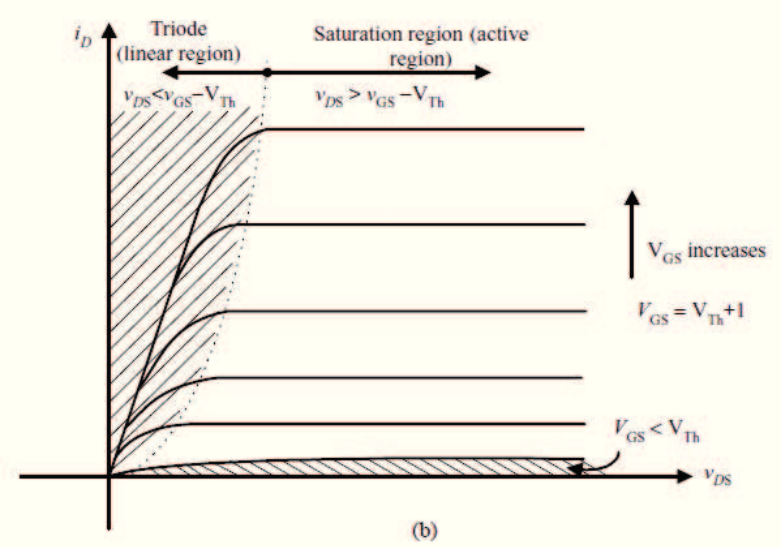


Fig. 1.10 n-channel enhancement-mode MOSFET characteristic curve.

In Fig. 1.10 we can see three regions: Triode (linear region), saturation region (active region) and cut-off region. For $V_{GS} > V_{Th}$, the device can be either in the triode region or in the saturation region, depending on the value of V_{DS}. For given V_{GS}, with small V_{DS} ($V_{DS} < V_{GS} - V_{Th}$), the device operates in the triode region and for larger V_{DS} ($V_{DS} > V_{GS} - VTh$), the device enters in the saturation region. For $V_{GS} < V_{Th}$, the device turns off, with drain current almost equal to zero. Under both regions of operation, the gate current is almost zero. This is why the MOSFET is known as a voltage-driven device and, therefore, requires simple gate control circuit. In the power electronic applications MOSFET is never operated in the active region because it acts as amplifier. For switching applications, MOSFET is operated only in triode and cut-off regions.

Because the MOSFET is a majority carrier transport device, it is inherently capable of high frequency operation [5],[9], [12]. However, the MOSFET has two limitations:

1. high input gate capacitances;

2. transient/delay due to carrier transport through the drift region.

1.4.2.3 GTO

The GTO (Gate Turn - Off Thyristor) is an alternative to SCR (Silicon Controlled Rectifier) better known as a Thyristor. A SCR device has been used in large power application because of high current density and low forward voltage drop. This device has two inconvenient: they are not able to turn off through a gate and the low switching speed. For this reason the GTOs was proposed as an alternative to SCR [9].

The GTO belongs to a thyristor family with a four-layer structure. Thyristors (SCR – Silicon Controlled Rectifier) are multijunction semiconductor devices with latching behavior. Thyristors in general can be switched with short pulses, and then maintain their state until current is removed. They act only as switches. The characteristics are especially well-suited to controllable rectifiers, although thyristors have been applied to all power conversion applications [9]. A GTO device has three-terminal, anode (A), cathode (C) and gate (G) and four layers, pnpn, as like conventional thyristors. GTOs have many applications, including motor drives, induction heating, distribution lines, pulsed power, and flexible ac transmission systems [9], [13]. The GTO behaves like thyristor except for turn-off. The GTO is a power switching device that can be turned on by a short pulse of gate current (short-duration gate current pulse) and unlike the thyristor, GTOs turned off by a reverse gate pulse (negative gate-cathode voltage). Once in the on state, the device may stay on without any further gate current. Hence there is no need for an external communication circuit to turn it off. Because turn-off is provided by bypassing carriers directly to the gate circuit, its turn-off time is short, thus giving it more

capability for high-frequency operation than thyristors. The GTO symbol and static characteristics (similar to that of SCR) are shown in Fig. 1.11.

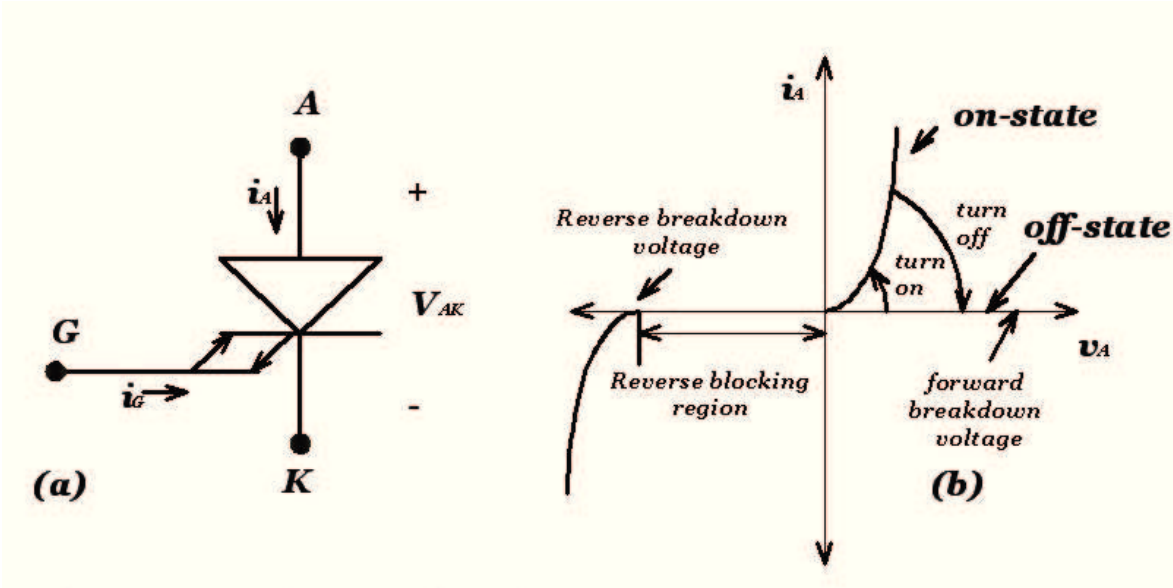


Fig. 1.11 GTO circuit symbol (a) I-V characteristics.

The structure is shown in Fig. 1.12

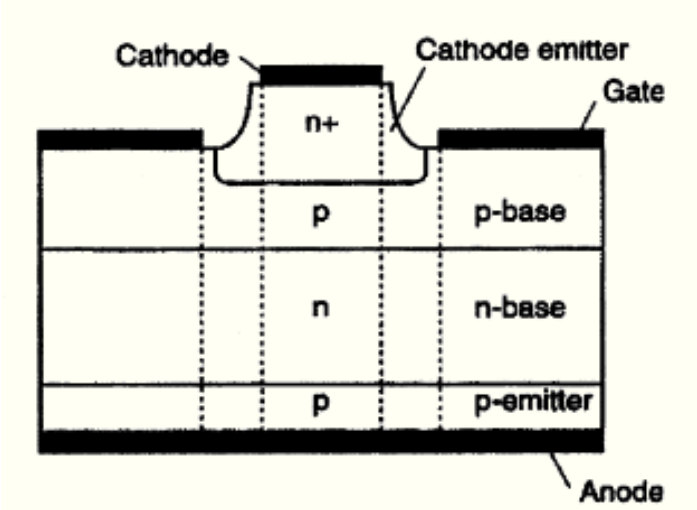


Fig. 1.12 structure of GTO.

The basic structure of a GTO, a four-layer p-n-p-n semiconductor device, is very similar in construction to a thyristor. It has several design features that allow it to be turned on and off by reversing the polarity of the gate signal. The most important differences are that the GTO has long narrow emitter fingers surrounded by gate electrodes and no cathode shorts.

The advantages of this device are: higher voltage blocking capability, gate has full control over the operation of GTO, low on state loss, high ratio of peak surge current to average current and high on state gain. The GTOs have some limitations too: they require large negative gate currents for turn off, for this reason they are suitable for low power applications, very small reverse voltage blocking capability and a very small switching frequencies [2].

1.4.2.4 MCT

The power MCT (MOS Controlled Thyristor) is a new type of device that combines the capabilities of thyristor voltage and current with MOS gated turn on and off [14]. In fact uses a pair of MOSFETs to turn on and turn off current. In this way MCTs overcomes some limitations of the existing power device, such as high input low current density and high forward drop of power MOSFETs, both of which do not make it suitable in low voltage and low power applications [9]. A MCT has a thyristor type structure with three junctions and *pnpn* layers between the anode and cathode.

Its circuit symbol and I-V characteristic is shown respectively in Fig. 1.13 and Fig. 1.14.

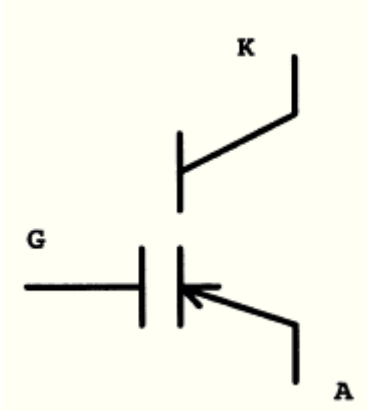


Fig. 1.13 MCT circuit symbol.

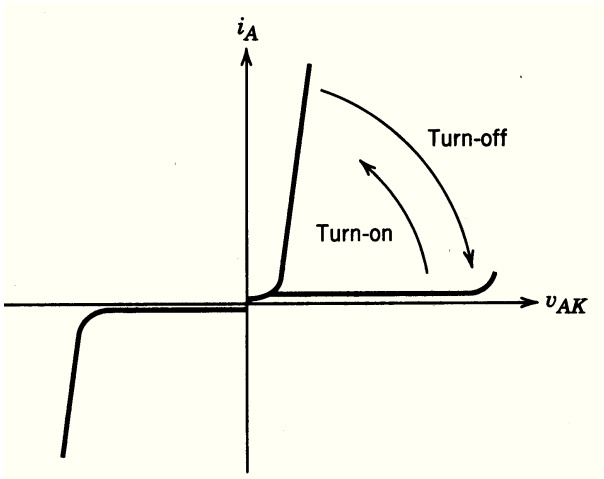


Fig. 1.14 MCT I-V characteristic.

From the I-V characteristic, shown in Fig. 1.14, it is possible to see that the MCT has many of the property of a GTO, including a low voltage drop in the on state at relatively high currents and a latching characteristic. This device has two significant advantages over the GTO:

1. Not require a large negative gate current for turn off;

2. Turn on and off times are about a few μs [5].

1.4.2.5 IGBT

The IGBT (Insulated Gate Bipolar Transistor) was introduced in the early 1980s becoming a successful device because of its superior characteristics. It is a three-terminal power semiconductor device that combines the simple gate-drive characteristics of the MOSFETs with the high-current and low-saturation-voltage capability of BJT [15]. The three terminals are: gate (G), collector (C) and emitter (E). Fig. 1.15 shows the symbol of IGBT.

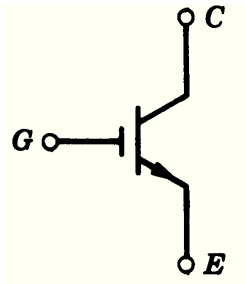


Fig. 1.15 IGBT circuit symbol.

The current flows from collector to emitter whenever a voltage between gate and emitter is applied. In this case the IGBT is in ON state. The IGBT is in OFF state when gate emitter voltage is removed. Thus gate has full control over the conduction of IGBT. The Fig. 1.16 shows the vertical cross-section of this devise. The structure of IGBT is similar to that of MOSFET except that n^+ layer at the drain in a power MOSFET is replaced by p^+ substrate called collector.

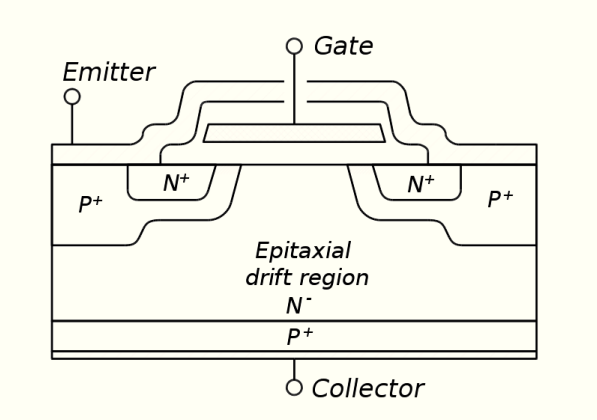


Fig. 1.16 Structure of IGBT.

IGBT is a voltage controlled device. It has high input impedance like a MOSFET and low on-state conduction losses like a BJT. When collector and gate voltage is positive with respect to emitter the device is in forward blocking mode. When gate to emitter voltage becomes greater than the threshold voltage of IGBT, a n-channel is formed in the P-region. Now device is in forward conducting state. In this state *p*+ substrate injects holes into the epitaxial *n*− layer. Increase in collector to emitter voltage will result in increase of injected hole concentration and finally a forward current is established.

Fig. 1.17 shows the V-I characteristics of n-channel IGBT. The collector is also called Drain and emitter Source. The drain current i_D is plotted with respect to drain source voltage V_{DS}. These characteristics are plotted for various values of gate source voltage (V_{GS}). When the gate to source voltage is greater than the threshold voltage $V_{GS(th)}$ the device is in ON state; when V_{GS} is less than $V_{GS(th)}$ the IGBT is turns off. The BV_{DSS} is the breakdown drain to source voltage when gate is open circuited.

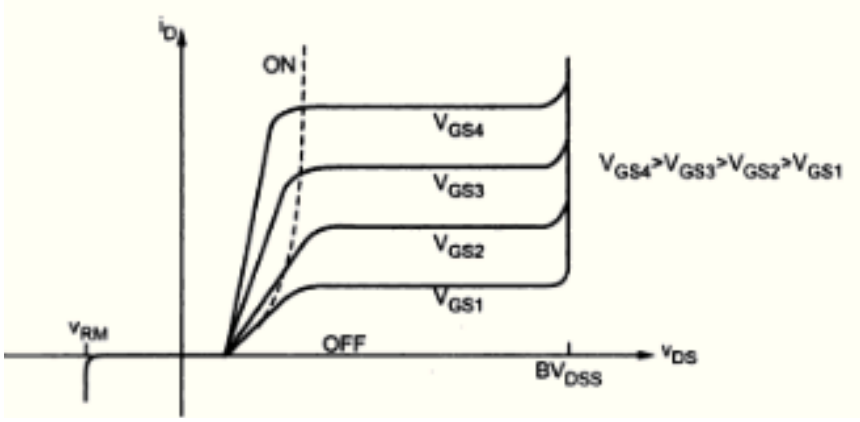


Fig. 1.17 V-I characteristics of IGBT.

IGBTs are faster than BJT's, but still not quite as fast as MOSFET's. the IGBT's offer for superior drive and output characteristics when compared to BJT's. IGBT's are suitable for high voltage, high current and frequencies up to 20kHz. IGBT's are available up to 1400V, 600A and 1200V, 1000A. IGBTs are used in medium power applications such as ac and dc motor drives, medium power supplies, solid state relays and contractors, general purpose inverters, UPS, welder equipments, servo controls, robotics, cutting tools, induction heating.

1.4.2.6 Comparison of controllable switches

The efficiency, capacity, and ease of control of power converters depend mainly on the power devices employed. The progress in semiconductor technology will undoubtedly lead to higher power ratings, faster switching speeds and lower costs. A summary of power device capabilities is shown in Table 1.2 [5].

Table 1.2 Relative properties of controllable switches

Device	Power Capability	Switching Speed
BJT	Medium	Medium
MOSFET	Low	Fast
GTO	High	Slow
IGBT	Medium	Medium
MCT	Medium	Medium

The Fig. 1.18 represents a summary of power device capabilities. All device, except the MCT, have a relatively mature technology. MCTs technology is in a state of rapid expansion, and significant improvements in the device capabilities are possible, as indicated by the expansion arrow in the Fig.1.18.

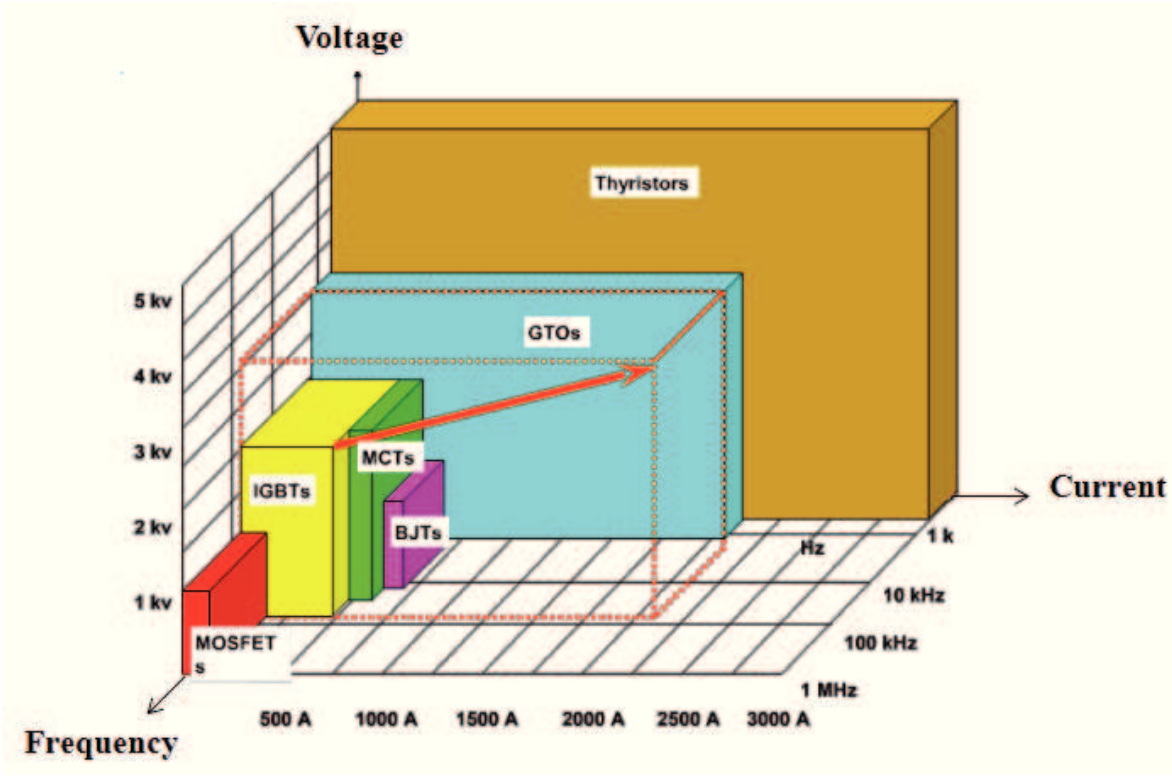


Fig. 1.18 Summary power device capabilities.

Chapter 2

Electromagnetic interference

2.1 Introduction to electromagnetic compatibility

A system is *Electromagnetic Compatible* (EMC) with its environment when it is able to function compatibly with other electronic systems and not produce or be susceptible to interference. Precisely a system is electromagnetically compatible with its environment if it satisfies the following three criteria:

1. It does not cause interference with other systems;
2. It is not susceptible to emissions from other systems;
3. It does not cause interference with itself.

Constructors of devices must respect not only the desired functional performance, but also legal requirements in force in all countries of the world before to sale the product. In essence, Electromagnetic Compatibility (EMC) deals with interferences and the prevention of it through the design of electronic systems. The emissions should not be considered all undesirable phenomena, because nowadays there are many devices are specifically designed to emit EM radiation (for example: radio transmitters / television, phones mobile). The emissions due to the geometry and structure of the device must be limited as much as possible because they represent the leading cause of malfunction.

The EMC problem can be divided into two major sub-problems: Emission (EMI) and susceptibility (EMS).

1. *Emission* pertain to the interference-causing potential of a product. The purpose of controlling emissions is to limit the electromagnetic energy emitted and thereby to control the electromagnetic environment in which other products must operate;

2. *Susceptibility* is the capability of a device or circuit to respond to unwanted electromagnetic energy (i.e. noise). The opposite of it is immunity that gives a measure of the ability of an apparatus to receive unwanted signals (and therefore be disturbed) [17].

Eelectromagnetic Compatibility is related to the generation, transmission and reception of electromagnetic energy [16]. These three aspects form the basic structure of each project to electromagnetic compatibility which is illustrated in Fig. 2.1.

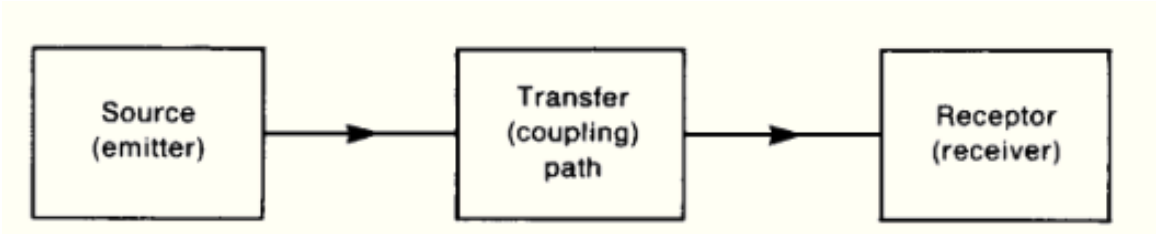


Fig. 2.1 The basic decomposition of the EMC coupling problem.

In the figure is shown a source (or emitter) that produces a specific signal, transmitted to a receiver by means of a transfer device or by means of a coupling path. This process creates a desired or a malfunction behavior. In the first case, the received signal is defined as the useful signal, in the second case, the signal is instead a noise, creating an

interference. In general, there is an interference when the energy received causes an unwanted behavior of the receiver. However, not always the unintentional transfer of energy causes interference: the latter only occurs if the received energy is sufficiently high and / or if the interfering signal has a spectral content sufficiently extended and the system that receives it is not capable of make a sufficiently selective filtering [16].

In order to address the problem it is important to understand the phenomenon in depth. Firstly, a distinction must be made according to the type of emission and the means by which the signal is transmitted. We can highlight three mechanisms through which the coupling between systems happens:

- *Conduction*: the disturbance propagates through a conductor, such as power cables, signal cables, ground wire, or other low-impedance paths;
- *Electromagnetic radiation*: the source circuit behaves as an antenna, as well as the receiver, and the signal is radiated through the free space;
- *Coupling reagent*: when different circuits have a common impedance.

Since the former two mechanisms are the main modes of interaction, a classification of compatibility issues may be performed by dividing them into four categories:

1. Conducted emissions (CE);
2. Conducted susceptibility (CS);
3. Radiated Emissions (RE);
4. Radiated Susceptibility (RS).

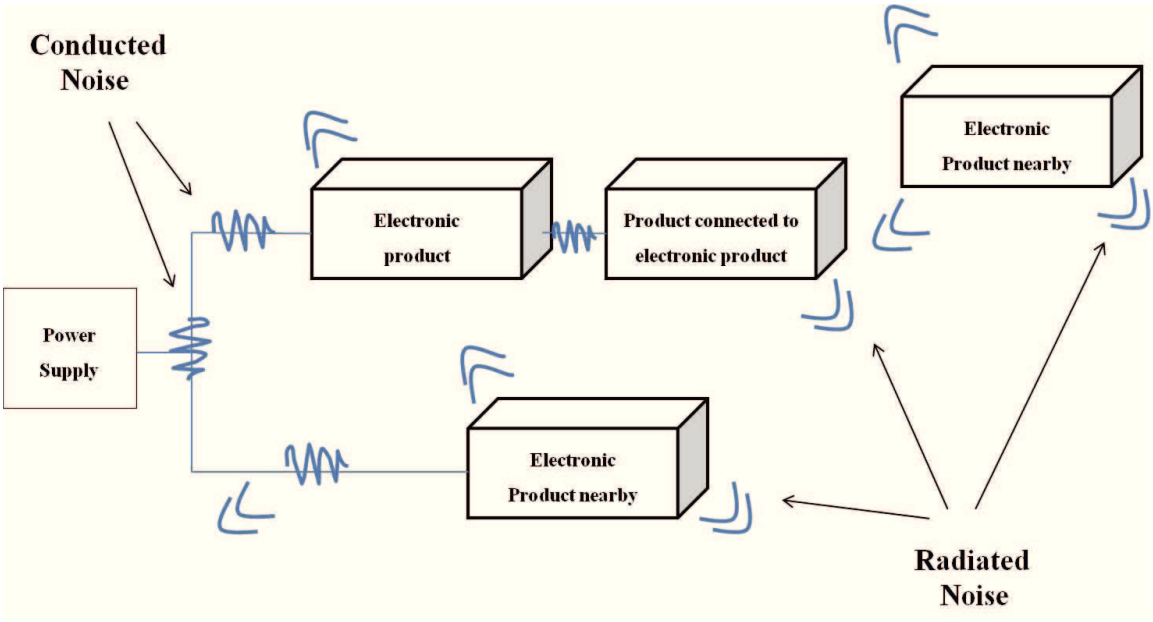


Fig. 2.2 Main mode of coupling electromagnetic disturbances: conducted and radiated noise.

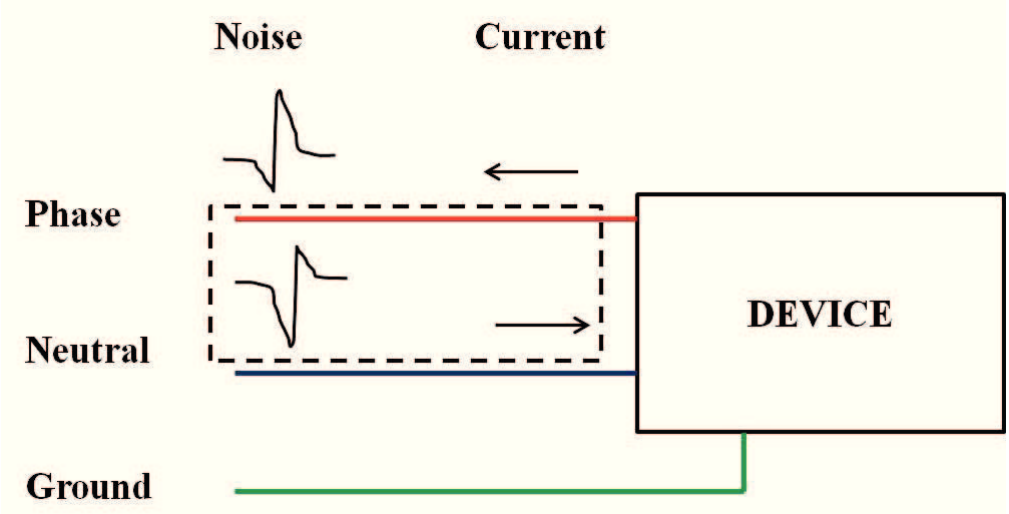
In the following we will consider only the conducted emission. The reduction of conducted emissions can also lead to the reduction of any radiated emission, generated by the same currents that travel long conductors, which can act as antennas.

2.2 Conducted EMI

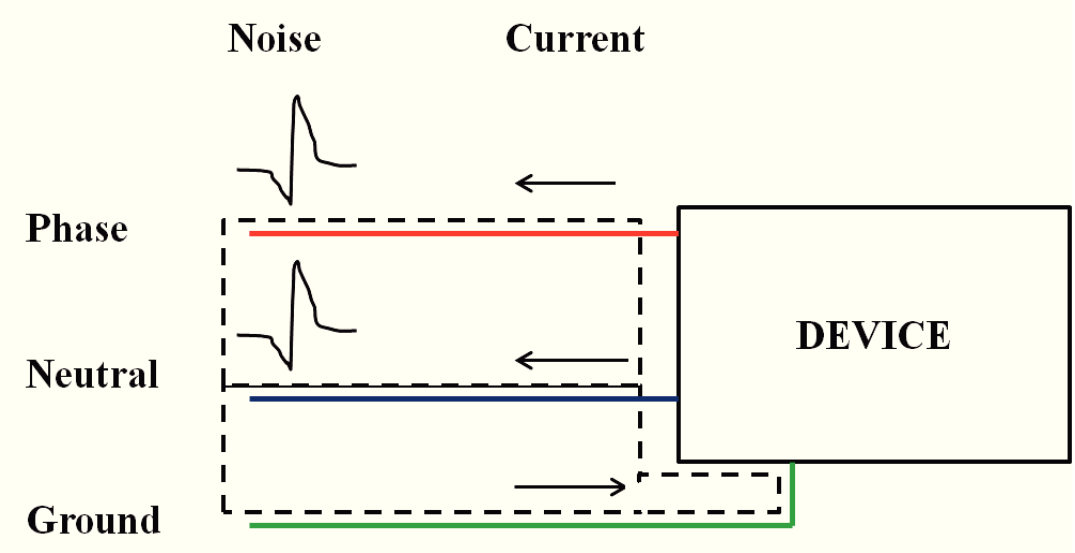
Conducted electromagnetic emissions are all the disturbances that propagate through the interconnecting wiring between a device and the network (power cord), or between multiple devices of the same device, or between different devices [18]. From the definition of conducted emissions is possible to highlight two important issues:

1. An external problem that concerns all electromagnetic coupling between the device and the network, or between the system and other systems in the same electromagnetic environment in which it is inserted;
2. An internal problem that concerns the electromagnetic coupling between the different components that make up the apparatus itself.

Conducted emissions are generated by two basic mechanisms: *differential mode* and *common mode*. The differential mode interference affecting only the conductors of a system, while the common mode interference affect all of the conductors and the ground reference. The differential voltage mode (MD) is an electrical potential difference between two conductors junk. This electrical potential difference, originated by the variations of the current required by the load at different frequency from the network, is due to electric currents in the conductors in the opposite direction, for that reason those of MD. There is a common-mode voltage (MC) whenever there is a electrical potential difference between one or more unwanted conductors and the ground reference. This tension, generated by the noise of connections that form common to several circuits (often connections to ground), is due to electric currents in the conductors in the same direction, so said common mode currents [19].



(a)



(b)

Fig. 2.3 Conducted Emission: a) differential mode interference: the conductors are affected by the voltage and current of the same magnitude but opposite sign; b) Common mode: the voltage and current on the phase conductors and neutral have the same sign and the same magnitude; currents close again through the ground wire.

Conducted noise currents are measured by a spectrum analyzer connected to the LISN (*Line Impedance Stabilization Network*) placed between the equipment (device) to be

tested (EUT, *Equipment Under Test*) and power source. A typical test configuration is illustrated in Fig. 2.4.

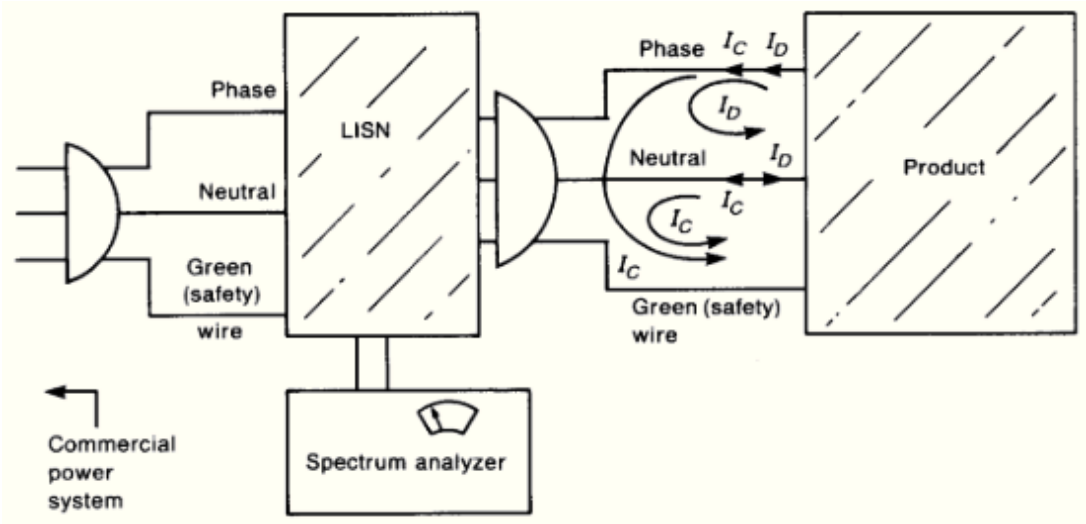


Fig. 2.4 Illustration of the use of a LISN in the measurement of conducted emissions of a product.

The power cord of the product is plugged into the input of the LISN. The output of the LISN is plugged into the commercial power system. AC power passes through the LISN to power the product. A spectrum analyzer is attached to the LISN and measures the "conducted emissions" of the product [16].

The spectrum analyzer measures the amplitude of the disturbance, the variation of frequency, existing between the conductors and the ground reference. It is important that the amplitude of the noise measured on each active conductor does not exceed the limits imposed by the rules for the entire frequency range fixed for the device analyzed.

So that the impedance of the power cord to the outlet of the device under test does not undergo significant variations from site to site and from the same site up changes to the network, you need to input the LISN which makes constant and defined for all the

frequencies of the measuring conducted emissions. The LISN also serves to block the conducted emissions in the network supplying the equipment under test, so as not to pollute the measurement made.

2.3 EMC regulations

In the past these issues were usually identified as Electromagnetic Interference (EMI) or Radio Interference (RFI), while currently adopts the name of "compatibility" that replaces the concept of positive "interference". The reasons for EMC having grown in importance at such a rapid pace are due to:

1. The increasing speeds and use of digital electronics in today's world;
2. The virtual worldwide imposition of governmental limits on the radiated and conducted noise emission of digital electronic products.

In 1979 the U.S. Federal Communications Commission (FCC) published a law that placed legal limits on the radiated emissions from and the conducted emissions out the device power cord of all digital devices (devices that use a clock of 9 kHz or greater and use "digital techniques") to be sold in the USA. Many countries and primarily those of Europe, already had similar such laws in place.

Before the EU directive 89/336/EEC on electromagnetic compatibility and subsequent amendments every country in Europe had its own regulations, which were often at odds with each other. The EU directive 89/336/EEC was subsequently repealed by Directive

2004/108/EC, the legislation currently in force, implemented in Italy by Legislative Decree n. 194 of 6 November 2007.

The merit of this work is the standardization of the CISPR (*Comité International Special des Perturbations Radioelectriques*), subcommittee of IEC (*International Electrotechnical Commission*), international organization that promulgates regulations to facilitate the trade between the nations. The CISPR is composed of several sub-committees, each of which deals with a specific area as shown in the Table 2.1.

Table 2.1 Classification of CISPR.

TECHINICAL COMMITTEE	OBJECT	PUBBLICATION
CISPR/A	MEASUREMENT EQUIPMENT	CISPR 16
CISPR/B	ISM EQUIPMENT	CISPR 11
CISPR/C	HIGH VOLTAGE LINES	CISPR 18
CISPR/D	MOTOR VEHICLES	CISPR 12
CISPR/E	EMISSIONS FROM RECEIVERS IMMUNITY OF RECEIVERS	CISPR 13 CISPR 20
CISPR/F	APPLIANCES FLUORESCENT LAMPS	CISPR 14 CISPR 15
CISPR/G	ITE EQUIPMENT	CISPR 22

In 1985 the CISPR published a set of rules on emissions for ITE equipment, under the title of Publication 22, which is based on Directive 89/336/EEC. The Table 2.2 and the Fig. 2.5 show the limits for conducted emissions of these devices, which are indicated with *Class A* devices used in domestic and industrial use and *Class B* with those for private use [16]. As shown above the FCC and CISPR 22 limit on conducted emission extend from 150 kHz to 30 MHz, from 30 MHz to 1 GHz for radiated emission.

Table 2.2 Limit of conducted emission of ITE.

CLASS A	
f (MHz)	Voltage (almost peak)
0,15 - 0,5	79 dBμV
0,5 - 30	73 dBμV

CLASS B	
f (MHz)	Voltage (almost peak)
0,15 - 0,5	66 - 56 dBμV
0,5 - 5	56 dBμV
5 - 30	60 dBμV

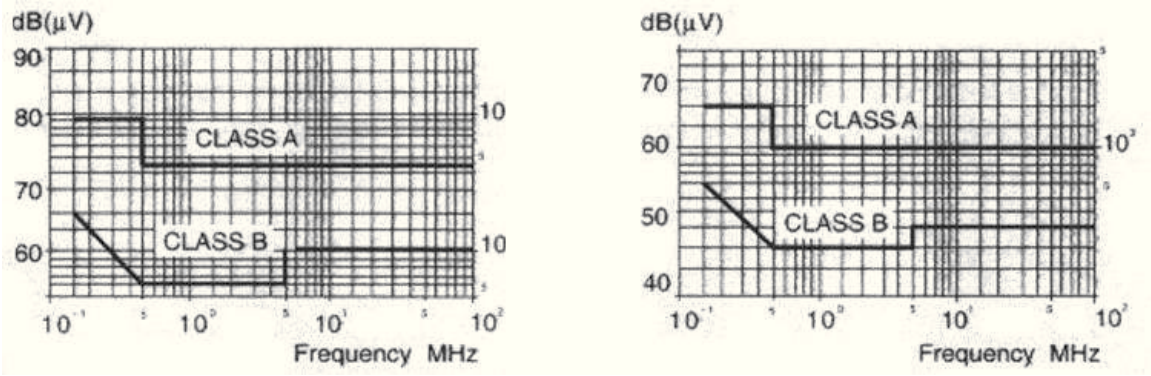


Fig. 2.5 Limits of Conducted Emission for ITE Class A and Class B.

At European level the institution with greater technical expertise in this area is the CENELEC (*Comité Européen de Normalisation Electrotechnique*), which is responsible for collecting and analyzing all national and international standards regarding EMC and remove any technical difference between national standards of member countries.

EU Directive 89/336/EEC and its amendments from 1st January 1996, apply to all electrical and electronic equipment, was subsequently replaced by the current Community legislation, Directive 2004/108/EC. The current Directive states that:

1. The equipment must be constructed in such a way that the electromagnetic disturbance it generates does not exceed a level allowing any other apparatus to function in a manner consistent with their destination;

2. The devices have an adequate level of intrinsic immunity to electromagnetic disturbance that would allow them to function in a manner not intended by the manufacturer.

The rules are a real guide, pointing to the measurement mode, the layout and characteristics of the instruments used and the statistical methods for measurements on large scale production. Today the problem of electromagnetic Compatibility regards all the manufacturers of electronic devices whatever their nationality. Currently the companies are very interested to EMC due to the highly competitive nature of the market. In fact, if a device fails the tests for verifying compliance with rules, cannot be sold, even if it is an innovative product. The initial project will therefore have changes such as configuration of the components. All these operations involve an increase in price that can make lasing competitiveness to the product. Also delays the production cycle, caused by the need to solve problems of EMC, can prevent to market the product at the best time, thus leading to declines in sales. On the other hand, device results in a higher profit and a great reputation to the manufacturer.

Chapter 3

Power module

3.1 Structure and materials of power modules

As it is mentioned in previous capitals many industrial applications use power modules. The structure of a power module is shown in Fig. 3.1. Power module consist of several semiconductor devices on top of many substrates, such as DBC (Direct Bonded Copper), which are soldered to a base plate.

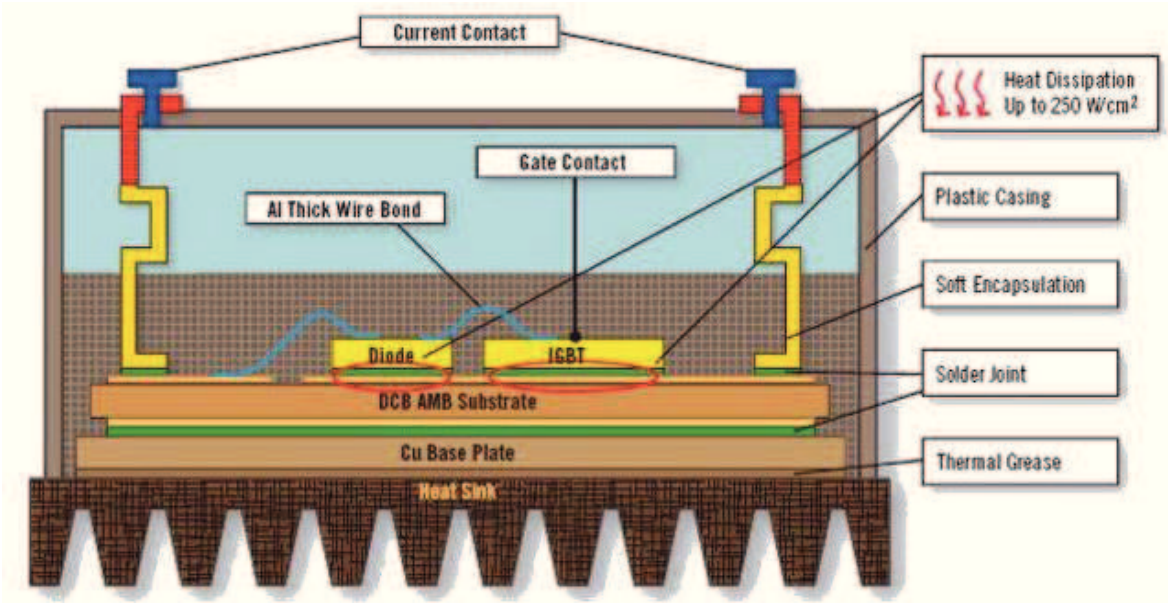


Fig. 3.1: General design of power module with silicon chip soldered to a ceramic substrates.

Fig. 3.2 shows the structure of a power module with two IGBTs and two diodes in the most common current technology with substrates made of *DCB*-ceramics with Al_2O_3 or AlN isolation, combining good thermal conductivity and high isolation voltage.

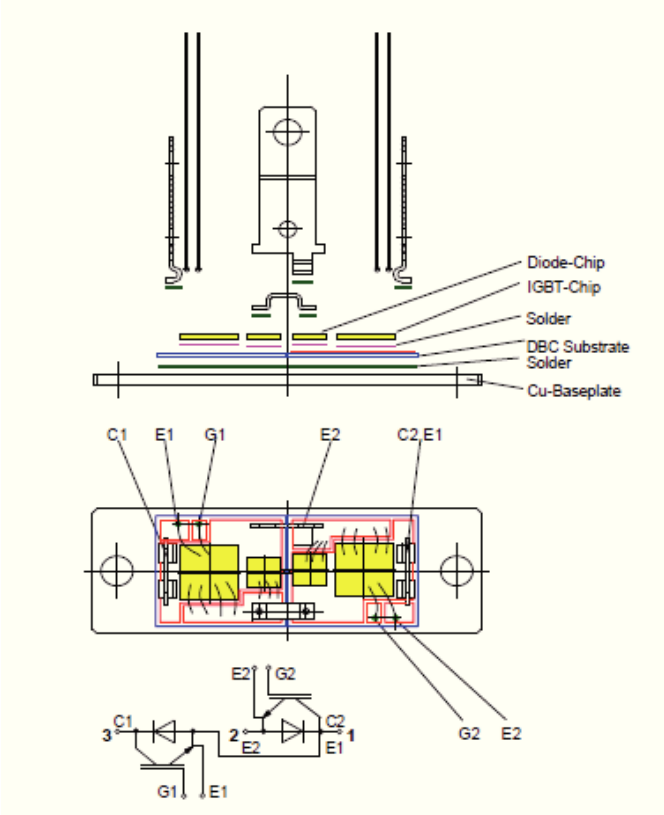


Fig. 3.2: Structure of Power Module with two IGBTs and two diodes.

The currently used isolation substrates for power modules are listed in the table 3.1:

Table 3.1: Isolation substrates for power modules.

Isolation material	
Ceramic	aluminum oxide Al_2O_3 aluminum nitride AlN (beryllia oxide BeO)
Organic	Epoxy; polyimide (Kapton);

Isolation material (Substrates)	
	Direct **C**opper **B**onding);
Metal Sheets	AMB (**A**ctive **M**etal **B**razing).
Metal Sheets	IMS (**I**nsulated **M**etal **S**ubstrate) Multilayer-IMS
Thick film layers	TFC (**T**hick **F**ilm **C**opper)

The combination of various materials with a wide range of CTEs (Coefficients of Thermal Expansion) leads to several issues within the assembly, especially the thermal mismatch between the DBC and the base plate or cooler. This is particularly true when these plates are made of conductive metals such as copper or aluminum, as is usually the case.

An important aspect of packaging technology is the selection of material to use for the substrate. Many options are available and selection largely guided by the thermal requirements of the application. The insulating layer between the power semiconductors and the heatsink is a substrate, which can be of different technology, such as: DBC (Direct Bonded Copper), AMB (Active Metal Brazed), IMS (Insulated Metal Substrate) and TFC (Thick-Film-Copper).

The most widespread substrate is Al_2O_3 ceramic. Over the past few years the thickness of this substrate was reduced from 0.63 to 0.38 mm for a number of applications to reduce the thermal resistance (Rth) of the chip to the heat sink [20].

The layers are usually Cu - Al_2O_3 - Cu. Typical thicknesses of the layers are as follows.

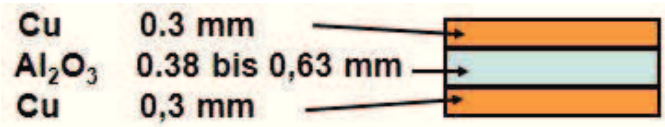


Fig. 3.3: Typical thicknesses of the layers.

A DBC substrates consists of a layer of ceramic insulator bonded between two layers of copper, providing electrical insulation and excellent thermal path to a single heatsink [21] (see Fig. 3.4 and Fig. 3.5).

Direct bonded copper is composed of a ceramic tile with a sheet of copper bonded to one or both sides by a high-temperature oxidation process.

Ceramic material used in DBC include:

- Alumina (Al_2O_3), which is widely used because of its low cost. It is however not a really good thermal conductor (24-28 W/mK) and is brittle;
- Aluminium nitride (AlN), which is more expensive, but has far better thermal performance (> 150 W/mK);
- Beryllium oxide (BeO), which has good thermal performance, but is often avoided because of its toxicity when the powder is ingested or inhaled.

With its good thermal conductivity and excellent dielectric properties, the ceramic layer within the DBC provides the silicon chips the essential electrically isolated thermal path with negligible impact on the overall thermal performance of the assembly [21]. For this reason DBC substrates are commonly used in power modules.

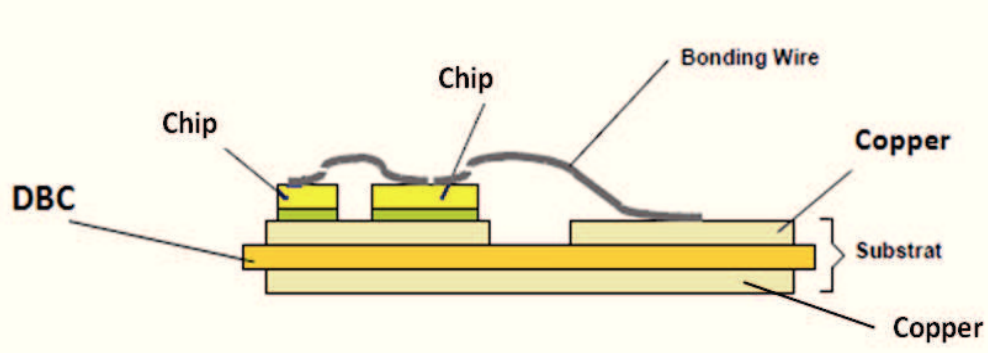


Fig. 3.4: Profile of DBC substrate show electrical isolation and low thermal resistance.

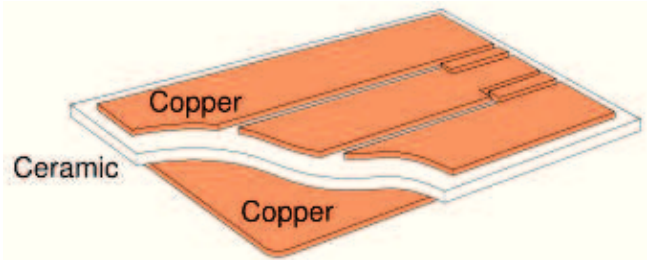


Fig. 3.5: Structure of a DBC.

The bottom side of the DCB-ceramic substrate is fixed to the module base plate by soldering, see Figure 3.6 and Fig. 3.7.

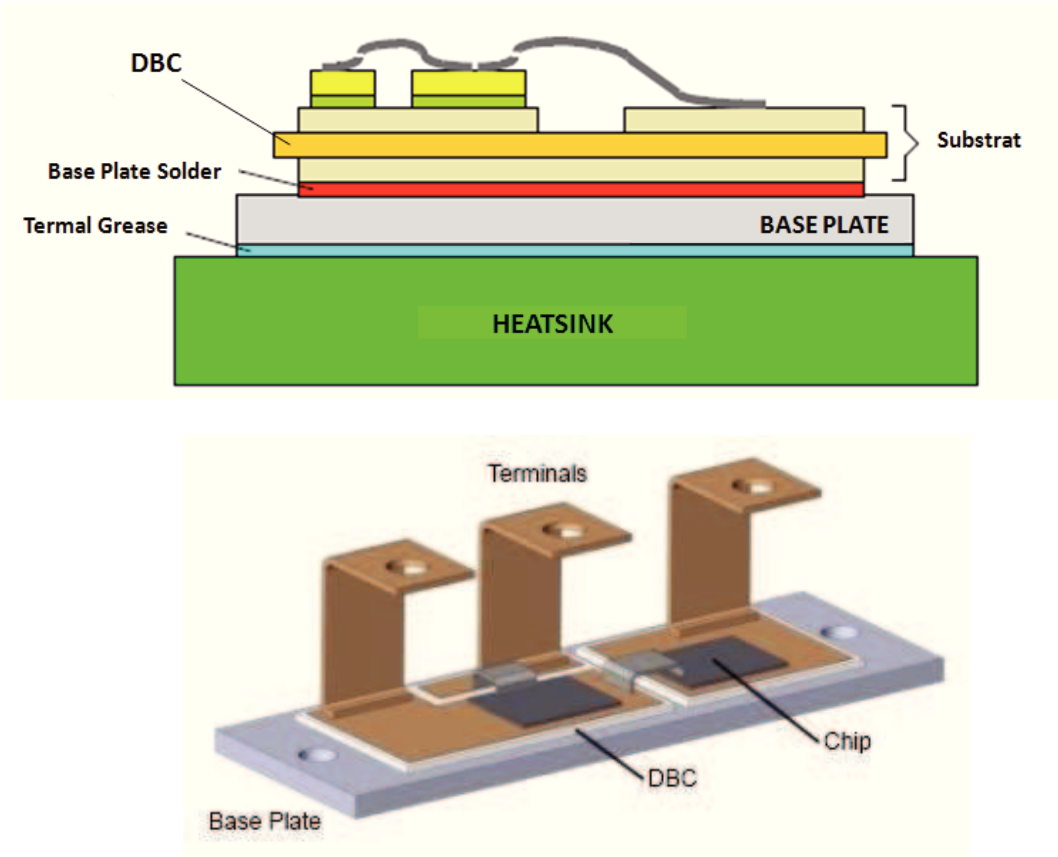


Fig. 3.6: Views of power module.

Advantages of the DCB-technology compared to others are:

- high current conductivity due to the copper thickness;
- good cooling features due to the ceramic material;
- the high adhesive strength of copper to the ceramic (reliability);
- the optimal thermal conductivity of the ceramic material [7],[22].

The AMB process ("brazing" of metal foil to substrate) has been developed on the basis of DCB technology. The advantages of AMB-substrates with AlN-ceramic materials compared to substrates with Al_2O_3-ceramic materials are e.g. lower thermal resistance,

lower coefficient of expansion and improved partial discharge capability. Figure 1.43 explains the differences between DCB and AMB.

The IMS (Insulated Metallic Substrate) is a doped polymer covered on one or both sides by a thin copper layer. IMS is used in power conversion, motor drivers, solid state relays and welding machines. IMS substrates have relatively high coefficients of thermal expansion and thus limited temperature stability and cycle life, while the coefficients of thermal expansion in DBCs are similar to silicon. Whereas IMS have low current carrying capacity, DBCs offer high current carrying capacity. Both substrates exhibit good heat dissipation. The main function of the base plate is as a mechanical support for the system whilst also transferring the heat, primarily via conduction, to the heatsink. When the passive cooling is insufficient, then base plates with larger surface areas can be utilized in active cooling. The thermal grease between the chip and the heatsink limits the thermal dissipation and induces temperature in-homogeneity. Aluminum wire bonding limits the current capability and fuse with high current leading to catastrophic failures [23]. Aluminum wire bonding are used to interconnect the emitter and gate pads from the device to the outside leads. One fundamental difference between power modules is that they are designed either with or without a base plate. In modules with no base plate the DBC substrate is mounted directly onto the heat sink (Fig. 3.7).

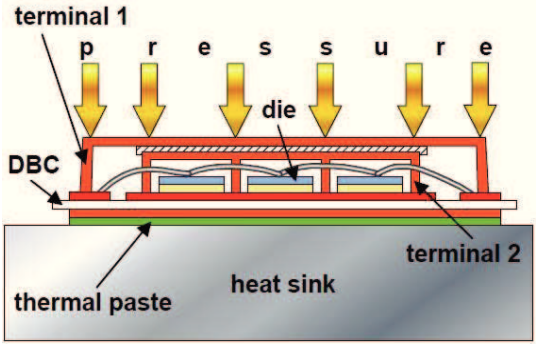


Fig. 3.7: Power module without a base plate.

Such modules are characterized by the use of few large chips with good heat spreading through the base plate:

Advantages:

- Mechanically more robust during transport and assembly;
- Larger thermal mass, lower thermal impedance within the range of 1 s.

Disadvantages of modules with soldered or bonded chips (IGBT modules):

- Higher thermal resistance chip because base plate bending requires a thicker layer of thermal paste;
- Reduced slow power cycling capability, since the large-area base plate solder pads are susceptible to temperature cycles;
- Higher internal terminal resistances, since, for thermo-mechanical reasons, the design is based on small ceramic substrates that require additional internal connectors;
- Increased weight.

Such modules use smaller chips and achieve thermal spreading on the heat sink thanks to heat sources which are better spread.

Advantages:

- Lower thermal resistance because layers are omitted, even contact with the heat sink results in thinner thermal paste layers;
- Improved thermal cycling capability; because of removal of solder fatigue in base plate soldering (because there is no base plate);

- Smaller chips; lower temperature gradient over the chip means a lower maximum temperature and less stress under power cycling conditions;
- Few large ceramic substrates with low terminal resistance.

Disadvantages:

- No heat storage;
- Processable chip size is limited, resulting in more parallel connections;
- Increased requirements for thermal paste application.

Chapter 4

Numerical methods in electromagnetism and simulation tools

4.1 Generality on numerical methods

The resolution of the problems of the electromagnetic type, as it is the case for several other scientific fields, can be addressed with analytical methods as long as the system does not present a high level of complexity. In fact, otherwise, when the geometries are no longer simple and regular, it becomes much more difficult the resolution of the differential equations that govern it, and then it is necessary adopt methods based on numerical techniques. The most widely used for the calculation of the electromagnetic fields are:

1. Finite Element Method (FEM);
2. Partial Element Equivalent Circuit (PEEC);
3. Method of Moment (MOM).

The idea behind is to calculate the value of the variables you want only at certain points of the domain of interest, transforming the differential equations that describe the problem in algebraic equations approximate, and respecting the boundary and initial conditions.

In the following there is a more detail description of the three methods and tools used for the analyses.

Table 4.1: Main features of the most common EM simulation techniques.

Method	FEM	MoM	PEEC
Formulation	Differential	Integral	Integral
Solution variables	Field	Circuit	Circuit
Solution domain	TD or FD	TD or FD	TD and FD
Cell geometries	Nonorthogonal	Nonorthogonal	Nonorthogonal
Advantages	Cell flexibility Complex materials	Cell flexibility	Same TD/FD model Comb. Circuit & EM Cell flexibility

4.2 Finite Element Method

4.2.1 Generality

The FEM (*Finite Element Method*) is one of the most widely used numerical techniques that allows to obtain approximate solutions to problems described by equations partial differential equations (PDEs). Originally, the FEM was developed by engineers for the mechanical calculation of structural elements. Today it is widely used in many areas both of scientific world and of industry, to make accurate modeling of various phenomena in the field of electromagnetism, structural and thermal analysis, fluid dynamics and also in problems so-called " Multiphysics " where you have to solve systems of coupled differential equations. It is possible to split the FEM in three main phases:

1. The first phase consists of the subdivision of the problem domain in subdomains called finite elements. In the case of the two-dimensional problems finite elements are usually triangles or quadrangles, similarly, in the case are three-dimensional tetrahedrons or parallelepipeds. Due to their better adaptability triangles and tetrahedrons are used more frequently. The set of the totality of all these elements is called a *mesh*.
2. The second phase is the translation of a BVP (*Boundary Value Problem*) in a system of linear equations algebraic. The two most common ways to get this system are the minimization of a functional, generally representing the energy of system and the variational methods as one of weighted residues of Galerkin.

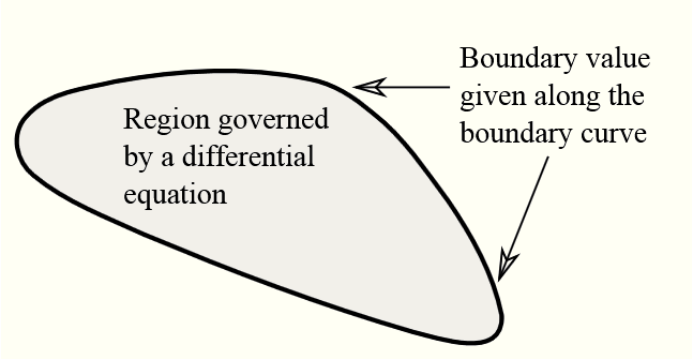


Fig. 4.1 Boundary Value Problem.

In each finite element, the solution (eg. a electromagnetic variable) is approximated by a series of simple functions called shape functions, associated to the degrees of freedom (DOF - degrees of freedom) of the problem. The degrees of freedom are often geometrically associated with both the vertices with both finite element interior points called nodes.

3. Finally, the equations of the different elements are assembled into a global system of linear equations algebraic, which resolved, in the third phase, known as post-*processing*, enable to perform the processing and interpretation of the results of the solution of the system of equations.

4.3 FEM and electromagnetism

4.3.1 Finite Elements and shape function

In this section some aspects of problems in electromagnetic field are presented. In scalar problems the field is calculated in the nodes and unknown approximate function is obtained by interpolating the nodal values by scalar functions $\alpha(\vec{r})$. The variable field V at each point of a finite element can be expressed as:

$$V(\vec{r}) = \sum_{i=1}^{N} V_i \alpha_i(\vec{r}) \tag{4.1}$$

where:

- N is the number of nodes of the element;
- V_i is the value of V to node i.

In the two-dimensional case, at any point $r = (x, y)$ internal a triangular element (Fig. 4.2) the linear shape function $\alpha(\vec{r})$ is defined as:

$$\alpha_i(\vec{r}) = \frac{A_i}{A} \tag{4.2}$$

where A_i is the area of a element section and A is the total area of the element (see Fig. 4.2).

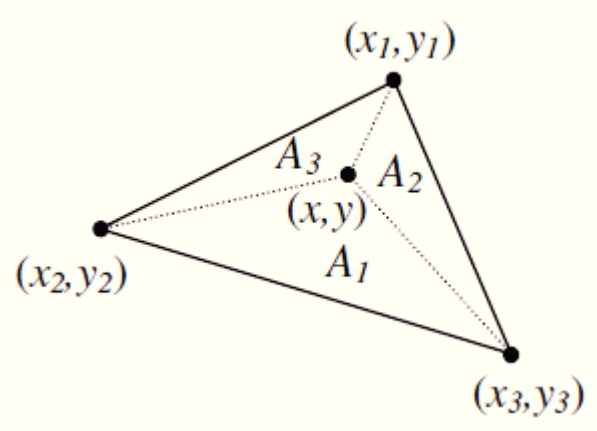


Fig. 4.2 Triangular Finite Element.

Considering $i = 1, 2, 3,$ A_i and A can be calculated as follows expressed:

$$A_i = \frac{1}{2}\begin{pmatrix} 1 & x & y \\ 1 & x_{i+1} & y_{i+1} \\ 1 & x_{i+2} & y_{i+2} \end{pmatrix}$$
$$A = \frac{1}{2}\begin{pmatrix} 1 & x & y \\ 1 & x_{i+1} & y_{i+1} \\ 1 & x_{i+2} & y_{i+2} \end{pmatrix} \tag{4.3}$$

The functions $\alpha_i(\vec{r})$ are called Lagrangian and fulfill the following relations:

$$\sum_{i=1}^{3} \alpha_i(\vec{r}) = 1 \tag{4.4}$$

$$\alpha_i(\vec{r}_j) = \begin{cases} 1 \text{ if } i = j \\ 0 \text{ otherwise} \end{cases} \tag{4.5}$$

For three-dimensional problems in the time or frequency domain, it is generally necessary to use a vector variable. With a such as variable we can rewrite the expression (4.6) using the same shape function present in (4.1):

$$\vec{U}(\vec{r}) = \sum_{i=1}^{N} \vec{U}_i \alpha_i(\vec{r}) \tag{4.6}$$

where $\vec{U}_i$ is the unknown nodal vector in the i-th node that is to say, we have 3N scalar coefficients.

Equation (4.6) can be used only if the unknown vector variable is continuous throughout the entire domain of the problem as in the case of vector potential $\vec{A}$ when it is used for the solution of problems eddy current. In fact, if we consider a region in which you want to calculate the electric field vector $\vec{E}$ or the magnetic field vector $\vec{H}$, characterized by material inhomogenities, the normal component of these vectors will be discontinuous at the interface between the different materials. Similarly, if in the same region you want to determine the vectors $\vec{D}$ or $\vec{B}$, will be the tangential component to be discontinuous at the interface.

In these cases the (4.6) is inappropriate and should be used an expression that takes account of these discontinuities. Below is the equation (4.7) that makes use of the vector function $\vec{w}$:

$$\vec{U}(\vec{r}) = \sum_{i=1}^{N} U_i \vec{w}_i(\vec{r}) \tag{4.7}$$

Given a 3D mesh consists of elements of tetrahedral shape (Fig. 4.3), it is possible to associate a vector shape function $\vec{w}_i$ to every edge of a tetrahedron.

By performing the dot product between the function $\vec{w}_i$ constant and the vector lying along the edge of the tetrahedron $\vec{e}_i$ with $i = 1,2,...,6$ we obtain the following relationship:

$$\vec{e}_i \cdot \vec{w}_j = \delta_{ij} \tag{4.8}$$

where δ_{ij} is the Kronecker symbol.

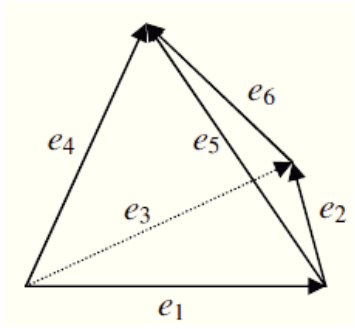


Fig. 4.3 Tetrahedron Element.

If for every element of tetrahedral shape the unknown function $\vec{U}$ is approximated through function $\vec{w}_i$ we obtain:

$$\vec{U}(\vec{r}) = \sum_{i=1}^{6} U_i \vec{w}_i(\vec{r}) \tag{4.9}$$

The integral linear $\vec{U}$ along the edge of the tetrahedron $\vec{e}_i$ is:

$$U_i = \frac{1}{L_i} \int_{\vec{e}_i} \vec{U} \cdot \hat{t}_i \, dl \tag{4.10}$$

where L_i is the length of the element.

4.3.2 The equations of the electromagnetic field

The study of all electromagnetic problems is based on Maxwell's equations, which describe the phenomena of interaction between the electric and magnetic fields. These are four partial differential equations and have the following form:

$$\vec{\nabla} \cdot \vec{D} = \rho^F \tag{4.11}$$

$$\vec{\nabla} \cdot \vec{B} = 0 \tag{4.12}$$

$$\vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \tag{4.13}$$

$$\vec{\nabla} \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \tag{4.14}$$

where:

$\vec{D}$ is the electric induction C/m^2;

$\vec{B}$ is the magnetic induction Wb/m^2;

$\vec{E}$ is the electric field V/m;

$\vec{H}$ is the magnetic field A/m;

ρ^F is the free electric charge C/m^3;

$\vec{J}$ is the density of electric current A/m^2.

The electrical and magnetic induction vectors depend on the respective fields as indicated in the following constitutive relations that, in the simplifying assumptions of isotropic, linear and non-dispersive media takes the form:

$$\vec{D} = \varepsilon \vec{E} \tag{4.15}$$

$$\vec{B} = \mu \vec{H} \tag{4.16}$$

being ε and μ the electrical and magnetic permeability respectively. The current density $\vec{J}$ is related to the electric field $\vec{E}$ and current source $\vec{J}_s$ by the following equation:

$$\vec{J} = \sigma \vec{E} + \vec{J}_s \tag{4.17}$$

where σ is the electric conductivity of the material.

Applying the divergence to both sides of (4.14) is obtained by the equation of continuity given by:

$$\nabla \cdot \left(\vec{J} + \frac{\partial \vec{D}}{\partial t} \right) = 0 \tag{4.18}$$

Starting from Maxwell's equations and the constitutive equations can be obtain different formulations for solving problems based on fields or potential, with one or more unknown variables. Moreover, in any case, it is necessary to impose the boundary conditions (typically Dirichlet or Neumann ones) on the surface of domain in which the problem of the electromagnetic field must to be solved; since, usually, the surfaces coincide with the boundary surfaces of separation between different mediums, the boundary conditions are imposed taking into account of the equations of the fields at the interface between two media with properties different physical.

4.3.3 The equations of electric quasi - stationary field

Considering negligible the temporal variation of induction electromagnetic $\frac{\partial \vec{B}}{\partial t}$ (electric quasi-stationary case) the Maxwell equations reduce to:

$$\nabla \cdot \vec{D} = \rho_f \tag{4.11}$$

$$\nabla \cdot \vec{B} = 0 \tag{4.12}$$

$$\nabla \times \vec{E} = 0 \tag{4.19}$$

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \tag{4.14}$$

Equation 4.21 implies the following relation:

$$\vec{E} = -\nabla V \tag{4.20}$$

where V is the electric scalar potential.

Assuming that 1 and 2 are two materials with different properties, the interface equations are:

$$E_{t_1} - E_{t_2} = 0 \tag{4.21}$$

$$D_{n_1} - D_{n_2} = \rho_s \tag{4.22}$$

$$J_{n_1} + \frac{\partial D n_1}{\partial t} = J_{n_2} + \frac{\partial D_{n_2}}{\partial t} \tag{4.23}$$

where:

E_{t_1} and E_{t_2} are the tangential components of $\vec{E}$ on both sides of the interface;

J_{n_1} and J_{n_2} are the normal components of $\vec{J}$ on both sides of the interface;

D_{n_1} and D_{n_2} are the normal components of $\vec{D}$ on both sides of the interface;

ρ_s is the surface electrical charge density.

4.3.3.1 Electric quasi-stationary analysis

Substituting equations (4.15), (4.17) and (4.20) into the equation of continuity (4.18) we obtain the equation (4.24) that governs the electric quasi-stationary field (EQS):

$$\nabla \cdot \left(\sigma \nabla V + \varepsilon \nabla \frac{\partial V}{\partial t} \right) = 0 \tag{4.24}$$

In the case of operation at steady state we have to neglect the variation time of the electric scalar potential and (4.24) reduces to equation Laplace:

$$\nabla \cdot \left(\sigma \nabla V \right) = 0 \tag{4.25}$$

The analysis of the electric field in time harmonic regime is:

$$-\nabla \cdot \left(\varepsilon \nabla V \right) + \frac{j}{\omega} \nabla \cdot \left(\sigma \nabla V \right) = 0 \tag{4.26}$$

where j is the imaginary unit $j = \sqrt{-1}$ and ω is the angular pulsation.

4.3.3.2 Electrostatic analysis

The electrostatic case is based on the Poisson equation (4.27) which is obtained by (4.11) making use of the constitutive equation (4.15) and eq. (4.20)

$$\nabla \cdot \left(\varepsilon \cdot \nabla V \right) = -\rho \tag{4.27}$$

4.3.4 The equations of magnetic quasi-stationary field

In the case of magnetic quasi-stationary field (MQS), in which the temporal variation of electric induction $\frac{\partial \vec{D}}{\partial t}$ in Maxwell's equations is negligible compared with the density current $\vec{J}$ and ρ^F assumed value zero, the field equations become:

$$\nabla \cdot \vec{D} = 0 \tag{4.11}$$

$$\nabla \cdot \vec{B} = 0 \tag{4.12}$$

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \tag{4.13}$$

$$\nabla \times \vec{H} = \vec{J} \tag{4.28}$$

in this case (4.28) the equation of continuity writes:

$$\nabla \cdot \vec{J} = 0 \tag{4.29}$$

The laws that govern the vector fields in presence of material discontinuities derive from the integral form of Maxwell's equations. Assuming that the subscripts 1 and 2 are referred to two materials with properties different, the equations at the interface are:

$$\left(\vec{B}_2 - \vec{B}_1\right) \cdot \hat{n} = 0 \tag{4.30}$$

$$\left(\vec{D}_2 - \vec{D}_1\right) \cdot \hat{n} = \rho_S \tag{4.31}$$

$$\left(\vec{H}_2 - \vec{H}_1\right) \times \hat{n} = \vec{K}_S \tag{4.32}$$

$$\left(\vec{E}_1 - \vec{E}_2\right) \times \hat{n} = 0 \tag{4.33}$$

where $\vec{K}_S$ is the surface current density.

Since the divergence of the magnetic induction is zero (4.12), it is possible define a magnetic vector potential $\vec{A}$, that satisfies the following relationship:

$$\vec{B} = \nabla \times \vec{A} \tag{4.34}$$

and

$$\vec{E} = -\frac{\partial \vec{A}}{\partial t} - \nabla V \tag{4.35}$$

The field equations in terms of $\vec{A}$ and $\vec{V}$ are:

$$\nabla \times \frac{1}{\mu} \nabla \times \vec{A} + \sigma \left(\frac{\partial \vec{A}}{\partial t} + \nabla V \right) = \vec{J}_S \tag{4.36}$$

$$\nabla \cdot \sigma \left(\frac{\partial \vec{A}}{\partial t} + \nabla V \right) = 0 \tag{4.37}$$

In the region of the domain where $\sigma = 0$ and $\nabla \times \vec{H} = \vec{J}_S$ equation (4.12) becomes:

$$\nabla \cdot \mu \nabla \phi = 0 \tag{4.38}$$

where ϕ is the magnetic scalar potential defined, for a given source of field $\vec{H}_S$, by:

$$\vec{H} = \vec{H}_S - \nabla \phi \tag{4.39}$$

On the surface of the conductor (4.29) implies:

$$-\sigma \left(\frac{\partial \vec{A}}{\partial t} + \nabla V \right) \cdot \hat{n} = 0 \tag{4.40}$$

and:

$$\frac{\partial A_n}{\partial t} + \frac{\partial V}{\partial n} = 0 \tag{4.41}$$

At the conductor interface through which the conductivity changes from σ_1 and σ_2, the equation (4.30) implies:

$$\sigma_1\left(\frac{\partial\vec{A}_1}{\partial t}+\nabla V_1\right)\cdot\hat{n}=\sigma_2\left(\frac{\partial\vec{A}_2}{\partial t}+\nabla V_2\right)\cdot\hat{n} \tag{4.42}$$

Equations (4.36) and (4.37) are not sufficient to solve the problem of field, because the Helmholtz theorem states that a vector field is determined by assigning its rotor and divergence. Thus to ensure the uniqueness of $\vec{A}$ it must specify the divergence (gauge). The divergent value be selected arbitrarily without changing the characteristics of the physical problem; however, a suitable choice of this value allows to simplify the equations to be solved. In the case of stationary and quasi-stationary field the most convenient choice is the gauge Coulomb:

$$\nabla\cdot\vec{A}=0 \tag{4.43}$$

Equations (4.36) and (4.37) can be rewritten as:

$$\nabla\times\frac{1}{\mu}\nabla\times\vec{A}-\nabla\frac{1}{\mu}\nabla\cdot\vec{A}=-\sigma\left(\frac{\partial\vec{A}}{\partial t}+\nabla V\right) \tag{4.44}$$

$$\nabla\cdot\sigma\frac{\partial\vec{A}}{\partial t}+\nabla\cdot\sigma\nabla V=0 \tag{4.45}$$

4.4 FEM algebraic system

Having approximated the unknown function V by (4.1), the condition of stationary of the functional $F(V)$ which represents the energy of electromagnetic field is obtained by imposing the following conditions:

$$\frac{\partial F}{\partial V_i} = 0 \quad \text{i=1,2,...,N} \tag{4.46}$$

where N is the number of nodes in which are not imposed conditions of Dirichlet kind. Since the functional of practical interest are quadratic approximate expression, the set of equations (4.46) written for each element is a linear algebraic system. The systems of equations thus obtained for each element are then assembled all the continuous domain discredited by imposing conditions of congruence in the nodes of interconnection between the various finite elements and taking into account the boundary conditions defined for the problem at hand. The system thus obtained can be expressed in matrix form:

$$[A][X] = [B] \tag{4.47}$$

where:

[A] is a square and symmetric matrix;

[X] is the vector of unknown nodal values;

[B] is the vector of known terms.

The system (4.47) is solved with respect to the unknown nodal values through the use of appropriate algorithms of resolution. Once known values

nodes, the calculation by (4.1) of the unknown function is approximated easily and the data thus obtained can be further processed.

4.5 The FEM for problems in unbounded domains

Practical electromagnetic problems may require to determine the fields in infinite domains. By its nature, the FEM cannot be used to solve problem domain without a closed contour. The most straightforward way to remedy this problem is to truncate the domain, and consequently the mesh, by means of a closed contour, place a suitable distance from the internal source so that null fields on it can be deemed. Generally, truncate the domain introduces errors which are not negligible in solution and this requires significant additional computational resources. To solve these problems a methodology must be coupled to a FEM to solve the problem. In the literature there are several techniques for both problems at low and high frequency with varying degrees of accuracy and computational resources necessary. Some techniques are: the ballooning method, the transformation of coordinates, the infinite elements, the PML (Perfectly Matched Method) and hybrid methods as the FEM / BEM (Boundary Element Method) [24] [25].

4.6 The Partial Element Equivalent Circuit Method

4.6.1 Generality

The Partial Element Equivalent Circuit (PEEC) method is known for its suitability to work out combined circuit and EM-analysis. However, the method has been successfully applied to numerous areas within EM modeling including:

• EM radiation from printed circuit boards;

• Transmission line modeling;

• Noise effect modeling;

• Inductance calculations;

• Scattering problems;

• Power electronic systems;

• Antenna analysis;

• Lightning-induced effects;

• Lightning protection systems;

• Inductance effects in chip design.

Possible applications for the PEEC method are increasing with the continuous development of the method.

The PEEC is an integral method based on a full-wave approach to solve combined circuit and electromagnetic problems in the time and frequency domain. Using PEEC, an electromagnetic problem is transferred to the circuit domain and then solved using circuit theory which gives PEEC a high flexibility to be used in combined electromagnetic and circuit modeling problems. Thus, the method can be applied to different classes of problems, for example power electronics systems and antenna simulation to ensure the

functionality of the system and also comply with electromagnetic compatibility (EMC) regulations.

The theoretical derivation starts from the expression of the total electric field in free space, $\vec{E}^T(\vec{r},t)$, by using the magnetic vector and electric scalar potentials, $\vec{A}$ and ϕ [26]

$$\vec{E}(\vec{r},t) = \vec{E}^i(\vec{r},t) - \frac{\partial \vec{A}(\vec{r},t)}{\partial t} - \nabla\phi(\vec{r},t) \tag{4.48}$$

where $\vec{E}^i$ is an applied external electric field. If the observation point, $\vec{r}$, is on the surface of a conductor, the total electric field can be written as

$$\vec{E}^T(\vec{r},t) = \frac{\vec{J}(\vec{r},t)}{\sigma} \tag{4.49}$$

in which $\vec{J}(\vec{r},t)$ is the current density in a conductor and σ is the electric conductivity of the conductor.

Combining (4.48) and (4.49) result in

$$\vec{E}^i = \frac{\vec{J}(\vec{r},t)}{\sigma} + \frac{\partial \vec{A}(\vec{r},t)}{\partial t} + \nabla\phi(\vec{r},t) \tag{4.50}$$

To transform (4.50) into the electric field integral equation (EFIE) the expressions of the electromagnetic potentials, $\vec{A}$ and ϕ are to be used. The magnetic vector potential, $\vec{A}$, at the observation point $\vec{r}$ is given by [26]

$$\vec{A}(\vec{r},t) = \sum_{k=1}^{K} \mu \int_{v_k} G(\vec{r},\vec{r}') \cdot J(\vec{r}',t_d)\, dv_k \tag{4.51}$$

in which the summation is over K conductors and μ is the magnetic permeability of the medium.

Since no magnetic material medium are considered in this thesis $\mu = \mu_0$. In (4.51) the free space Green's function is used which is defined as [26]

$$G(\vec{r},\vec{r}') = \frac{1}{4\pi}\frac{1}{|\vec{r}-\vec{r}'|} \tag{4.52}$$

In (4.51) $\vec{J}$ is the current density at a source point $\vec{r}'$ and t_d is the retardation time between the observation point $\vec{r}$, and the source point given by

$$t_d = t - \frac{|\vec{r}-\vec{r}'|}{c} \tag{4.53}$$

where $c \approx 3 \cdot 10^8$m/s. The electric scalar potential ϕ, at the observation point $\vec{r}$ is given by [26]

$$\phi(\vec{r},t) = \sum_{k=1}^{K}\frac{1}{\varepsilon_0}\int_{v_k} G(\vec{r},\vec{r}')\cdot\rho(\vec{r}',t_d)\,dv_k \tag{4.54}$$

in which ε_0 is the electric permittivity of free space and ρ is the electrical charge density at the source point.

Combining (4.50), (4.51) and (4.54) results in the well known electric field integral equation (EFIE) or mixed potential integral equation (MPIE) that is to be solved according to

$$\hat{n}\times\vec{E}'(\vec{r},t)=\hat{n}\times\left[\frac{\vec{J}(\vec{r},t)}{\sigma}\right]+\hat{n}\times\left[\sum_{k=1}^{K}\mu\int_{v_k}G(\vec{r},\vec{r}')\right]\frac{\partial\vec{J}(\vec{r}',t_d)}{\partial t}dv_k \tag{4.55}$$

where $\hat{n}$ is the outward normal unit vector of the body surface. In the PEEC method the EFIE, (4.55), is discretized using a method of moments, interpreted as an equivalent circuit and solved using circuit theory. The solution from PEEC model simulations are in general:

- Current I in the materials, where $I = J_a$ being the cross sectional area normal to the current flow.
- Node potentials, ϕ, in the materials.

The values, I and ϕ, together with the PEEC model give a complete characterization of the EM behavior of the modeled structure from which all quantities in Maxwell's equations, (4.11) - (4.14), can be calculated.

4.6.2 Partial Element Equivalent circuit for conductors

In this section the PEEC method for conductors, perfect or lossy, is detailed. The exclusion of dielectric bodies and external fields reduces (4.55) to

$$0 = \hat{n}\times\left[\frac{\vec{J}^C(\vec{r},t)}{\sigma}\right]_{\hat{u}} + \hat{n}\times\left[\sum_{k=1}^{K}\mu\int_{v_k} G(\vec{r},\vec{r}')\cdot\frac{\partial\vec{J}^C(\vec{r}',t_d)}{\partial t}dv_k\right]_{\hat{u}} + \hat{n}\times\left[\sum_{k=1}^{K}\frac{\nabla}{\varepsilon_0}\int_{v_k} G(\vec{r},\vec{r}')\rho^F(\vec{r}',t_d)dv_k\right]_{\hat{u}} \tag{4.56}$$

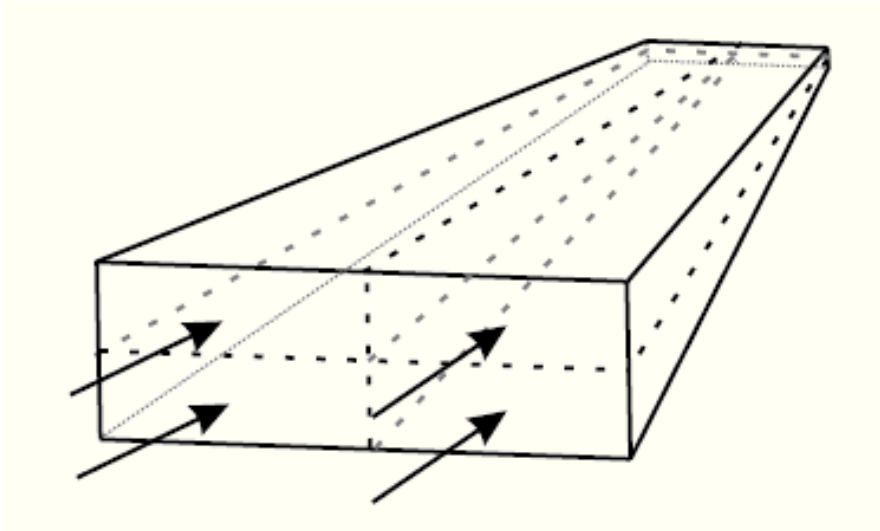


Fig. 4.4: Four volume cells, separated by dashed lines, accounting for the current flowing in the direction of the arrows. The currents in the volume cells are constant and determined by the final PEEC model solution.

Note that the system of equations in (4.56) have two unknowns, the conduction current density, $\vec{J}^C$, and the charge density, ρ_f. To solve the system of equations the following procedure is employed:

1. The current densities are discretized by volume cells and give a 3D representation of the current flow. This is done by defining the rectangular pulse functions

$$P_{\gamma nk} = \begin{cases} 1 \text{ inside the nk-th volume cell} \\ 0 \text{ elsewhere} \end{cases} \tag{4.57}$$

where $\gamma = x, y, z$ indicates the current component of the n-th volume cell in the k-th conductor.

2. The charge densities are discretized by surface cells and give a 2D representation of the charge inside the corresponding volume cell. This is done by defining the rectangular pulse functions

$$P_{mk} = \begin{cases} 1; \text{ inside the mk-th surface cell} \\ 0; \text{ elsewhere} \end{cases} \tag{4.58}$$

for the charge density in the m-th volume cell of the k-th conductor. Using the definitions in (4.57) and (4.58) the current and charge densities can be written as

$$\vec{J}_{\gamma k}^{C}\left(\vec{r}', t_d\right) = \sum_{n=1}^{N\gamma k} P_{\gamma nk} J_{\gamma nk}\left(\vec{r}_{\gamma nk'}, t_{\gamma nk}\right) \tag{4.59}$$

$$q_k^T\left(\vec{r}', t_d\right) = \sum_{m=1}^{M_k} p_{mk} q_{mk}\left(\vec{r}_{mk}', t_{mk}\right) \tag{4.60}$$

where

$$\begin{aligned} t_{\gamma nk} &= t - \frac{\left|\vec{r} - \vec{r}_{\gamma nk'}\right|}{v} \\ t_{mk} &= t - \frac{\left|\vec{r} - \vec{r}_{mk'}\right|}{v} \end{aligned} \tag{4.61}$$

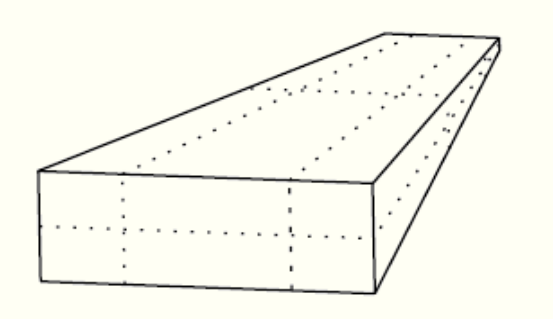


Fig. 4.5: Surface cells which accounting for the charge distribution in the conductors.

The vector $\vec{r}'_{\gamma nk'}$ is the source position vector indicating the center of the n-th volume cell of the k-th conductor in the γ discretization and $\vec{r}_{mk'}$ is the source position vector indicating the center of the m-th surface cell of the k-th conductor. In (4.59), the summation is over all the volume cells in conductor k-th for γ direction current, while in (4.60) the summation is over all the surface cells in conductor k-th.

Pulse functions are also used for the testing functions of the Galerkin method [6]. The inner product between to function $\langle f, g \rangle$ is defined as a weighted volume integral over a cell:

$$\langle f, g \rangle = \frac{1}{a} \int_v f(\vec{r}) g(\vec{r}) dv \tag{4.62}$$

Combining (4.56), (4.59) and (4.60) and using the inner product defined in (4.62) results in the systems of equations given by:

$$0 = \hat{n} \times \frac{\left[\vec{J}^C(\vec{r}', t) \right]}{\sigma} + \left[\sum_{k=1}^{K} \sum_{n=1}^{N\gamma k} \mu \int_{v'} \int_{v_{\gamma nk}} G(\vec{r}, \vec{r}_{\gamma nk'}) \frac{\partial P_{\gamma nk} J_{\gamma nk}(\vec{r}_{\gamma nk'}, t_{\gamma nk})}{\partial t} dv_{\gamma nk} dv' \right] + \hat{n} \times \left[\sum_{k=1}^{K} \sum_{m=1}^{Mk} \frac{\nabla}{\varepsilon_0} \int_{v_{mk}} G(\vec{r}, \vec{r}_{mk'}) p_{mk} q_{mk}(\vec{r}_{mk'}, t_{mk}) dv_{mk} \right] \tag{4.63}$$

The equation (4.63) is the basic discretized version of the electric field integral equation of the PEEC method and it enables to identify the partial electric elements as will be shown in the following.

Partial Inductances**.** The basic expression of partial inductances can be derived from the second term in (4.63) by using:

• The free space Green's function, (4.52).

• The expression $I_{\gamma m} = I_{\gamma m a_m}$ for the total current, $I_{\gamma m}$, through a cross sectional area, a_m.

This results in

$$\sum_{k=1}^{K}\sum_{n=1}^{N\gamma k}\frac{\mu}{4\pi}\frac{1}{a_{v'}a_{v_{\gamma nk}}}\int_{v'}\int_{v_{\gamma nk}}\frac{\frac{\partial}{\partial t}I_{\gamma nk}\left(\vec{r}_{\gamma nk'},t_{\gamma nk}\right)}{\left|\vec{r}-\vec{r}'\right|}dv_{\gamma nk}dv' \tag{4.64}$$

and can be interpreted as the inductive voltage drop, v_L, over the corresponding volume cell. By defining the partial inductance [48] as

$$L_{p\alpha\beta} = \frac{\mu}{4\pi}\frac{1}{a_\alpha a_\beta}\int_{v_\alpha}\int_{v\beta}\frac{1}{\left|\vec{r}_\alpha-\vec{r}_\beta\right|}dv_\alpha dv_\beta \tag{4.65}$$

(4.64) can be rewritten as:

$$v_L = \sum_{k=1}^{K}\sum_{n=1}^{N_{\gamma k}}L_{p_{v'_{\gamma nk}}}\frac{\partial}{\partial t}I_{\gamma nk}\left(t-\tau_{v'v_{\gamma nk}}\right) \tag{4.66}$$

where $\tau_{v'v_{\gamma nk}}$ is the center to center delay between the volume cells v' and $v_{\gamma nk}$. (4.65) is the basic definition for the partial self and mutual inductance using the volume

formulation. It is from this definition that simplified and analytical formulas for the partial inductances for special geometries have been developed.

The interpretation of the second term in (4.63) as the inductive voltage drop (using the partial inductance concept) results in:

• The connection of nearby nodes using the partial self inductance $\left(L_{p_{\alpha\alpha}}\right)$ of the corresponding volume cell (α).

• The mutual inductive coupling of all volume cells using the concept of partial mutual inductance.

This is illustrated in Fig. 4.6 where a voltage source, V_m^L, has been used to sum all the inductive (magnetic field) couplings between all volume cells and it corresponds to the summation in (4.66).

The voltage source is defined as [36]

$$V_m^L(t) = \sum_{\forall n, n \neq m} L_{p_{mn}} \frac{\partial i_n\left(t - \tau_{mn}\right)}{\partial t} \tag{4.67}$$

Where $i_n\left(t - \tau_{mn}\right)$ is the current through volume cell n-th at the earlier time, $\left(t - \tau_{mn}\right)$.

The (4.67) can be rewritten using the voltage v_n (node potential difference)

over the volume cell n as [49]:

$$V_m^L(t) = \sum_{\forall n, n \neq m} \frac{L_{pmn}}{L_{pnn}} v_n\left(t - \tau_{mn}\right) \tag{4.68}$$

A PEEC model only consisting of partial inductances is entitled a $\left(L_p\right)$ PEEC model (see Fig. 4.6).

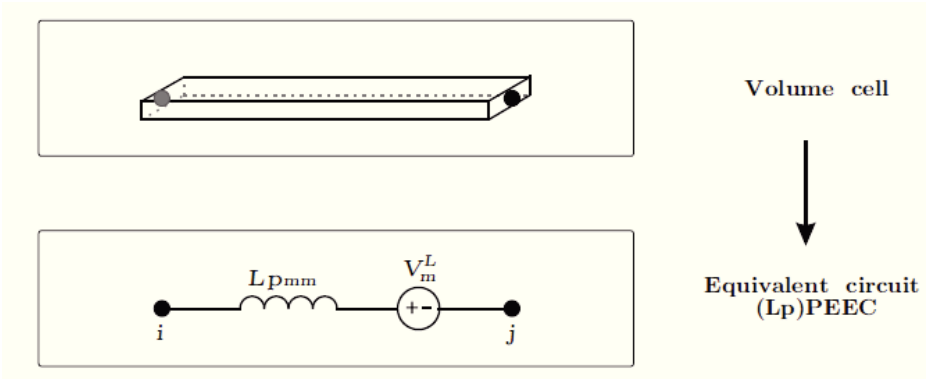


Fig. 4.6 (Lp)PEEC model for volume cell m connecting node i and j.

Coefficients of Potential**.** The basic definition for partial coefficients of potential can be derived from the third term in (4.63) by using the following approximations:

• The charges only resides on the surface of the volumes, i.e. converting the volume integral to a surface integral.

• The integral in the γ coordinate can be calculated using a finite difference (FD) approximation according to

$$\int_v \frac{\partial}{\partial\gamma} F(\gamma)\, dv \approx a\left[F\left(\gamma + \frac{l_m}{2}\right) - F\left(\gamma - \frac{l_m}{2}\right)\right] \tag{4.69}$$

This results in:

$$\sum_{k=1}^{K}\sum_{m=1}^{M_k}\left[q_{mk}(t_{mk})\frac{1}{4\pi\varepsilon_0}\int_{S_{mk}} \frac{1}{\left|\vec{r}^{+} - \vec{r}'\right|} ds' - q_{mk}(t_{mk})\frac{1}{4\pi\varepsilon_0}\int_{S_{mk}} \frac{1}{\left|\vec{r}^{-} - \vec{r}'\right|} ds' \right] \tag{4.70}$$

which can be interpreted as the capacitive voltage drop, v_C, over the actual cell and the vectors $\vec{r}^{+}$ and $\vec{r}^{-}$ are associated with the positive and negative end of the cell respectively [24]. By defining the partial coefficient of potential as

$$p_{ij} = \frac{1}{S_i S_j}\frac{1}{4\pi\varepsilon_0}\int_{S_i}\int_{S_j} \frac{1}{\left|\vec{r}_i - \vec{r}_j\right|} dS_j dS_i \tag{4.71}$$

the capacitive voltage drop can be written as

$$v_C = \sum_{k=1}^{K} \sum_{m=1}^{M_k} Q_{mk} \left(t - t_{mk}\right) \left[pp^{+}{}_{i(mk)} - pp^{-}{}_{i(mk)} \right] \quad (4.72)$$

using the total charge, Q_{mk}, of the mk-th cell.

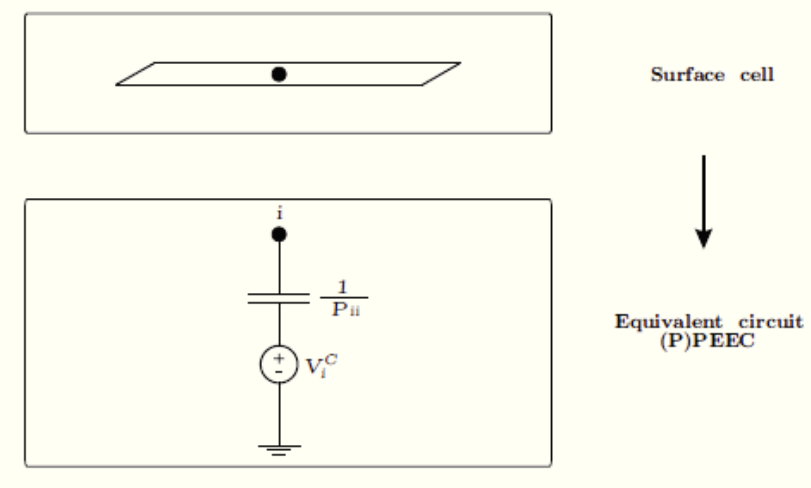


Fig. 4.7: (P)PEEC model for one surface cell node i where P_{ii} is the partial self potential coefficient of the node i and V_i^C accounts for the mutual capacitive coupling from other surface cells.

From the basic definition in (4.71) a number of simplified and analytical formulas for partial coefficients of potential can be derived for special geometries configurations.

The interpretation of the third term in (4.63) as self and mutual partial coefficient of potential (capacitive) coupling results in:

• The connection of each surface cell (node) to infinity through self partial (pseudo-) capacitances.

• Mutual capacitive couplings of all surface cells (nodes) .

This is illustrated in Fig. 4.7 where a voltage source, V_i^C has been used to sum all the capacitive (electric field) couplings from all other surface cells.

The voltage source is defined as [49]:

$$V_i^C(t) = \sum_{\forall jj \neq i} \frac{P_{ij}}{P_{jj}} V_{C_j}\left(t - \pi_{ij}\right) \tag{4.73}$$

Where $V_{C_j}\left(t - \tau_{ij}\right)$ is the voltage over the pseudo-capacitance, $\frac{1}{P_{jj}}$, of the j-th node, at an earlier time, $\left(t - \tau_{ij}\right)$.

4.7 Method of Moments

The Method of Moments (MoM) is a technique used to solve electromagnetic boundary or volume integral equations.

The basic form of the equation to be solved by the Method of Moments is the following:

$$L(f) = g \tag{4.74}$$

Where L is a linear operator, g is a known forcing function and f is the unknown. In electromagnetic problems L is typically an integro-differential operator, f is the unknown function (charge or current) and g is a known excitation source assigned. Let us now expand f into a sum of N weight basis functions,

$$f = \sum_{n=1}^{N} a_n f_n \tag{4.75}$$

where a_n are unknown weight coefficients. Because L is linear, the substitution into (4.74) yields

$$\sum_{n=1}^{N} a_n L(f_n) \approx g \tag{4.76}$$

where the residual is

$$R = g - \sum_{n=1}^{N} a_n L(f_n) \tag{4.77}$$

Let us now generalize the method by which the boundary conditions were previously enforced. We define an inner or *moment* product between a basis function $f_n(\vec{r}')$ and a *testing* or *weighting* function $f_m(r)$ as

$$\langle f_m, f_n \rangle = \int_{f_m} f_m(r) \cdot \int_{f_n} f_n(r') dr' dr \tag{4.78}$$

where the integrals are line surface, or volume integrals depending on the basis and the test functions. Requiring the inner product of each testing function with the residual function to be zero yields:

$$\sum_{n=1}^{N} a_n < f_m, L(f_n) > = < f_m, g > \tag{4.79}$$

which results in the N x N matrix equation **Za**=**b** with matrix elements

$$z_{m,n} = < f_m, L(f_n) > \tag{4.80}$$

and right-hand side vector elements

$$b_m = < f_m, g > \tag{4.81}$$

In the MOM, each basis function interacts with all others by means of the Green's function and the resulting system matrix is dense. All the elements of the matrix must therefore be explicitly stored in memory. This can be compared to other method such as the finite element method, where the matrix is typically sparse, symmetric and banded, in which many elements of matrix are zero [4].

4.8 Q3D Extractor software

The software Q3D Extractor makes use of PEEC method previously described to compute the parasitic components such as the stray capacitance (C), conductance (G), resistance (R) and inductance (L) in both 2D and 3D structures for frequencies up to 1,5GHz.

For this purpose it is necessary to choose the matrices you want to generate, draw the structure which can be created in Q3D or be imported from external software suites such as AutoCAD, specify material properties for each object, identify conductors and specify source excitations. The software then generates the necessary circuit parameters. From these matrices, it is possible to generate lumped equivalent circuit models in any of several SPICE formats.

The following screenshot reports the desktop of the software.

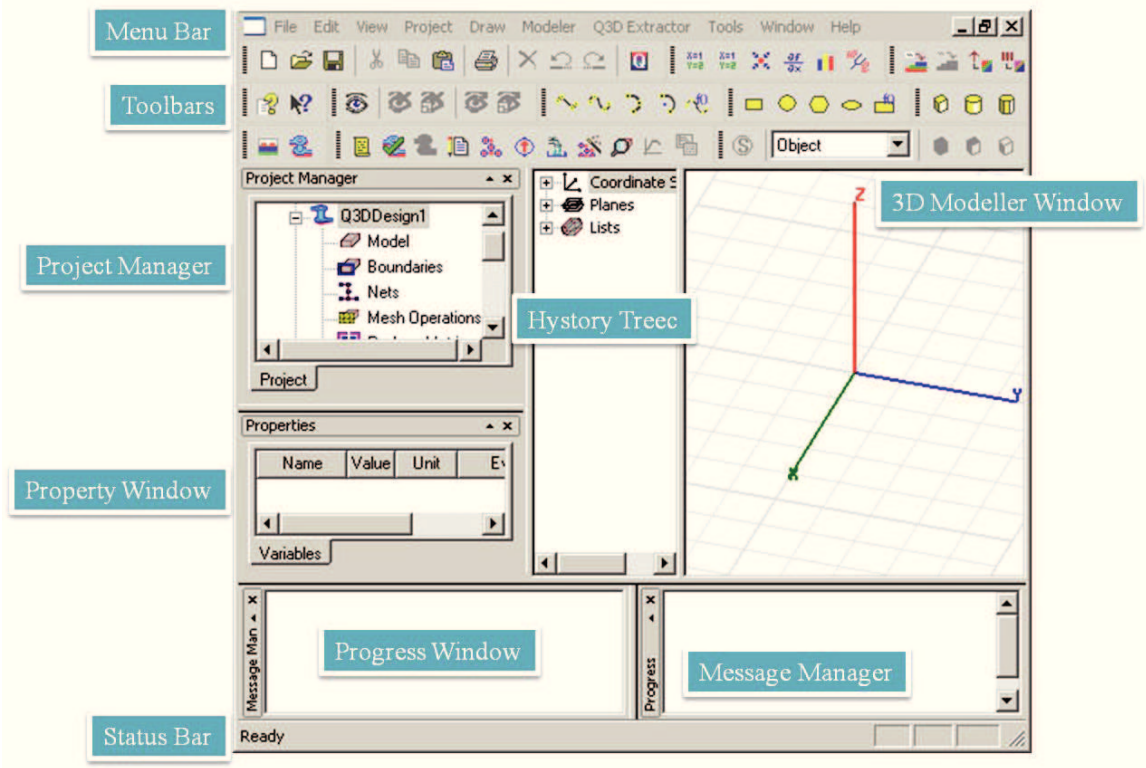


Fig. 4.8 The desktop of Q3D Extractor.

Q3D Ex. utilizes two methods to calculate the self and mutual parasitic elements of a structure: the Method of Moments (MoM) and the Finite Element Method (FEM). In general, the FEM divides the full problem domain into smaller regions (finite elements) and represents the field in each element with a local approximated function. The MoM divides up the surfaces (or volumes) of conductors and dielectrics into many triangular (or tetrahedral) elements to represent the charges and currents present.

Q3D solves DC resistance problems using the FEM while inductance and capacitance problems are solved with the MoM.

Each conducting body in the model has to be assigned to a net which Q3D Ex. then uses to creates surface meshes on all the conductors and dielectrics. These defined nets will then used in the calculation of all the S - Prameters (*Parasitic Components*).

The matrices, R, L, C, can be export to PSpice (through a file *.cir*) to include full wave effects in the circuit simulations.

4.9 PSpice software

To design an electronic circuit or to analyze one requires accurate methods for evaluating circuit performance. Moreover, modern electronic circuits are so complex that computer-aided circuit analysis is indispensable.

PSpice by MicroSim Corporation is one of the many commercial derivatives of U.C. Berkeley SPICE (*Simulation Program with Integrated Circuit Emphasis*). It is widely used for analog circuit simulation.

Writing a circuit file for PSpice simulation is quite easy. First of all, a circuit diagram must be drawn and all the nodes numbered. All the special devices like the diode, SCRs or transistors must be modeled before using them. Sometimes it may be possible to use the default models provided with the software package.

Probe is a separate program that comes with PSpice. It allows the user to look at the waveforms of different current and voltages. After running the PSpice file, the input required for running the probe is written in a .dat file if the .probe command was included in the original pspice circuit file. Probe is also capable of mathematical computations involving currents and/or voltages, including numerical determination of rms and average values and harmonic analysis.

The type of simulation performed by PSpice depends on the source specifications and control statements. The types of analysis usually executed in the PSpice program are as follows:

1. DC Analysis: it is used for circuits with time invariant sources (e.g., steady state dc sources). It calculates all nodal voltages and branch currents over a range of values.
2. Transient Analysis: It is used for circuits with time variant sources (e.g., ac sources/switched dc sources). It calculates all nodes voltages and branch currents over a time interval and their instantaneous values are the outputs.
3. AC Analysis: It is used for small signal analysis of circuits with sources of varying frequencies. It also calculates all nodal voltages and branch currents of a specify a range of frequencies.

Chapter 5

Analysis and reduction of conducted EMI in a power electronic module

5.1 Description

In this section it is described an investigation method developed to analyze the electromagnetic conducted emission of a power electronic module operating up to 50 MHz and to understand how is possible to optimize the electric elements and geometry in order to minimize the noise in phase of the design.

The attention has been focalized on a power electronic module prototype of the *ST*Microelectronic. This module is based on an IGBT power device and consists of 3-phase full bridge operating with a voltage of 600V and current of 40 A, shown in Fig. 5.1.

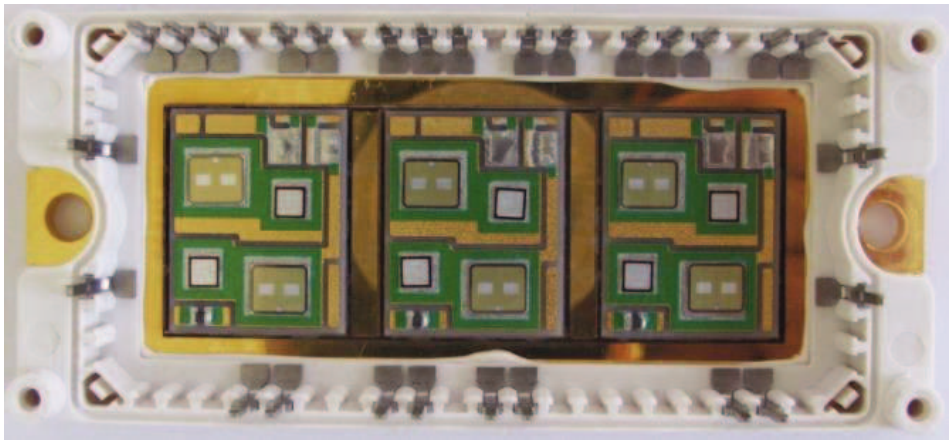


Fig. 5.1: *ST*Microelectronics IGBT Power Module prototype.

The device consists of:

- 6-Pack IGBTs Power Module with short circuit rugged IGBTs;
- 6 freewheeling diodes;
- 3 shunt resistors for the current phase sensing;
- 1 NTC temperature sensor.

As shown in Fig. 5.2, the analysis focused on the first leg of the power module operating in DC-DC step down mode for sake of simplicity. The three legs are all equal to each other and each of them are composed of two part containing a diode in parallel to an IGBT. The Fig. 5.2 highlights the part analyzed and its equivalent circuit.

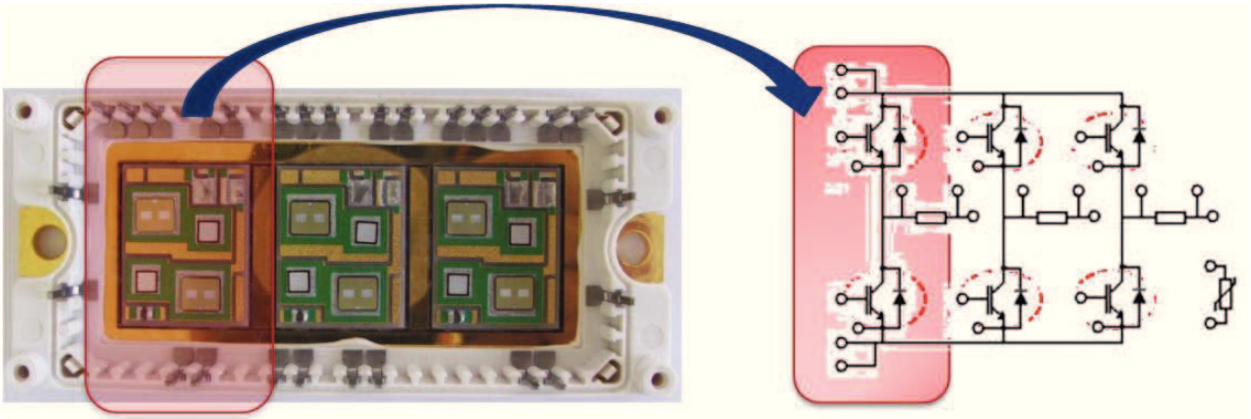


Fig. 5.2: part analyzed part with its equivalent circuit.

As is it mentioned in the Section 5, the software Q3D Ex. is used to generate the equivalent circuit models in a SPICE format and to calculate all the S-Parameters

(*Parasitic Components*). To do this, at the first has been drawn the 3D scheme of the power module reported in the Fig. 5.1 and imported in the Q3d Ex., whose are shown in the following Figures.

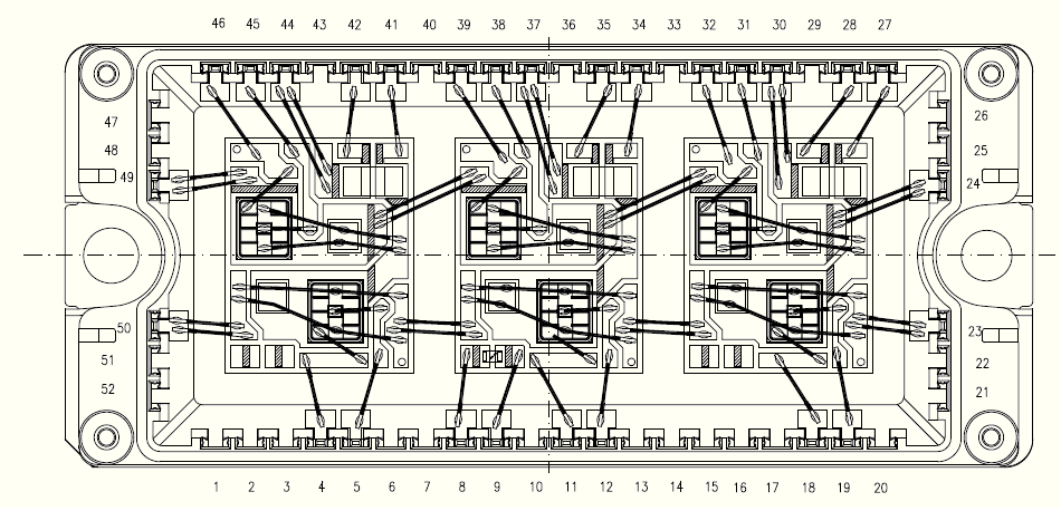


Fig. 5.3: 3D representation of the power module prototype.

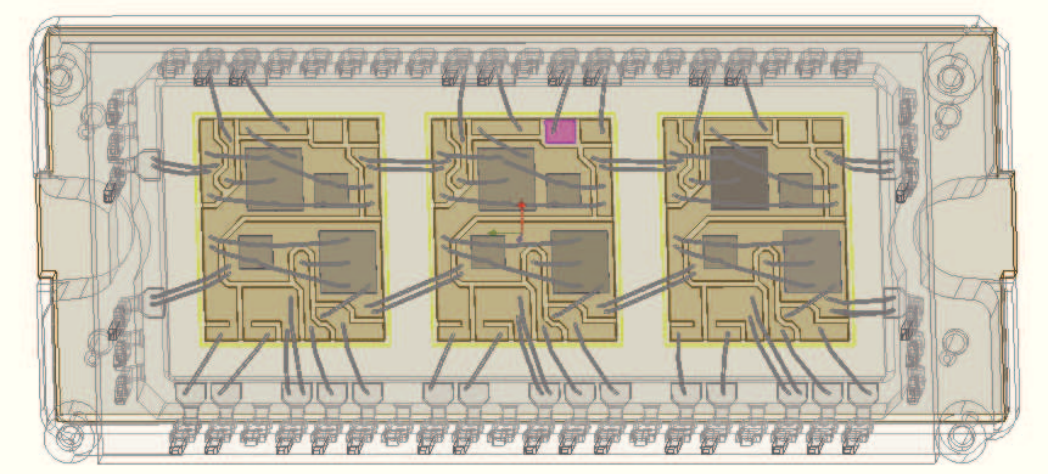


Fig. 5.4: 3D CAD of the power module obtained from Q3d Ex.

The geometrical description of the module is completed in the Fig. 5.5 which represents the side lateral views of the device.

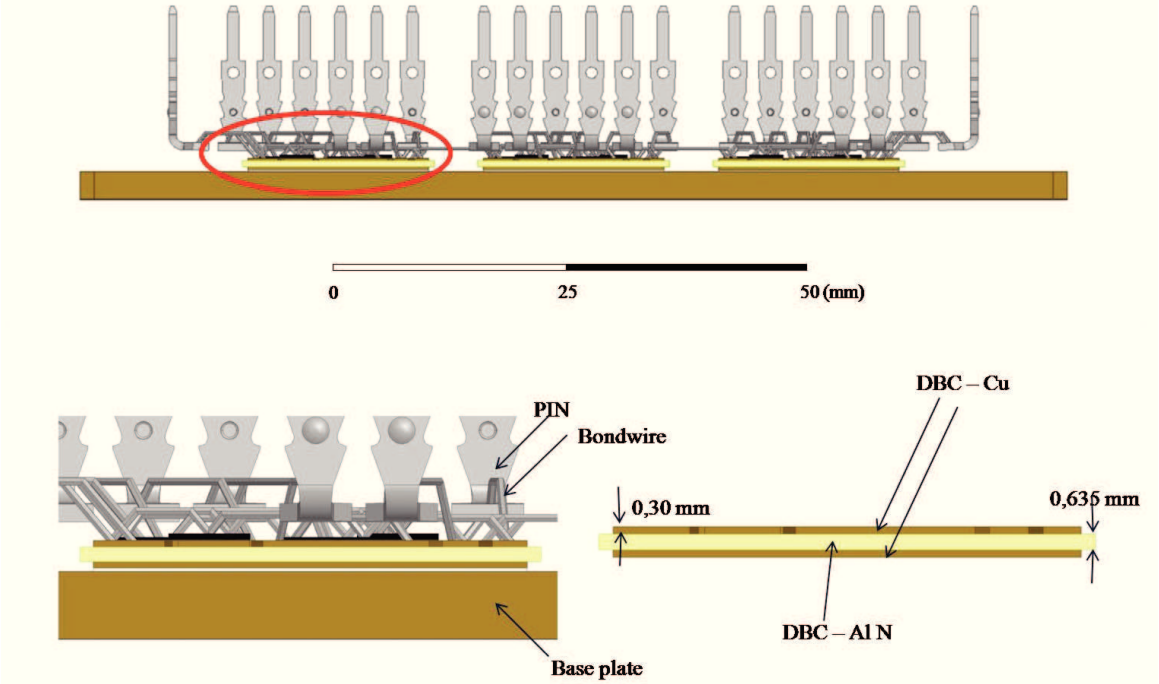
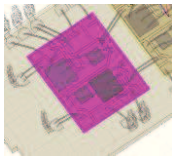
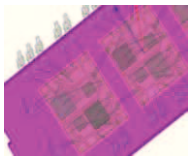
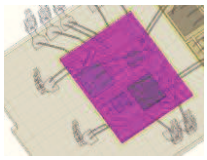
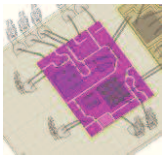
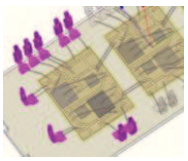
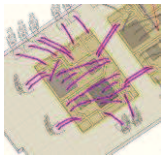
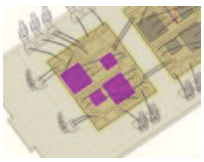
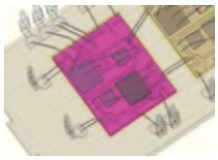


Fig. 5.5: Side views of the device from Q3d Ex.

In the second step the material characteristics of the objects are assigned and specified in the Table 5.1.

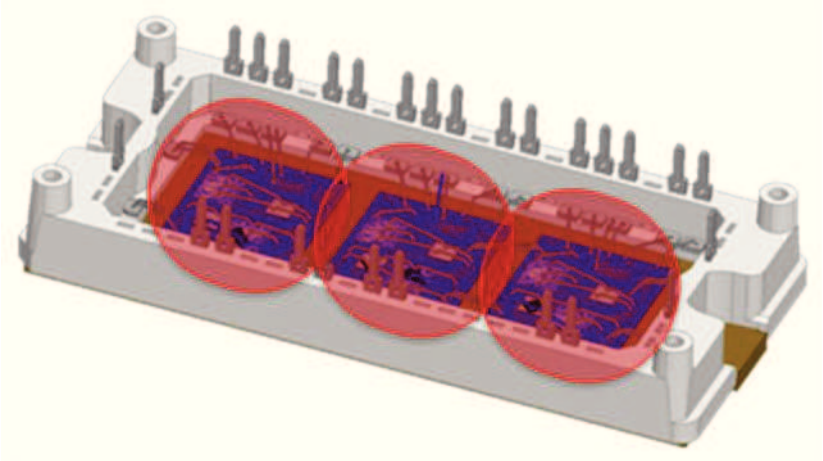
Table 5.1: List of materials.

Element	Material
 DBC-Ceramic	Aluminium Nitride
 Baseplate    PINs	Copper
 Bond wire	Aluminium

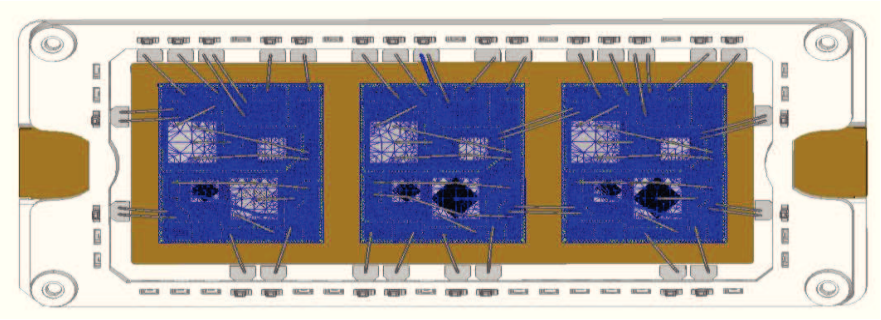
Element	Material
 	Solder

5.2 Analysis

In order to start the analysis it is necessary preliminarily to identify the *nets* of the module which are collections of connected conductor objects separated by non-conducting materials or by the background material. Nets can be assigned only to conductive materials. Each conducting body in the model has to be assigned to a net, which Q3d Ex. then uses to create *surface meshes* on all the conductors and dielectrics (see Fig. 5.6).



(a)



(b)

Fig. 5.6 (a) (b): Views of the surface meshes.

Any net that we want to include in the L,R,C matrices solution must have a single sink defined, along with at least one source. In the Fig. 5.7 there is an example of net with its source and sink.

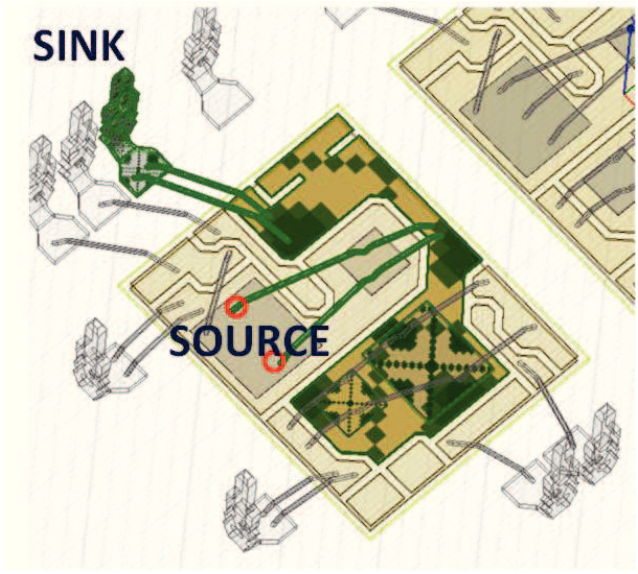


Fig. 5.7: A view of a net.

Through Q3d Ex. we obtain the value of parasitic elements of the first leg. By means of the computation capability of this software it is possible to analyze an electrical circuit constituted of many resistances, inductances and capacitances, self and mutual, which are imported into a SPICE file. From the model so obtained, which is frequency dependent, is possible to evaluate the parasitic elements of the most critical loop inside the module. In order to simplify the computation, only one leg of the module has been taking in exam and the results compared with the measurement carried out on the real prototype.

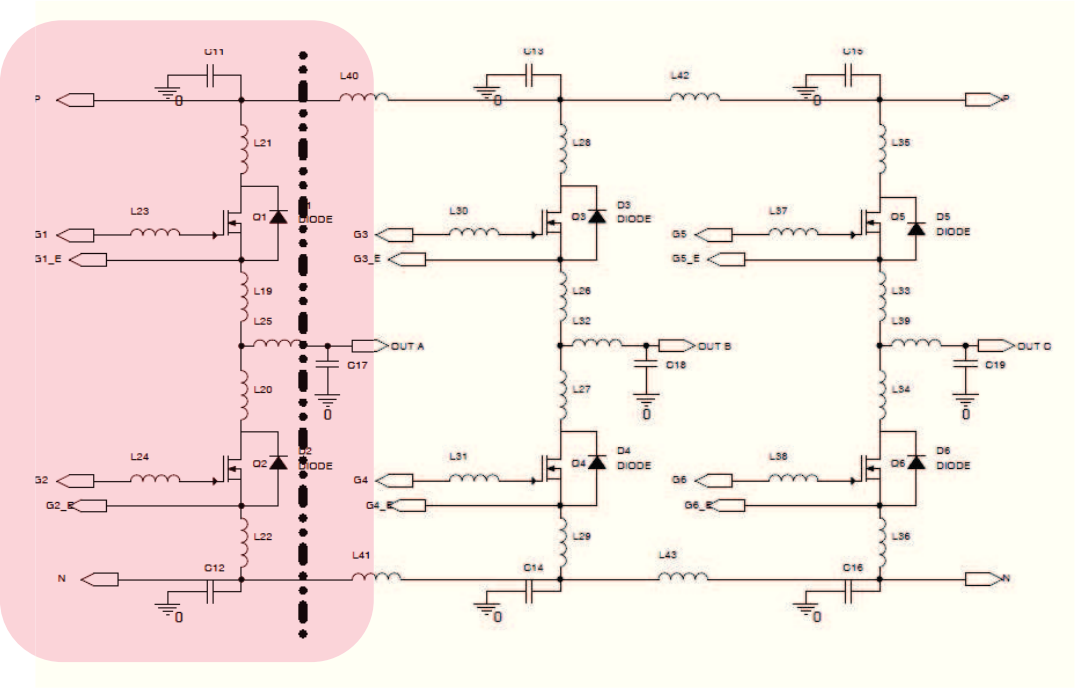


Fig. 5.8: Simplified equivalent circuit with parasitic elements.

The module equivalent circuit shown in Fig. 5.8 has been obtained by a Q3d Ex. simulation without considering the effect of the mutual elements. This simplification is useful to obtain the most important parasitic elements; then the results of this simulation have been compared with the measurements done directly on the module, avoiding in this way to perform very heavy computation on the entire netlist. In fact, normally the

computation requires several hours without considering the mutual elements. The individuation of the most critical parasitic elements of the module is an important topic during the design phase of the power module, strictly depending on the real application for which the power module is to be used. During the commutation of the active devices the overshot amplitude of the V_{CE} of IGBT may accurs for the effect of the high values L di/dt, overcoming the maximum breackdown voltage of the IGBT and diodes and decreasing the reliability of the module. Parasitic elements have to be optimized in order to minimize spikes during the commutation and to reduce electromagnetic interferences (EMI). The Table 5.2 shows the obtained values of the parasitic elements.

Table 5.2: Obtained values of parasitic elements LCR of the 1st leg.

L/nH	C/pF	R/mΩ
L_{21} = 7	C_{21} = 17,75	R_{21}=13
L_{23} = 19,36	C_{23} = 3,70	R_{23} = 48
L_{23b} = 16,22	C_{23b} = 3,57	R_{23b} = 49
L_{19} = 21,45	C_{19} = 27,89	R_{19}=42
L_{20} = 21,38	C_{20} = 27,89	R_{20}=21
L_{24} = 13,52	C_{24} = 2,83	R_{24} = 43
L_{24b} = 16,42	C_{24b} = 2,65	R_{24b} = 46
L_{22} = 15,69	C_{22} = 6,51	R_{22}=31

5.3 Simulation of the power electronic module

The electromagnetic EMI of the power module in DC-DC operation are analyzed by using a IGBT model in the SPICE circuit simulation which in particular enables to evaluate the voltage spikes during the commutation of the power device. A part of overshot amplitude of the V_{CE} is due to the effect of the L di/dt, which causing to reach the maximum breackdown voltage of the IGBT and diodes. The circuit model of the entire system we have considered in the simulation are shown in Fig. 5.8. The considered circuit for the calculation is shown in the Fig. 5.9 and consists of 4 main parts: LISN, DC Link Capacitor, Bus Bar, and the inner part of the power module. This circuit enables to evaluate the voltage spikes erasing during the commutation of the IGBT and accross DC Link voltaged with a tension of 80 V and linked to a load absorbing a current of 40 A; the frequency of commutation is 16 kHz with a duty cycle of 16% (see the Table 5.3).

Table 5.3: Operating condition.

Operating condition	Value
Input voltage	$80V_{DC}$
Load current	40A
Switching frequency	16 kHz
Duty Cycle	16 %

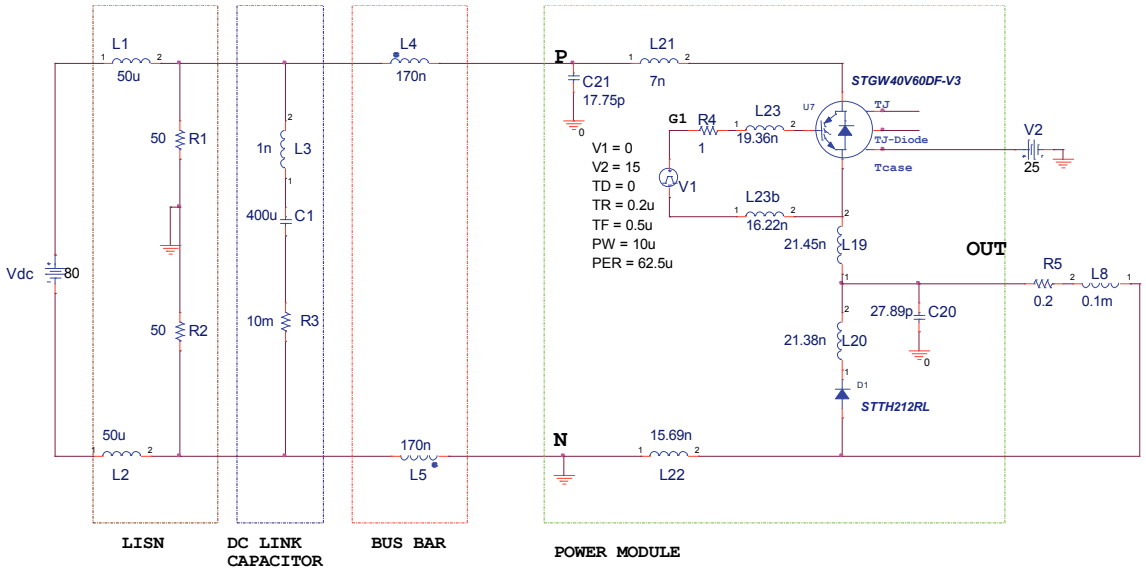


Fig. 5.9: Circuit considered for the simulation.

The first part is the LISN (Line Stabilisation Network) is inserted between the DC source and the power module for decoupling the noise from the circuit under evaluation and the main block of the module.

The second part conteins the equivalent circuit of the bulk capacitor with its parasitic element ESL and ESR (Equivalent Serial Inducatance and Equivalent Serial Resistance).

The tirth part represents the equivalent circuit of the bus bar used for the connections of the applied V_{DC} to the power module. This part is considered critical due to the noise generated by the presence of inductances of high value which depending on the layout connections and strongly influenced by the shape of the links, whose lengths are very difficult to minimize. A tipical optimized value of positive and negative bus inductance connections is 170 nH.

Finally the forth part includes the inner portion of the power module, with the internal parasitic elements.

As shown in the Fig. 5.9, to semplify the calculation it has been necessary to substitude the lower IGBT with an equivalent diode; this modification is correct because during the operation of the device it is maintained OFF, that is to say a DC-DC step down operation mode is considered. The analysis concerns the study of peaks output voltage of the IGBT during the commutations when the output is connected to an load impedence with 0.2 Ω resistence and an 0.1 mH inductance. The simulations are done considering three values of the Bus Bar inductances L_4 and L_5, wich takes the values 170 nH, 100 nH and 50 nH. To reduce the peaks overvoltage on the IGBT, was chosen a DC link voltage of 80 V, relatively low compared with the breakdown values of the device under examination (*STGW40V60DF)*. In this way it is possible to focalize the attention on the generated voltage peaks existing accross the collector and emitter of the IGBT and to avoid of working near the breackdown region. This aspect is very important for the reliability of the IGBT in the real-world applications because the overvoltage on the IGBT must be mainteined much lower than the maximum breakdown value. The simulation performed to calculate overvoltages applied to the device helps the designers to understand how is possible to optimize the involved parasitic elements.

Now are described the results of circuit simulations done:

- First simulations concern time domain;
- The second ones are in the frequency domain (*FFT*).

The critical parameters are identified and optimized to reduce electromagnetic emission. In the Fig. 5.10 and 5.11 are shown the circuit parasitic elements obtained by means Q3D Ex.

5.3.1 Time domain analysis

The simulation in the time domain permits to evalutate the overvoltage peaks across the device and to understand how is possible reduce then. The electromagnetic interferences are mainly related to dV/dt and thus, if the overvoltage are reduced, a great reduction of impact of the emissions is obtained.

In the Fig. 5.10 the circuit considered for the time domain analysis is shown.

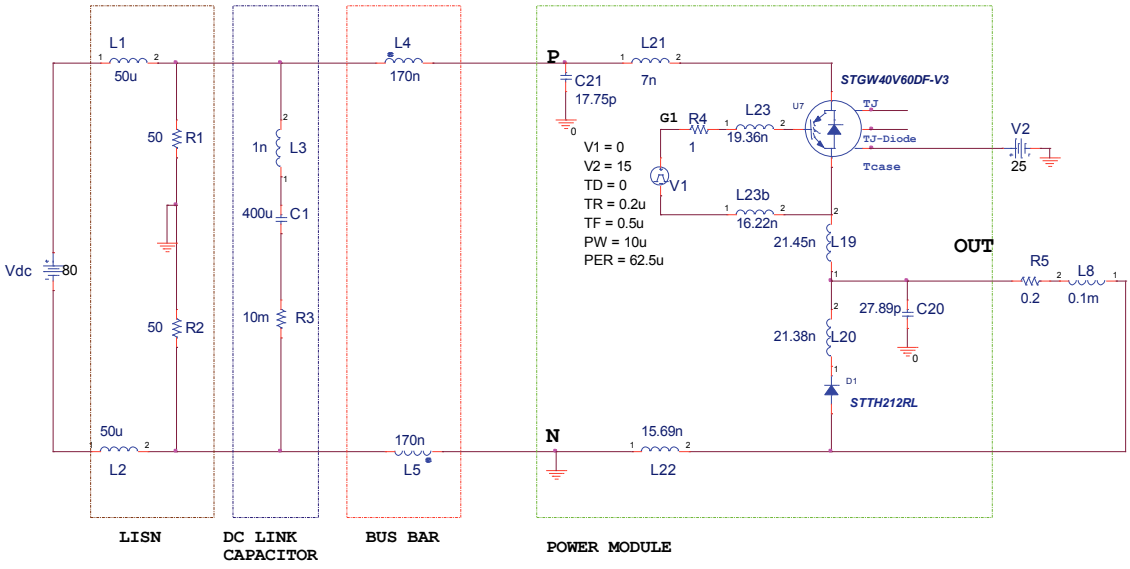


Fig. 5.10: The circuit schematic analysed for the time domain simulation.

In the Table 5.3 are given the values of the overvoltage obtained by the SPICE simulation for tree different Bus Bar inductance with an input voltage of 80V and a current of 40A.

5.4: List of results.

DC link voltage	Load current	Bus Bar inductance	Overshot voltage V_{CE}
80 V	40 A	170 nH	**745 V**
80 V	40 A	100 nH	**732 V**
80 V	40 A	50 nH	**627 V**

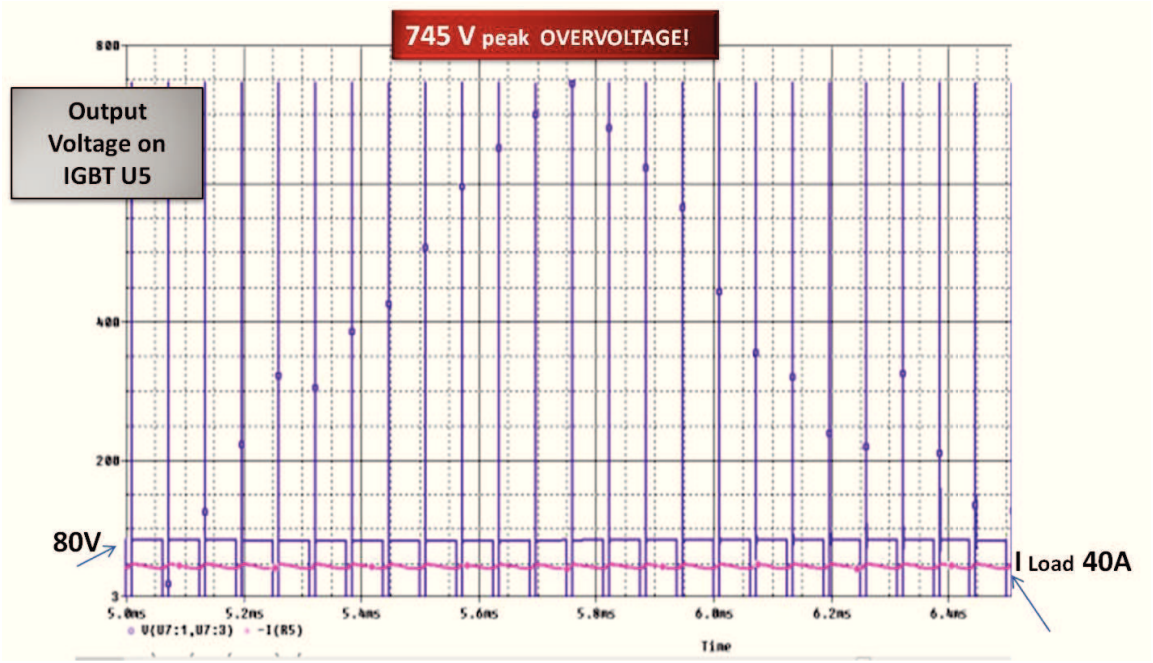


Fig. 5.11: SPICE simulation: the blue trace represent the Vce IGBT voltage and the red trace is the load current.

Since the module has a maximum permissible voltage about of 600 V and current capability of 40 A, it is very important to limit the unwanted peak overvoltage on the device to prevent damage and problems during the life time of the power devices. Decreasing only the Bus Bar inductance, an improvement the layout of the bar distribution is achieved, but this is not sufficient to limit the overvoltage spikes, in that

for 50 nH bus bar inductance a value of 627 V overvoltage is reached. This value is still too large for the device, and other actions are necessary. To reduce the peak, at the first, two capacities, C_2 and $C_3$was added, internal and external to the module respectively, in order to filter the effect of the bus bar inductance. For this purpose three cases have been considered as described in the following.

CASE I: C_2=10µF (low ESR and ESL type); C_3 = 1µF (low ESR and ESL type).

As highlighted in the Fig. 5.12, an internal 1µF capacitor C_3 is considered inside the power module and a local 10 µF capacitor C_2 is put near to V_{DC} link Pins (P and N) of the power module.

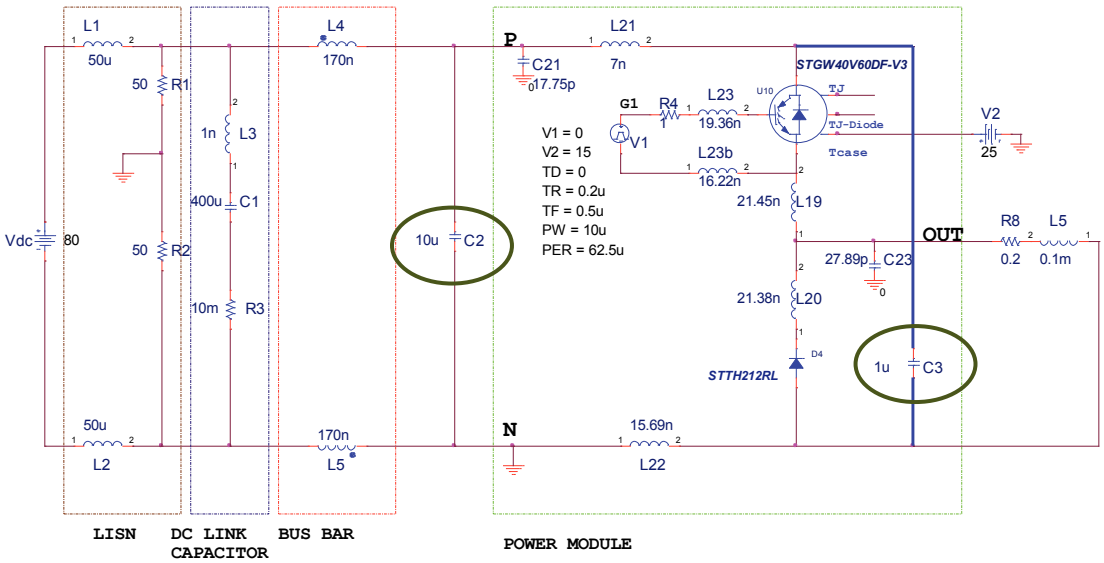


Fig. 5.12: Circuit for the simulation with C_2 and C_3 filter capacitors.

In the Table 5.5 the simulation results with the considered filter capacitors for different values of L_4 and L_5 bus bar inductance are given.

Table 5.5: List of results for the case I.

DC link voltage	Load current	Bus Bar inductance	Overshot voltage V_{CE}
80 V	40 A	170 nH	**328 V**
80 V	40 A	100 nH	**318 V**
80 V	40 A	50 Nh	**322 V**

The Fig. 5.13 shows the voltage and current for this case.

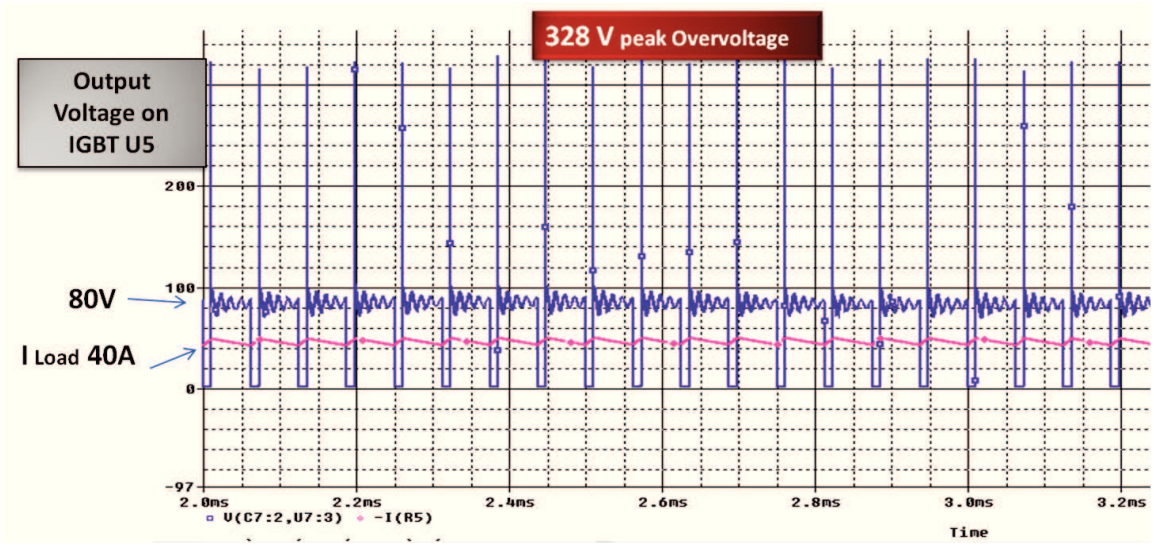


Fig. 5.13: Voltage and current for the case I.

As it can see we have a significant decreasing of the overvoltage spikes. There is a reduction of about 56% with respect to the circuit without capacitors; in fact, the overshot voltage is halved, as compared with the case to the case without C_2 and C_3, from 745 V to 328 V.

While reducing the inductance due to the current path of the Bus Bar, it is not possible further reducing the overvoltage peaks without an improvement within the module.

From a theoretical point of view, there is a margin to improve the configuration by increasing C_2 and C_3; however, this solution is not fully realizable because to the little space available inside the module.

Furthermore, other simulations carried out with increasing capacitance values don't lead to further spikes reduction. It's clear that further optimization should be sought by reducing the internal stray inductances. For this reason, we tried to reduce the inductance values of the module, L_{19} and L_{20}, assuming a value of 10 nH instead of 21 nH, leaving the two capacitance C_2 and C_3 as in previous case. As described in the case II, a better value peak spike is obtained.

CASE II: C_2=10µF (low ESR and ESL type); C_3 = 1µF (low ESR and ESL type); L_{19}=L_{20}=10 nH.

The Fig. 5.14 shows the simulation results of the second case, in which a reduced value of L_{19} and L_{20} wire bonding parasitic inductances has been considered (see Fig. 5.14).

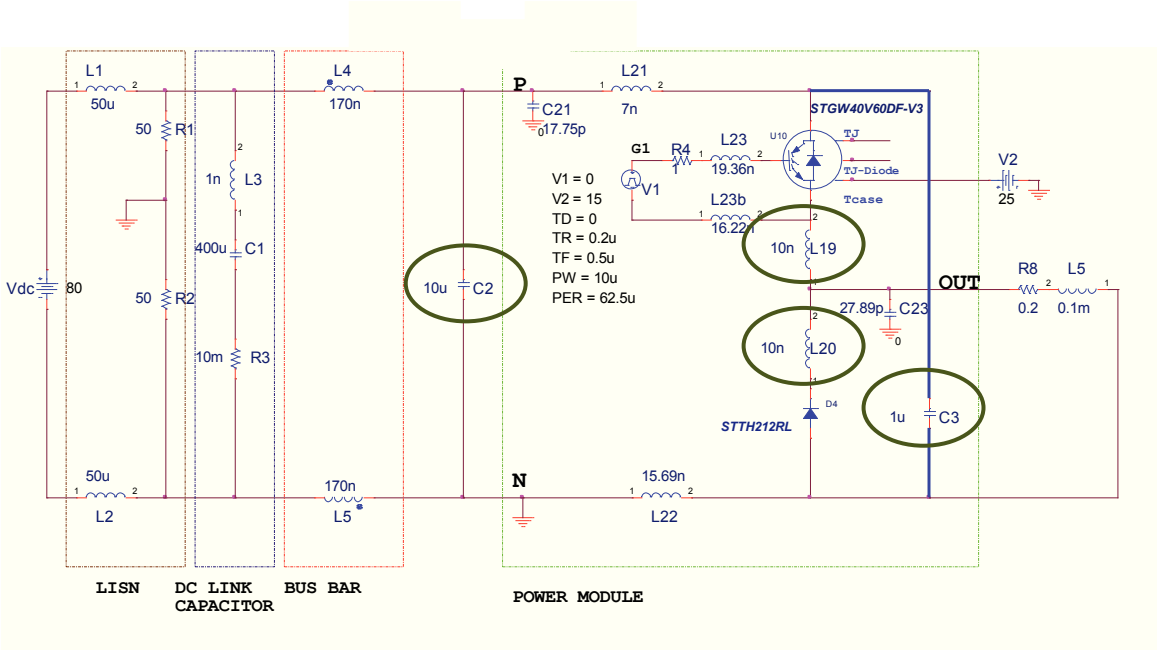


Fig. 5.14: Circuit with L_{19}=L_{20}=10 nH and C_2 and C_3.

Table 5.6: List of results for the case II.

DC link voltage	Load current	Bus Bar inductance	Overshot voltage V_{CE}
80 V	40 A	170 nH	**220 V**
80 V	40 A	100 nH	**226 V**
80 V	40 A	50 Nh	**224 V**

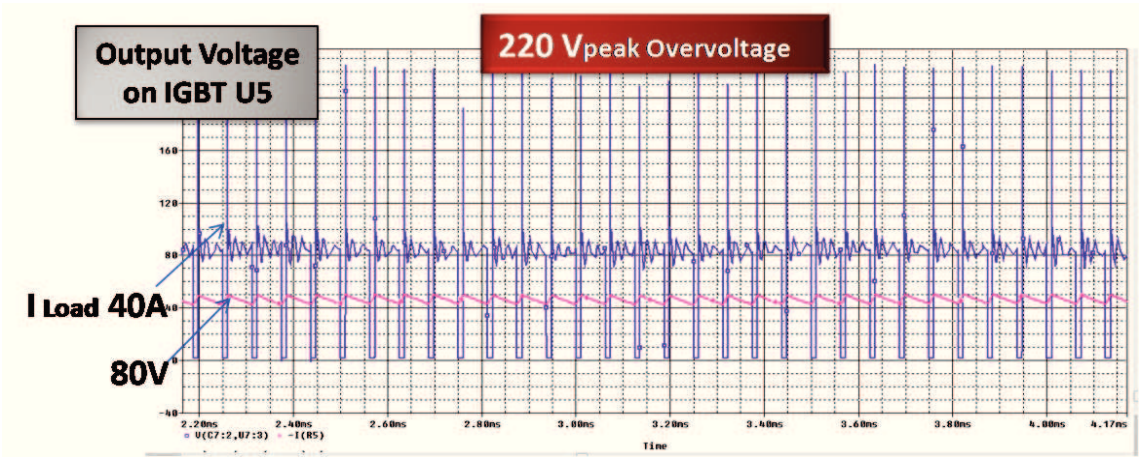


Fig.5.15: Voltage and current for the case II.

Also in this case we achieved a significant reduction of the overvoltage spike; in fact, it has dropped from 328 V to 220 V, which represents a 33% reduction with respect of the case I and 70% with respect to the circuit without capacitors.

CASE III: C_2=10µF (low ESR and ESL type); C_3 = 1µF (low ESR and ESL type); L_{19}=L_{20}=10 nH; L_{22}=7nH.

Finally, in the last case, the value of L_{22} was reduced to 7 nH, the same value of the L_{21} inductance.

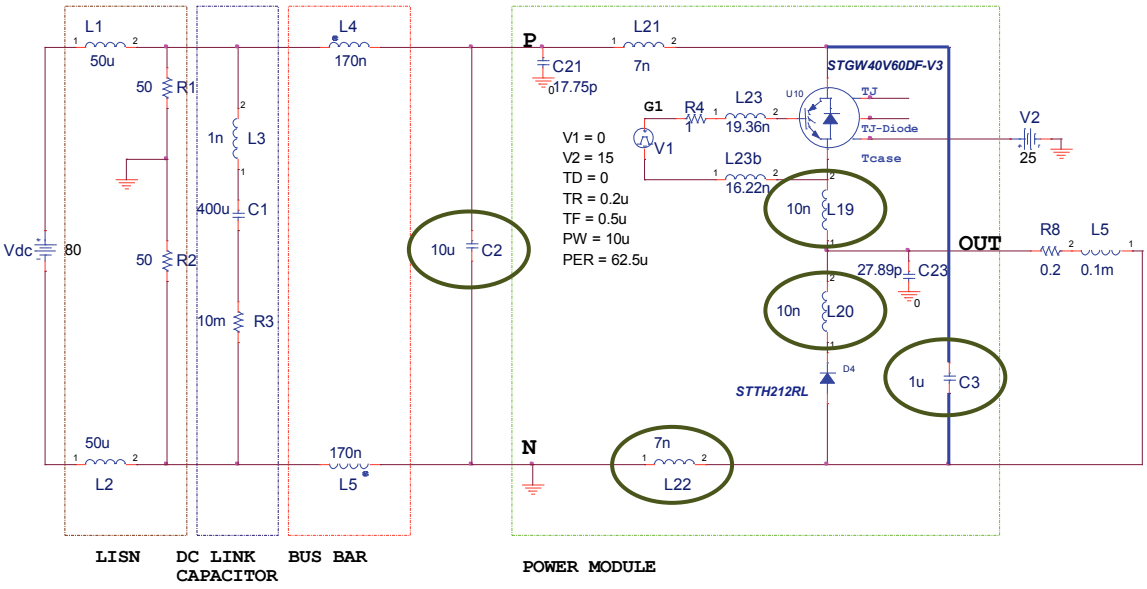


Fig.5.16: Circuit with L_{19}=L_{20}=10 nH, L_{22}= 7 nH and C_2 and C_3.

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Table 5.7: List of results in the case III.

DC link voltage	Load current	Bus Bar inductance	Overshot voltage V_{CE}
80 V	40 A	170 nh	**127 V**
80 V	40 A	100 nH	**126 V**
80 V	40 A	50 nH	**124 V**

A further improvement of the overvoltage has been reached, in percentage terms corresponding to an overall reduction of 83% with respect to the case of the not optimized power module. In absolute terms a 618 V peak reduction is obtained.

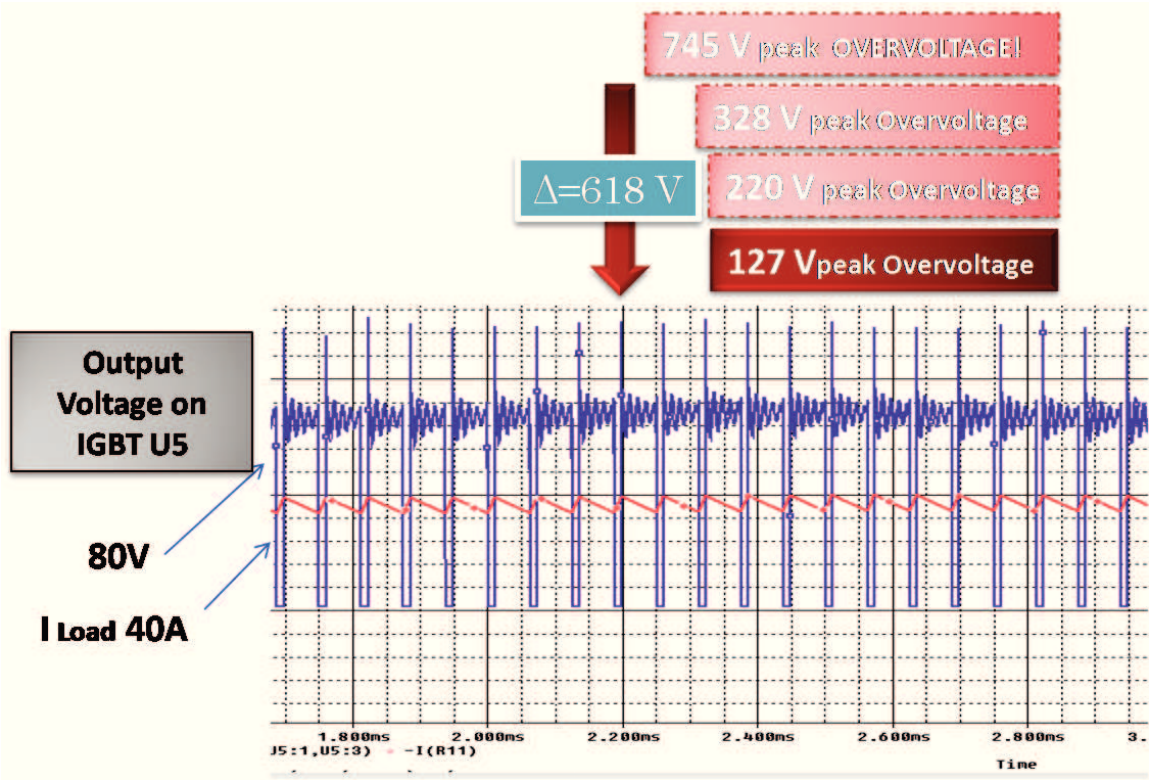

Fig.5.17: Voltage and current for the case III.

5.3.2 Frequency domain analysis

The time domain noise source has been transferred in the frequency domain and its partial element equivalent circuit is considered.

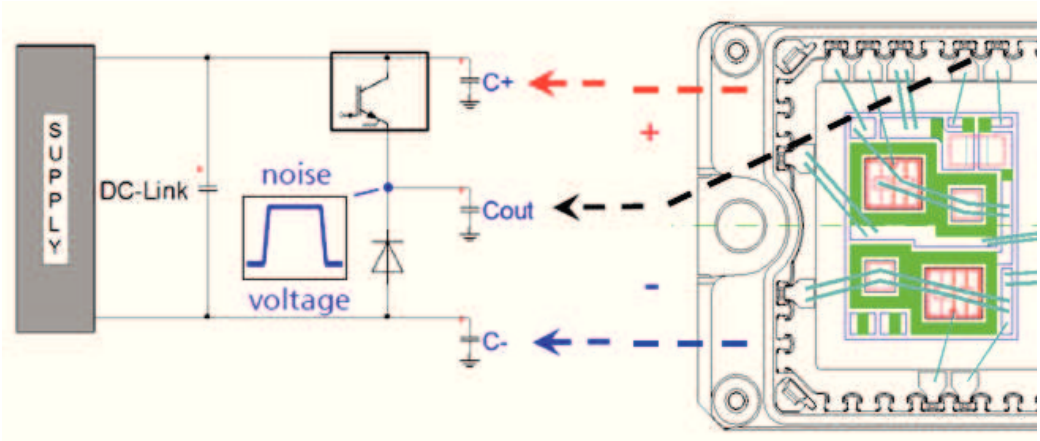

Fig.5.18: Principle schematics related to input V_{DC} link supply voltage, DC link capacitor and ground capacitors versus the GND base plate.

For the frequency domain analysis the IGBT switch has been substituted with a voltage source generating the same noise signal presents on the middle point of the inverter leg.

In the Fig. 5.19 are reported the waveform of time domain pulse and its frequency domain spectrum.

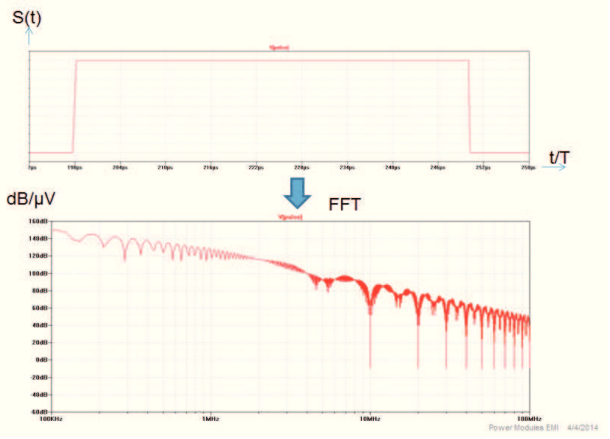

Fig.5.19: Time domain pulse and its frequency spectrum.

The V_{CE} voltage source is therefore considered as a square pulse, having a certain rise time and fall time, as it is in the reality (see Fig. 5.20).

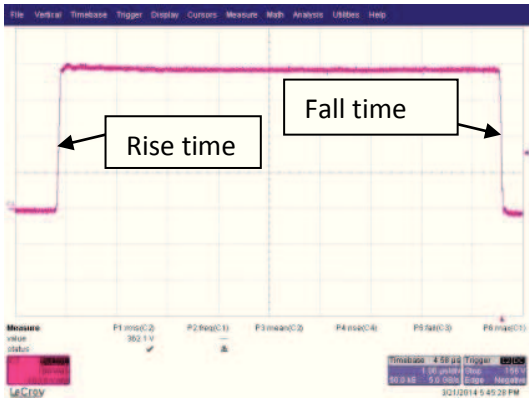

Fig. 5.20: A square waveform V_{CE} voltage source.

A 200 ns for the rise time and a 100 ns for the fall time is chosen. EMI behaviour of the power module as a source of interference is investigated up to frequency of 50 MHz. The analysis has been done considering the equivalent Q3d Ex. circuit of one leg. Some laboratory measurements performed directly on the prototype, have confirmed the values of the self-inductance and capacitance obtained by the Q3d Ex. The measured values are reported on the Table 5.8.

Table.5.8: Measure values.

Measured Values
C_{19}=19 Pf
C_{20}=6 pF
C_{out}=22 pF
L_5=7 nH
L_{19}=16 Nh
L_{28}=L_{23}=20 nH

Although the measured values are very close to calculated ones, which confirms roughly the calculation obtained, we will continue to use the values of parasitic elements by the Q3D Ex., because of the inevitable error we may have on the accuracy of the measure itself. In the Fig. 5.21 the not optimized module is presented.

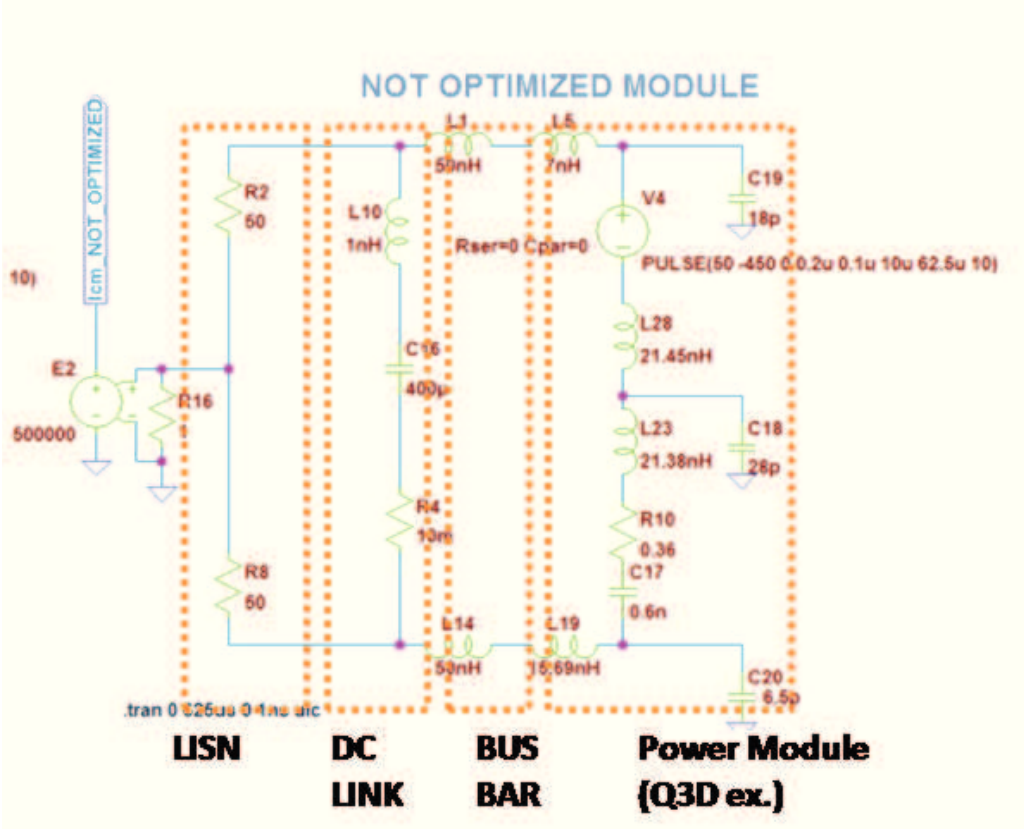

Fig.5.21: High Frequency equivalent circuit of the not optimized power module.

The common mode current of the not optimized module, shown in the Fig. 5.21, has been analyzed by means the FFT (Fast Fourier Transform) and the simulation results is reported on graphic of Fig. 5.24. The current peak reached the value of 60 dB/μV at 18 MHz.

In the second case considered, we have reduced the value of L_7 from 15.69 nH to 7 nH, the same value of L_3 in order to obtain balanced inductances.

In fact, during the design phase, it is possible to try of maintaining the symmetry of layout geometries and thus avoiding long trace or long wire bonding for the connections.

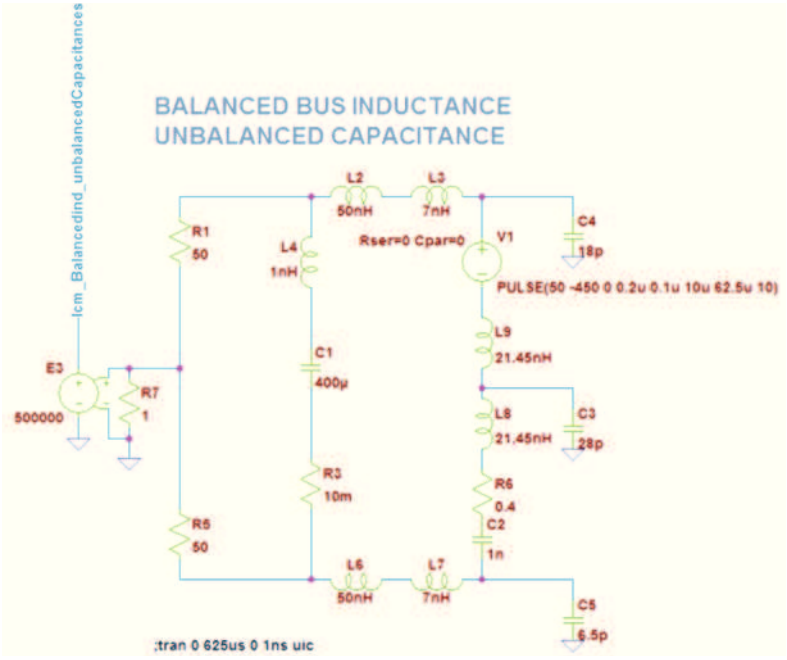

Fig. 5.22: Equivalent circuit of the power module with balanced bus inductance and unbalanced capacitance.

The FFT simulation in this case is represented with a pink waveform of Fig. 5.24.

We note a shift of the noise peak to the left of the diagram in the region of lower frequency, but the peak is still high, more than 60 dB/µV.

A better noise behavior is possible by decreasing the L_{26}, L_{27}, C_{13} values and by balancing C_{14} and C_{15}. The FFT results are shown in the Fig. 5.24 with green trace.

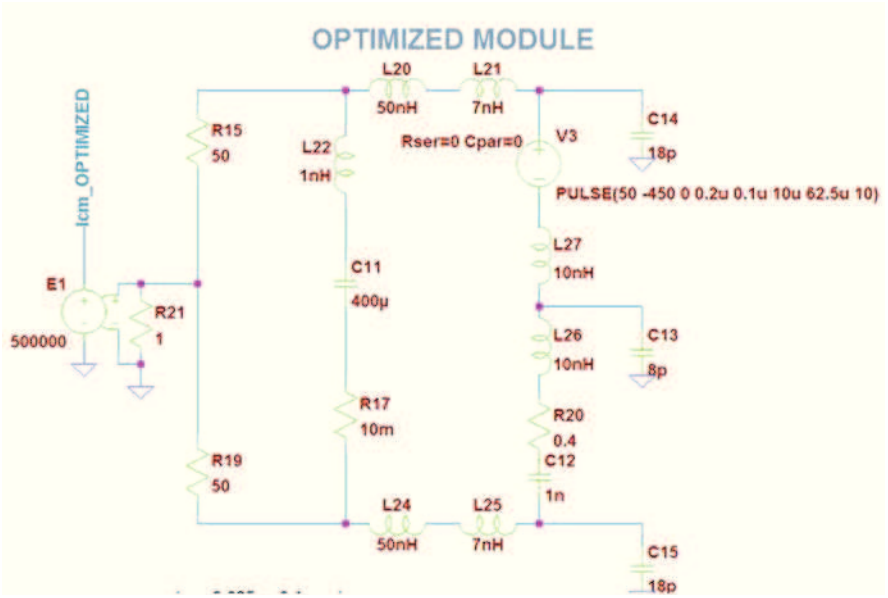

Fig. 5.23: Equivalent circuit of the power module with balanced bus inductance, reduced L_{27} and L_{26} and balanced capacitances.

In this case the simulation shows a noise reduction of 15-20 dB/µV of the peak noise and we note a considerable improvement of the overall noise.

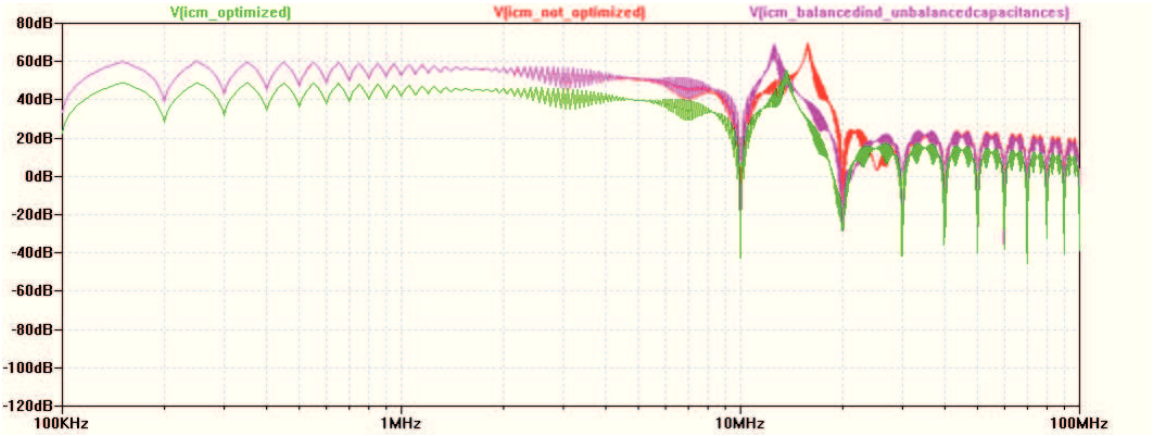

Fig. 5.24: Current common mode noise FFT spectrum of the three simulations for different parasitic element values. The red trace is the common mode current of the not optimized prototype; the pink trace represents the case of balanced inductances and unbalanced capacitances; the green trace refers the final optimization leading a considerable noise reduction of the overall noise.

Conclusion

In the thesis we carried out a theoretical investigation, supported by software tools, mainly aimed to analyse electromagnetic conducted emissions up to 50MHz generated in an electronic power module and to set up techniques for reducing significantly their unwanted effects. In this work we have made use of time and frequency domain analyses performed by the code PSpice on several RLCG electrical equivalent networks of a prototype of a power electronic module. These equivalent networks have been previously obtained by means of software Q3d Ex to model by lumped elements an electrical device having irregular geometrical shape and various and complex material components, as it is the prototype module under in consideration. In particular, this software has enabled us to compute values of the most critical parasitic inductances and capacitances of the module. In the real-world applications of the power electronic modules, a very important problem is to protect the active devices, typically IGBTs, against the spikes overvoltage, so increasing their life time. To discover how is possible to mitigate the overvoltage across the switches, three cases have been taking into account and simulated with PSpice. Best results are obtained using a capacitor of small value inside the power module and a 10 μF capacitor placed near the P and N nodes of the DC link connection, thus obtaining an overall overvoltage reduction of 83%. Successively, the frequency domain analyses performed have highlighted that the capacitance through the baseplate plays an important role as concerns the common mode current emissions. At this regard, the analyses carried out have showed both capacitances and inductances must be minimized and balanced to obtain a significant noise reduction of the common mode noise spectrum. In fact, an improvement of 15-20 dB/μV for the peak noise around 15 MHz is reached.

The analysis which has lead to the noise reduction may be useful to power module designers to reduce parasitic elements, to reach smaller conducted emissions, to simplify the filtering in the systems and of the power line. In this way a module of small dimension is obtained and it will be more competitive in the market.

It is believed that further investigations and developments of this present work could lead to set up an intelligent algorithm, intended to minimize the parasitic elements and to give some suggestions about layout and wire bonding module which are compatible with the design rules.

References

[1] B.K. Bose, *Power Electronics – a Technology Review*, Proceedings of the IEEE, Vol. 80, No 8 august 1992, pp 1303 – 1334;

[2] J.S. Chitode, *Power Electronic*, 4th ed., 2009;

[3] M. Nishihara, Power Electronics Diversity, Proceeding of the international Power Electronics Conference (Tokyo), 1990, Vol. 1 pp 21-28

[4] V. Jagannathan, *Power Electronics: Devices and Circuits*, 2nd ed., november 2010;

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 2nd ed., John Wiley & Sons, New York, 1995;

[6] T. L. Skvarenina, *The Power Electronics Handbook*, CRC Press LLC, 2000 N.W. Corporate Blvd;

[7] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, *Application Manual Power Semiconductor*, SEMIKRON International GmbH;

[8] B. W. Williams, *Power Electronics: Devices, Drivers and Applications*, John Wiley & Sons, NY, 1987;

[9] M. H. Rashid, *Power Electronics Handbook*, Academic Press, USA

[10] B. Joyant Baliga, *Power Semiconductor Devices*, PWS Publishing, New York, 1996

[11] Lorenz, Marz and Amann, *Rugged Power MOSFET—A milestone on the road to a simplified circuit engineering,* SIEMENS application Notes on S-FET Application, 2000.

[12] D. K. Schroder, *Advanced MOS Devices, Modular Series on Solid State Devices*, MA: Addison Wesley, 1987;

[13] L. Malesani, P Tenti, *Medium-frequency GTO inverter for induction heating applications*, Second European Conference on Power Electronics and Applications: EPE. Proceedings, Grenoble France; 22–24 Sept. 1987, Vol. 1, pp. 271–276;

[14] T. L. Skvarenina, *The Power Electronics Handbook Industrial Electronics Series*, CRC Press LLC, 2000 N.W. Corporate Blvd;

[15] V. K. Khanna, "*Insulated Gate Bipolar Transistor (IGBT): Theory and Design*" IEEE Press, Wiley-Interscience;

[16] Clayton R. Paul, 1995, *Introduction to Electromagnetic Compatibility*, John Wiley

[17] H. V. Ott, *Electromagnetic Compatibility Engineering*

[18] Pubblicazione IEC 50 (161), International Electrotechnical Vocabulary (IEV) Chapter 161: Electromagnetic Compatibility

[19] Xun Liu, C.K. Lee, S.Y. Hui, *"An Integrated Planar EMI Filter for Ultra-high Frequency Power Converters"*, Power Electronics Specialists Conference, 2007. IEEE 17-21 June 2007 Page(s):1528 – 1534.

[20] http://www.powerguru.org/new-alternative-materials-and-concepts-for-power-electronics/

[21] high power IPMs Simplify Design rivista

[22] Emerald, P.; Greenland, Power Multi-Chip Modules", PCIM Europe, Sep./Oct. 1995, pp. 242-246

[23] M. Mermet - Guyennet, *New structure of power integrated module*

[24] G. Aiello, S. Alfonzetti, E. Dilettoso, N. Salerno, "*An Iterative Solution to FEMBEM Algebraic Systems for Open-Boundary Electrostatic Problems*", IEEE Transactions on Magnetics, vol. 43, n. 4, April, 2007, pp. 1249-1252.

[25] G. Aiello, S. Alfonzetti, G. Borzì, N. Salerno, "*An improved solution scheme for open-boundary skin effect problems*", IEEE Transactions on Magnetics, vol. 37,n. 5, september, 2001, pp. 3474-3477.

[26] A. F. Peterson, S. L. Ray, and R. Mittra, *Computational Methods for Electromagnetics.* IEEE Press, New York, USA, 1998.

[27] A. Lidow, *Power Conversion: The End of the Road for Silicon*