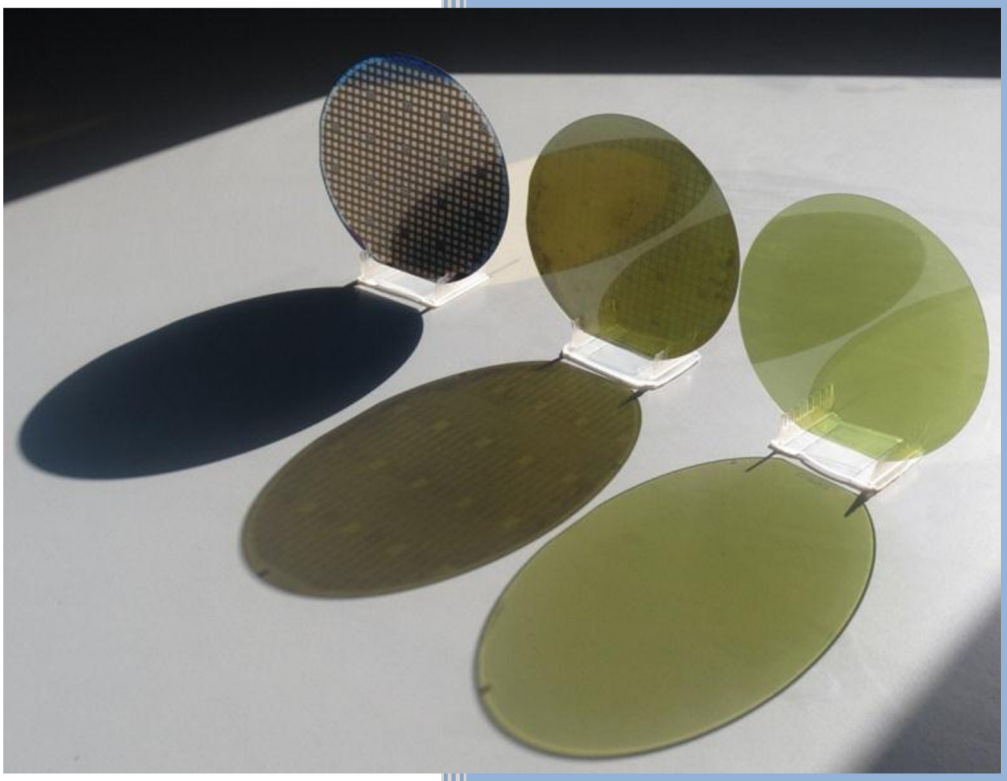
Universita' degli Studi di Catania
Scuola Superiore di Catania

International PhD
in Energy

XXVI cycle

Alessia Maria Frazzetto

Advanced processes for next generation energy efficient MOSFETs in Silicon Carbide



Tutor: ***Prof. Ing. M. Cacciato***

Scientific Tutors: ***Dott. F. Roccaforte***
Dott. M. Saggio

2014

Universita' degli Studi di Catania
Scuola Superiore di Catania

International PhD in Energy
XXVI cycle

Alessia Maria Frazzetto

Advanced processes for next generation energy efficient MOSFETs in Silicon Carbide

Tutor: ***Prof. Ing. M. Cacciato***

Scientific Tutors: ***Dott. F. Roccaforte***
Dott. M. Saggio

2014

Abstract

In the modern society, the reduction of the energy consumption through its efficient use has become one of the main task of power electronics. In this context, Silicon Carbide (SiC) exhibits interesting electrical and physical properties which can satisfy the continuous demands of improved energy efficiency, overcoming the limitations of Silicon. Today several SiC technologies have reached the industrial maturity. In this thesis, different aspects and challenges related to the fabrication of 4H-SiC MOSFETs (which are among the most appealing devices due to their driving simplicity) have been treated. Indeed, in spite of remarkable and recent progress, several scientific aspects still need to be dealt for reducing the energy dissipation and to overcome the issues still open. In particular, the aim of this thesis has been to clarify the mechanisms ruling the transport properties at the interfaces metal/SiC and SiO_2/SiC. Special focus was given to the study of the mechanisms limiting the channel mobility in lateral MOSFET. All the achievements and progresses obtained have been integrated in a power MOSFET device, whose behaviour has corroborated the great potential of the material.

Riassunto

Nella società moderna la riduzione del consumo di energia attraverso un suo uso efficiente è diventato il compito principale della elettronica di potenza. In questo contesto, il carburo di silicio (SiC) presenta interessanti proprietà fisiche ed elettriche che permettono di soddisfare le continue esigenze di miglioramento dell'efficienza energetica e di superare i limiti del silicio. Oggi diverse tecnologie in SiC hanno raggiunto una maturità industriale. In questa tesi sono stati affrontati diversi aspetti e problemi relativi alla fabbricazione di dispositivi MOSFET in 4H-SiC (che sono tra i dispositivi più interessanti a causa della loro semplicità di pilotaggio). Infatti, nonostante i notevoli recenti progressi, ancora numerose sfide scientifiche devono essere affrontate per ridurre la dissipazione di energia e superare le questioni ancora aperte. In particolare, lo scopo di questa tesi è stato quello di chiarire i meccanismi che regolano le proprietà di trasporto alle interfacce metallo/SiC e SiO_2/SiC. Un'attenzione particolare è stata dedicata allo studio dei meccanismi che limitano la mobilità di canale nei MOSFET laterali. Tutti i risultati e i progressi ottenuti sono stati integrati in un dispositivo MOSFET di potenza il cui comportamento ha confermato il grande potenziale del materiale.

The science of today is the
technology of tomorrow
-Edward Teller-

Contents

Acknowledgements

It is anything but easy thank all the people who contributed to my personal and professional development during my Ph.D. studies.

First of all, I extend my deepest thanks to Dr. Fabrizio Roccaforte for his guidance and for his scientific suggestions during my doctoral study. I will ever be grateful to him to have me allowed to achieve important goal. I also owe Dr. Mario Saggio many thanks for his great assistance and encouragements during the PhD years and the ST work.

More than anyone else, I want to thank Dr. Vito Raineri, unfortunately no longer with us, for the opportunity he gave me to work on various challenging and interesting areas.

I should never finished this work without the precious help and daily support of Dr. Alfio Guarnera from ST: endless thanks.

Big thanks go out also to Prof. Mario Cacciato from the University of Catania, tutor of the thesis for his comprehension whenever I requested something from him.

Of course, another profound thanks is for all people of the CNR-IMM, who have contributed to this work of thesis. In particular, I thank: Dr. Filippo Giannazzo for his precious discussions and valuable contributions in the AFM analysis; Dr. Raffaella Lo Nigro for her exquisite scientific discussions and the interpretation of XRD analysis; Dr. Patrick Fiorenza for his encourages during the CNR-IMM years. I want also to thank Salvo Di Franco for his valuable support during the devices processing in the CNR-IMM clean room. Finally, special thanks to Corrado Bongiorno and Salvo Pannitteri for the useful TEM analysis and discussions.

I am indebted to my colleagues at STMicroelectronics for providing a stimulating environment in which to learn and grow. I especially grateful to Simone Rascunà, Edoardo Zanetti, Dario Salinas and Leonardo Fragapane. Every one of them have had an important role in this adventure.

Thank you to all friends, who accompanied me in this experience and shared with me the “box 2” during the CNR-IMM years: Giuseppe Greco, Carmelo Vecchio, Jens Eriksson and Sushant Sonde.

I would like also to thank all the people who assisted and believed me in this years. A special acknowledgment is due to my parents Lino e Cetty who always encouraged me in my studies and learned to live. A particular acknowledgment is due to my sisters, Simona and Ilaria, and my brother, Fausto to make special every instant of my life. Finally, a lovely acknowledgment is dedicated to my husband Andrea, who made this thesis possible by his support and unrivalled Love.

Thank you everyone

Alessia

Introduction

We live in an energy-hungry world in which industrialization and globalization have accelerated the demand for resources that now doubles approximately every 40 years. *Microelectronics* research activity has grown with a nearly exponential rate. In parallel to the advent of the continuous progresses leading to the miniaturizing of the devices and integrated circuits, the reduction of the energy consumption through its efficient use is the main task of modern power electronics. The increasing dependence of power electronics in modern society has motivated great advances in power electronics technology. These advances are significantly dependent on performance enhancements of power devices that have been widely used in power generation and power distribution. Three driving forces make reducing energy losses a major priority. The first is the Kyoto Protocol that sets binding obligations on industrialized countries to reduce emissions of greenhouse gases. The second is the rising cost of energy, which incites everyone to cut down on its use. The third driving force is the fact that the majority of the world's energy comes from hydro-carbons and only 15% from renewable energy.

In the last six decades Silicon (Si) technology has always dominated the power electronic field, providing semiconductor devices able to operate in a broad spectrum of power levels and frequencies. Due to the inherent limitations of Silicon material properties, such as narrow bandgap, low thermal conductivity and low critical electric field, Silicon power devices are approaching theoretical limits in terms of higher power and higher temperature operations, offering no significant improvement in device performances with further investment.

Hence this material is no longer suitable for modern power electronics application [1,2]. The demand for improved energy efficiency in power electronics, which can be satisfied by reducing the switching and conduction losses of devices, as well as for devices capable of high temperature operation, is pushing the power electronics technology development toward *wide band gap* (WBG) semiconductors. In this context, Silicon carbide (SiC), gallium nitride (GaN), exhibit interesting electrical and physical properties that can satisfy the continuous demands of improved energy efficiency. SiC has been recognized, among all the WBG materials, as a good candidate for replacing

silicon [3] in certain power device applications [4]. First of all, SiC has a great advantage over competing compound semiconductors in the fact that, like silicon, it has silicon dioxide (SiO_2) as its native oxide. Moreover, thanks to the commercial availability of large size SiC wafers accompanied by an improvement in the quality of substrates (micropipes reduction) [5] and to the achievement of a high level of maturity in manufacturing processes, several SiC technologies, operating at different voltages (600V and 1200V), have reached the industrial maturity [6,7,8,9]. SiC switches available in the market are *junction field effect transistors* (JFETs), *barrier junction transistors* (BJTs) and *metal-oxide-semiconductor field effect transistors* (MOSFETs). The MOSFET is the most promising technology, due to its driving simplicity and market appeal.

SiC-based electronic devices can work at higher temperature, higher power and higher frequency and in environments harsher than the current traditional semiconductor technology may afford. Therefore, the potential applications of SiC-based electronic devices nowadays include aerospace (high temperature engines, radiation hard devices), transportation (power supply, power switching and power module) as well as industry (power supply), communications (radio frequency (RF) switching) and renewable energies (e.g., power conversion in solar and photovoltaic plants) [10].

The advantages of SiC over Si based power devices can be summarized as follows:

- SiC unipolar devices are thinner, and they have lower on-resistances, which results in lower conduction losses and higher overall efficiency.
- SiC based power devices have higher breakdown voltages because of their higher critical breakdown electric field.
- SiC has higher thermal conductivity (4.9 W/cmK for SiC and 1.5 W/cmK for Si), meaning that SiC power devices have a lower thermal resistance; hence the device heating rate is slower, also enabling size reduction in the cooling systems of power applications, according with application specifics.
- SiC can operate at higher temperatures (up to 600°C compared to 150°C for Si).

- SiC is extremely radiation hard and therefore suited for aerospace applications, by decreasing the additional weight of radiation shielding.
- Because of low switching losses, SiC based devices can operate at high frequencies (> 20 kHz) which are not reachable with Si based devices for power levels higher than a few kilowatts.

Among all the large number of polytypes of SiC (cubic, hexagonal or rhombic), the more mature and better studied is the hexagonal polytype 4H-SiC. Indeed, the wide bandgap of 4H-SiC allows power devices to function at high junction temperatures such that they can operate at higher current densities without violating the power dissipation limit [11]. Moreover, thanks to its critical electric field, which determines the material's breakdown strength, 4H-SiC devices allow a significant reduction of device specific on-resistance [12]. Therefore, 4H-SiC is an ideal material for high power and high temperature applications.

SiC MOSFET can be used in various challenging applications such as solar inverters, high voltage power supplies, wind plant stations, and electric vehicles. It is expected that, together with high voltage SiC Schottky Barrier Diodes, the 4H-SiC MOSFET can play an important role in designing high power switching circuits and systems.

In spite of remarkable and recent progress in the fabrication of 4H-SiC devices, still several scientific challenges need to be treated to reduce the energy dissipation and so to improve the efficiency of the devices. In particular, the still existing lack of knowledge of the physical properties of the material determines unclear transport mechanisms at the interface metal/semiconductor or insulated/semiconductor. There are still several scientific open issues related to the basic transport properties at SiC interfaces that can affect the device performance, keeping them from reaching their theoretical limits. These aspects cannot be regarded as secondary objectives. Hence, the research work on power 4H-SiC MOSFET focuses not only on the development of innovative device structures, but also on the study of processing techniques able to overcame these issues and hence to improve on-resistance, blocking capability and switching time of the devices.

In this context the research activity of this thesis is focused first of all on the formation of good Ohmic contacts on the implanted p-type SiC to obtain high frequency and high power performance MOSFET devices [13]. In fact, a contact resistance that is

significantly higher compared to the on-resistance of the device leads to a voltage drop at the metal-semiconductor interface, in turn resulting in decreased efficiency due to added resistive losses [14].

The second aspect handled in this research activity concerns the investigation of channel mobility in the implanted region and the limiting mechanism at the interface SiO_2/SiC. Indeed, the fundamental blocking point to realize the 4H-SiC power MOSFETs is to obtain a device with a total on-resistance comparable with the theoretical prediction. The high total on-resistance observed in the power device is associated with not optimized channel resistance component. Indeed, the high channel resistance has been influenced by a low channel mobility. The poor interface quality between SiC and SiO_2 results in large amounts of interface surface states and low inversion layer mobility. The low channel mobility is the major limiting factor for realizing efficient MOS gated power devices. Many approaches to improve the channel mobility have been conducted for many years including different post oxidation annealing (NO or N_2O) [15], and today the practical channel mobility with achievable current technologies is in the range of ~30-50 $cm^2/V \cdot s$ [16].

Nevertheless, the future of this material seems to be bright and the 4H-SiC MOSFET devices can be used in applications that require fast, efficient switching.

The dissertation is divided into five main chapters.

In *chapter 1*, a general introduction on silicon carbide is presented, providing an overview of the most important physical and electrical properties of SiC materials, as a semiconductor for power electronic devices. Then, the advantages of 4H-SiC as a material, which offers intrinsically the best performance in terms of breakdown voltage, switching frequency and system efficiency, have been also briefly highlighted. Therefore, the chapter concludes with the current status and future research on this material with regards to both fundamental issues and processing technologies.

In *chapter 2*, after brief summary of the main power applications of SiC devices, the benefits of using the SiC MOSFET with respect to the conventional Si MOSFET or Si IGBT in terms of the switching losses and power performances are shown. Hence, the fundamental Figures of Merit for energy efficient power SiC devices are compared with the figures of merit of Si devices. In particular, thanks to the physical properties of the material, SiC exhibits a better trade-off between the breakdown voltage and on-resistance in conduction, which allows to obtain a substantial reduction of power losses

and an improvement of the power efficiency of the MOSFETs devices. The working mechanisms and output characteristics of a basic power MOSFET have been described. Finally, the technological and scientific issues for SiC MOSFTEs (ohmic contacts, channel mobility, etc.) are briefly described.

In the *chapter 3*, the morphological and electrical properties of Ohmic contacts fabricated on p-type implanted 4H-SiC using annealed Ti/Al layers were studied. After a brief summary of the state of art of the ohmic contacts on the implanted p-type region and metal-semiconductor theory, the influence of a different morphology and microstructure of Al-implanted 4H-SiC, resulting from different high temperature annealing conditions, on the electrical and structural properties of Ti/Al Ohmic contacts, was discussed. To evaluate the effect of these different annealing conditions on the properties of the Ti/Al Ohmic contacts, several morphological, structural and electrical characterization techniques were employed in this study. Atomic Force Microscopy (AFM) was carried out for the morphological analysis, before of the implantation processes, subjected at different annealing conditions for the activation of the dopant. Afterward, the same analysis was performed on the alloyed Ti/Al Ohmic contacts. The surface of the implanted regions influences the roughness of the Ohmic contacts. The experimental approach included also the macroscopic electrical measurements conducted on the Transmission Line Model (TLM) structures. In particular, by the TLM theory the specific contact resistances, ρ_c, was extracted. By the electrical analysis a lower ρ_c has been observed in the sample processed with a protective carbon capping layer during the high temperature activation annealing of the dopant. The temperature dependence of the ρ_c was also studied and enabled the extraction of the barrier height in two cases. The electrical results were correlated with the microstructural analysis of the interface region carried out by the Transmission Electron Microscopy (TEM) and X-ray Diffraction (XRD).

In *chapter 4*, the mechanisms limiting the channel mobility were studied on lateral MOSFETs. In particular, the mobility behavior was investigated for devices fabricated using two different post-implantation annealing (with and without a protective capping layer) and different values of the channel mobility have been measured. Moreover, the temperature dependence of the channel mobility showed that the Coulomb scattering is the main limiting mechanism to the electron transport in the channel.

The electrical analyses were correlated with the microstructural investigations of the interface region SiO_2/4H-SiC. To validate this approach, a direct measurement of the density traps at the interface (D_{it}) has been performed on the MOS structures, fabricated with the same flow of the lateral MOSFET. Moreover, the temperature dependence of the threshold voltage has been evaluated and different behaviours, in both samples analysed, have been observed with respect to the theoretical prediction.

To complete this study an alternative approach to increase the channel mobility has been investigated: a post oxidation annealing in phosphorus oxychloride ($POCl_3$) ambient. Using $POCl_3$ annealing, a huge channel mobility (~108 $cm^2V^{-1}s^{-1}$) and a lower D_{it} ($5.7x10^{11}$ $eV^{-1}cm^{-2}$) have been measured in the lateral MOSFETs with respect to the structures subjected to N_2O annealing. In spite of this advantage, by C-V measurements, an instability of the electrical behaviour of the MOS capacitors has been observed and an "unstable" threshold voltage under stress has been observed using $POCl_3$ in the MOSFETs device. Hence, an optimal compromise between the channel mobility and the oxide reliability can be identified to realize a power device using the N_2O processes annealing.

Finally, in the *chapter 5* all the results of this study have been implemented in a 4H-SiC power MOSFET device. An overview of the main behaviours of 4H-SiC vertical power MOSFET (VMOS), fabricated in STMicroelectronics front end line site of Catania (Italy), is shown. In particular, a preliminary static and dynamic characterization of 4H-SiC power MOSFET has been provided and compared with the behaviour of Si devices and of other SiC devices commercially available.

The results that have come out from this thesis can of course also be extended to a broader and more general area of interest.

The research activity presented in this thesis was carried out in a collaboration with University of Catania, the CNR-IMM in Catania and ST Microelectronics of Catania. In particular, the fabrication processes and characterization of the devices have been performed partly in STM equipment and partly in CNR-IMM laboratories and clean room.

References

[1] J. Millman and C.C. Halkias, *Electronic Devices and Circuits*, Tata McGraw-Hill Publishing Company Ltd., New Delhi, (1991).

[2] J. Millàn, *IET Circuits Devices System* .**1**, 372 (2007).

[3] K. Shenai, R. S. Scott, and B. J. Baliga, *Optimum Semiconductors for High-Power Electronics*, IEEE Trans. Electron Devices, **36** (9), 1811–1823, (1989).

[4] P. Chow, N. Ramungul, and M. Ghezzo, *Proc. High Temperature Electronic Materials, Devices, and Sensors Conference*, San Diego, U.S.A, (1998).

[5] J.W. Palmour, R. Singh, R.C. Glass, O. Kordina, Jr. Carter, CH. IEEE International Symposium on Power Semiconductopr Devices and IC'S, ISPSD, Weimar, Germany, p.25 (1997).

[6] www.cree.com

[7] www.st.com

[8] www.rohm.com

[9] www.infineon.com

[10] P. Tobias, A. Baranzahi, A. L. Spetz, O. Kordina, E. Janzen, and I. Lundström, IEEE Electron. Device Lett. vol. 18, pp. 287, 1997.

[11] P. G. Neudeck, J. B. Petit, and C. S. Salupo, *Silicon Carbide buried-gate junction field effect transistors for high temperature power electronic applications*, in Proc. 2nd Int. High Temperature Electronic Conf., 23-28 (1994).

[12] B. Jayant Baliga, Chap. 3, Section 3.3, pp. 100-101, *Fundamentals of Power Semiconductor Devices, Springer*, (2008).

[13] F. Roccaforte, F. La Via, V. Raineri, *International Journal of High Speed Electronics and Systems*, **15 (4)**, 781-820 (2005).

[14] G. Pensl, F. Ciobanu, T. Frank, M. Krieger, S. Reshanov, F. Schmid, M. Weidner, *SiC Materials and Devices*, **vol. 1**, 1 – 41, M. Shur, S. Rumyantesev and M. Levinshtein eds, World Scientific, Singapore, (2006).

[15] S.-H. Ryu, S. Dhar, S. Haney, A. Agarwal, A. Lelis, B. Geil, C. Scozzie, *Mater. Sci. Forum* **615-617**, 743 (2009).

[16] Y. Wang, T. Khan, M.K. Balasubramanian, H. Naik, W. Wang and T. Paul Chow, *IEEE Trans. Electron Devices*, **55(8)**, 2046 (2008).

Chapter 1
Properties of SiC

For several years Silicon has been the material that has dominated the electronics industry. However, silicon devices are reaching their physical limits associated to the narrow bandgap, low thermal conductivity and low critical electric field and will not be able to improve further. For overcoming the problem, which will make the conventional semiconductors inapt for potential demands, especially in high power and high efficiency applications, manufacturers are exploring the possibilities of using a worthy substitute. The favorite candidates to fulfill the demands of future power electronics devices are surely the wide band gap (WBG) semiconductors, like Gallium Nitride (GaN) and Silicon Carbide (SiC). In particular, compared to Silicon, SiC exhibits largely better properties for most of the key specifications, such as a higher energy gap, a higher critical electric field, a higher electron mobility and melting point, offering intrinsically better performance in terms of breakdown voltage, switching frequency and system efficiency. Thus, due to its unique electrical and chemical properties, this innovative material is becoming very attractive into the electronics field.
The first chapter of this thesis reviews some of the most important physical properties of SiC materials. The current status and future research on this material are also briefly highlighted with regards to both fundamental issues and processing technologies.

1.1 Structural properties and polytypes of SiC

The common semiconductors occur in the diamond crystal structure (Si and Ge), the zincoblende crystal structure and the wurtzite crystal structure (for example, GaAs and other III-V compound semiconductors) even though there is a large number of different crystal structures possible in nature [1].
SiC is the most stable compound of carbon (C) and silicon (Si) among those belonging to IV group of periodic table, with a partially ionic (12%) – covalent (88%) bond between C and Si atoms [2, 3]. The fundamental basic structural unit is a tetrahedron, shown in *Figure 1.1*, with four atoms of Si (C) and one atom of C (Si) at the center with

a binding energy of 5eV. SiC occurs in nature with different stable crystal structures having the same chemical composition (50% of Si and 50% of C). The different crystal structures, called *polytypes*, have equal basic tetrahedral structure, formed by four atoms of Si (or C) linked to a C atom (or Si).

The distance *a* between adjacent Si and C atoms is near to 3.08 Å [4]; the C atom is located at mass centre of the tetrahedral structure, to keep an equidistance among neighboring Si atoms of about

$$a\sqrt{\frac{3}{8}} = 1.89\text{Å} \qquad \textbf{(1.1)}$$

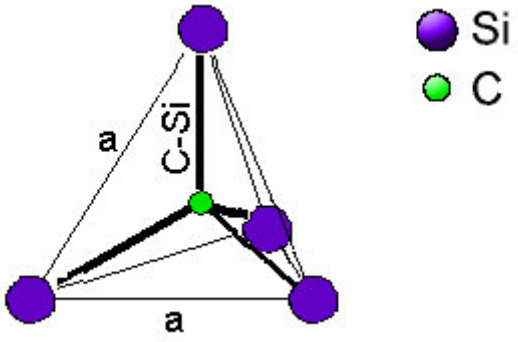


Figure 1. 1: *SiC basic tetrahedral structure*

The height of the cell *c* changes among the *polytypes*: in particular, the *c/a* ratio is 1.641, 3.271 e 4.908, for different *polytypes* 2H-, 4H- and 6H-SiC, respectively.

The fundamental structural characteristic of SiC is the polymorphism [5], that describes the phenomenon of the same material crystallizing in different modifications.

Over 200 SiC *polytypes* exist. The existence of different crystalline modifications of SiC was discovered in 1912 [6].

There are a large number of SiC polytypes which are characterized by the stacking sequence of the tetrahedrally bonded Si-C bilayers. While the individual bond lengths and local atomic environments are nearly identical, the overall symmetry of the crystal is determined by the stacking periodicity. Among all the polytypes, 3C-, 4H-, and 6H-SiC are the most common sequences available today and the ones used in the electronic

field. Each SiC polytype shares the same chemical composition but exhibits different electrical, optical, and thermal properties due to differences in stacking sequence.
The atomic planes of the lattice structure may overlap in three different provisions that are commonly indicated with the notation ABC. The different sequences of overlapping of planes distinguish the various polytypes. The stacking sequence ABC along the c axis gives rise to a cubic structure (zincoblenda); this is the only cubic structure in SiC and corresponds to the polytype 3C-SiC, also called β-SiC. The sequences of the type ABCB plans and ABCACB correspond to the 4H-SiC and 6H-SiC, also known as α-SiC: these structures have a different periodicity 4 and 6 and a hexagonal structure (H). A schematic view of different stacking sequence for some common SiC polytypes is presented in *Figure 1.2*. In particular, in the *Figure 2(a)* the stacking sequence of 3C-SiC is reported, while the staking sequence of 4H-SiC and 6H-SiC are showed in the *Figures 2(b)* and *2(c)*, respectively. The number in the notation refers to the number of layers before the sequence repeats itself [7].

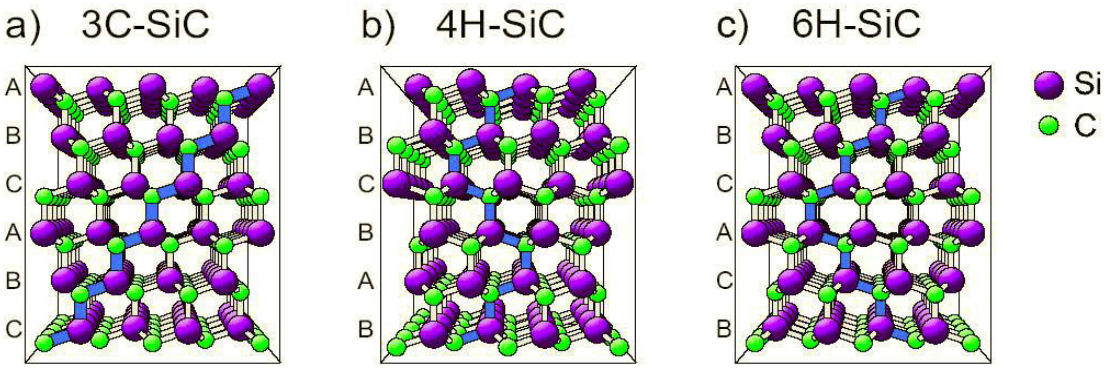


Figure 1. 2: *A schematic view of different stacking sequence for some common SiC polytypes.*

Compared to polytypes of other compounds, all SiC polytypes have a strong bond between the bi-layers that determine the material hardness. Of course, in the reality, there are small structural distortions, compared to the schematic stacks reported in *Figure 1.2*, but overall the structures illustrated are very well respected. The geometrical characteristics of the bi-layers characterize the different polytypes. For example, in the cubic polytype 3C-SiC, known $\boldsymbol{a_c}$, the length of the cubic cell, the length of the axes of the rhomboidal cell $\boldsymbol{a}$ and the thickness of the bilayer $\boldsymbol{t}$ are respectively:

$$a = \frac{a_c}{\sqrt{2}} \text{ and } t = \frac{a_c}{\sqrt{3}} \quad \textbf{(1.2)}$$

Finally, for a generic NX-SiC polytype, always indicating with ***c*** the length of the spatial period, with ***c/N*** the height of the tetrahedron, and finally with ***a*** the distance between the atoms in the Si-Si or C-C, it is possible to define a relationship characterizing the lattice:

$$\frac{c}{Na} = \sqrt{\frac{2}{3}} \approx 0.8165 \quad \textbf{(1.3)}$$

It is convenient to characterize SiC polytypes by the so called "hexagonality" γ [8], which is defined as the ratio between the number of atoms in hexagonal positions (N_H) and the total number of atoms in the unit cell (N_H+N_C):

$$\gamma = \frac{N_H}{N_H+N_C} \quad \textbf{(1.4)}$$

The hexagonality of a polytype may vary from unity (2H-SiC) to zero (3*C*-SiC). It is noteworthy that the ability to crystallize in different crystal lattices is inherent not only in SiC, but also in quite a number of other compounds: GaN, ZnSe, ZnO, diamond, etc.

At present, there is no theory that would be completely satisfactory in explaining why SiC crystallizes in a wide variety of polytypes. Moreover, it is not completely clear which are the key factors determining the formation of one or another polytype.

1.2 Electronic properties of SiC

The importance of SiC in the field of power electronics is mainly related to its electronic properties [9,10]. In *Table 1.1*, the fundamental electronic properties of the most common SiC politypes are listed, and compared to those of Si, GaN and Diamond.

	4H-SiC	3C-SiC	6H-SiC	Si	GaN	Diamond
E_G@300K [eV]	3.2	2.2	2.86	1.1	3.4	5.45
E_C [MV/cm]	3.5	2	3.8	0.3	2.0	10
v_{sat} [x10^7cm/s]	2.0	2.7	2	1.0	2.5	2.7
μ_n @N=10^{16}cm^{-3} [cm^{2}v^{-1}s^{-1}]	750	700	*370[a]	150	1000	2200
			*75[c]	0		
μ_p @N=10^{16}cm^{-3} [cm^{2}v^{-1}s^{-1}]	120	40	90	480	30	850
ε_r	9.7	9.7	9.7	11.9	8.9	5.5
λ [W/cm K]	5	4.9	4.9	1.5	1.3	22

Table 1. 1: *Key electronic properties of SiC polytypes vs. other semiconductor materials.*

From a direct comparison of the fundamental electrical properties, the advantages of SiC with respect to Si are basically the higher bandgap energy, E_G (about three times), the higher critical electric field, E_C (about ten times), the twofold increase in saturation velocity, v_{sat}, [11] and more than the doubling of thermal conductivity, λ [12]. It is instantly evident that wide bandgap semiconductors, and in particular SiC, are very promising materials in high performance electronic devices, where a higher critical electric field brings to power devices with higher breakdown voltages.

Although the carrier mobility in SiC is somewhat lower than in Si, in general the transport parameters give to SiC devices performances better than comparable Si devices.

Many of the favourable transport parameters in SiC are related to its large bandgap E_G: along with conduction and valence band structure, it defines the electric properties of the semiconductor. Band structure calculations for SiC have been made for the past forty years. Early, the theorists have concentrated on the zincoblende 3C-SiC polytype and the wurtzite 2H-SiC structure given that the other polytypes are much more complicated due to their larger unit cell [13]. Then, since both 3C-SiC and 2H-SiC are indirect-gap semiconductors, they have reasonably assumed that all polytypes are indirect-gap semiconductors. In the following years, the accuracy of initial calculations has been considerably improved to work also on the band structures of 4H- and 6H -SiC polytypes [14].

The SiC band structure is indirect, and the width of the bandgap strongly depends on the polytype. *Choyke et al.* in Ref.[15] have derived an empirical correlation of E_G with percentage of hexagonal planes. A plot of energy gap as a function of the hexagonality for the most common polytypes is shown in *Figure 1.3*, from which a quasi linear relationship is deduced. E_G varies from 2.39 eV for 3*C*-SiC (lower value) to 3.33 eV (higher value) for 2H- SiC.

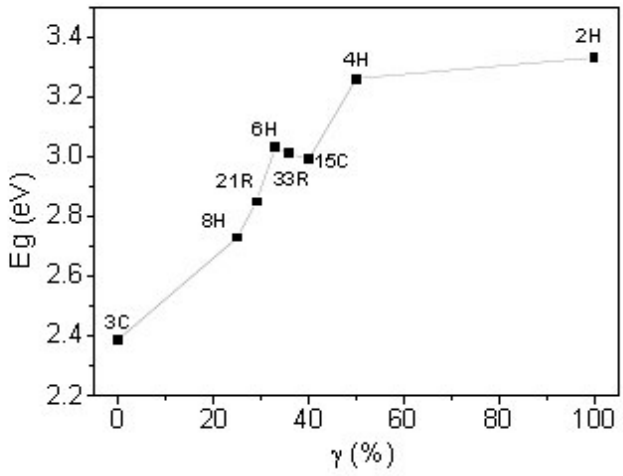


Figure 1. 3: *Energies of indirect bandgap of several SiC polytypes as a function of the hexagonality.*

In particular, the wide bandgap of 4H-SiC (3.2 eV) allows power devices to work at high junction temperatures such that they can operate at higher current densities without violating the power dissipation limit [16].

The number of atoms per unit cell in SiC varies from one polytype to another, and it influences the number of electronic and vibrational levels of the material. This difference in the band structure is due to the different physical and electrical properties between the several polytypes.

The intrinsic carrier density of several SiC polytypes is obviously determined by the wide band gap, E_G.

In particular, with the parabolic approximation for conduction and valence bands [17], the intrinsic carrier concentration can be expressed as a function of E_G and the temperature:

$$n_i^2 = N_C(T)N_V(T)e^{-\frac{E_{G(T)}}{KT}} \quad \textbf{(1.5)}$$

where K is Boltzmann constant and N_C (T) and $N_V(T)$ are the effective density of states in the conduction and valence bands, respectively, which are given by:

$$N_C(T) = 2M_C\left(\frac{2\pi m_e^* KT}{h^2}\right)^{3/2} \quad \textbf{(1.6)}$$

and

$$N_V(T) = 2M_C\left(\frac{2\pi m_h^* KT}{h^2}\right)^{3/2} \quad \textbf{(1.7)}$$

with m_e^* and m_h^* the electron and hole effective masses, and Mc the equivalent valleys in conduction band. For the 4H-SiC polytype, the values of these parameters are: $m_e^* = 0.77m_0$ [18], $m_h^* = 1.2m_0$ [19] (where m_0 is the electron rest mass) and $Mc=3$. Intrinsic carrier density is positively dependent on the temperature because the energy bandgap is a quadratic function of temperature and intrinsic carrier density is an exponentially dependent on the energy bandgap.

The modification of the density of states with the doping leads to an additional influence on intrinsic carrier density, the so-called "band gap narrowing". This phenomenon is generally modeled by rigid shifts of the band edges and brings [20], evaluating the consequent bandgap shrinking by the term ΔE_g to express the effective intrinsic carrier concentration as:

$$n_{ie} = n_i e^{\frac{\Delta E_G(T)}{2KT}} \tag{1.8}$$

Figure 1.5 shows the intrinsic carrier concentration n_i for the most common SiC polytypes (3C-SiC, 6H-SiC, and 4H-SiC) compared with that of Si as a function of the reciprocal temperature, where also the temperature dependence of energy gap (*equation **1.8***) is considered.

As expected, a larger bandgap leads to lower values of the intrinsic carrier concentration n_i: in particular for 4H-SiC, at room temperature (see dashed line) the intrinsic carrier density results 18 orders of magnitudes lower than in Silicon.

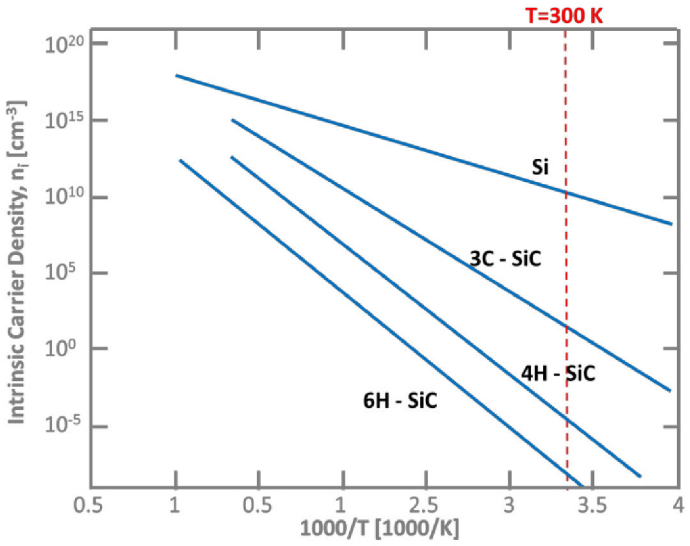


Figure 1. 5: *Intrinsic carrier density as a function of reciprocal temperature for the most common SiC polytypes, compared with Si.*

Another important parameter for the power switch devices is the saturation drift velocity, v_{sat}.

At high electric fields, the velocity ceases to be proportional to the electric field, due to increased scattering and it saturates at v_{sat} value. In SiC, the saturation drift velocity is 2-2.7 × 10^7 cm/sec [21], which is at least twice that of Si. A high-saturated drift velocity is advantageous in order to obtain high channel currents and to maximize the operation frequency, thus making SiC an ideal material also for high-gain and high-speed solid-state devices. In this way, it is allowed to achieve faster devices with shorter switching times [22].

One of the most widely investigated and discussed parameters in SiC polytypes is the mobility. In particular, the carrier mobility is generally related to the material properties such as crystallinity, spatial distribution and density of defect.

The mobility in SiC is somewhat lower than in Si and much lower than in high-mobility materials, such as GaAs. However, the low mobility in SiC devices is compensated by the possibility to operate at larger electric fields taking advantage of the higher carrier velocity.

The mobility describes the average velocity of carriers (electrons or holes) when an electric field is applied. At low electric fields, the velocity increases proportionally to the field, since the carrier mobility is fundamentally due to the Coulomb and phonon scattering. For higher fields, the proportionality is lost and the velocity saturates at v_{sat}. In general, there are various scattering mechanisms, which determine the free carrier mobility.

Carrier mobility is an important parameter for the high voltage devices, since it is related to their series resistance. In particular, in the case of MOSFETs (that are the object of this thesis), the mobility of the carriers in the inversion channel is a key parameter for the devices performance, as it will be discussed later.

The mobility model for electrons at low electric field has the form of *equation (**1.9**)* reported below, which is dependent on the doping concentration in the drift layer and on the temperature, with the maximum value of μ_{max} [23]:

$$\mu_n = \frac{\mu_{max}\left(\frac{300}{T}\right)^{\eta_B}}{1+\left(\frac{N_D-N_A}{N_{ref}}\right)^{\gamma_B}} \qquad \textbf{(1.9)}$$

where T is the lattice temperature, μ_{max} is the maximum mobility at T=300K. Commonly agreed value for the μ_{max} is 950 $cm^2/V \cdot s$ [24,25,26]. η_B, γ_B and N_{ref} are empirical parameters obtained experimentally [27]. N_A and N_D are the acceptor and donor doping concentrations, respectively.

The mobility is dependent on the local electric field, lattice temperature, doping concentration, polytype, crystal quality, local scattering at defects, etc. If the doping concentration increases, the mobility decreases due to scattering. For low doping concentration, the mobility decreases with temperature due to decreased vibrational energy of the lattice phonons.

However, as it will be reported in the next chapters, in MOSFETs the mobility in the channel region, which can be considered the heart of the device, is described by a different formalism, in order to consider the different contribution to the carrier scattering in the inversion layer.

Another important properties for power-device applications is the critical electric breakdown field, E_C. This property determines maximum electric field that the material can support before suffering physical breakdown.

As a wide-bandgap material, SiC offers a critical electric field of 3.5 MV/cm, i.e. one order of magnitude higher than that of Si [28]. A higher electric breakdown field enables the fabrication of power devices with a higher breakdown voltage. In order to understand this advantage, let us consider the breakdown voltage at an abrupt *p-n* junction, which can be expressed as [29]:

$$V_B = \frac{E_C W_D}{2} \tag{1.10}$$

where V_B is the breakdown voltage, Ec is the critical electric field and W_D the drift region width.

In *Figure 1.6* the breakdown voltage for different material as a function of the drift region width is reported:

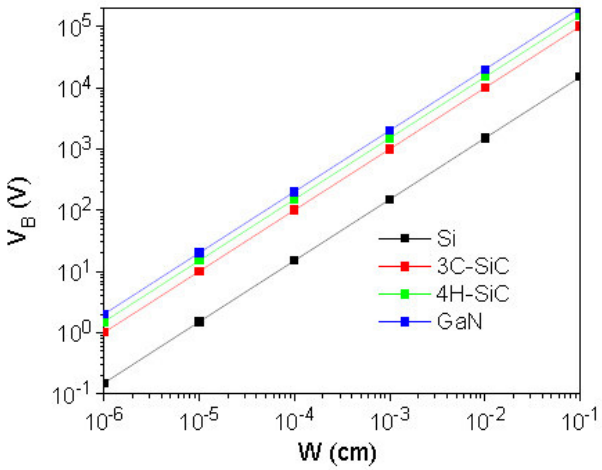


Figure 1. 6: *Breakdown voltage as a function of drift region width for Si, 3C-SiC, 4H-SiC and GaN.*

Clearly, for a given thickness of the drift layer, a higher breakdown voltage can be obtained using SiC devices.

The significant increase of the blocking capability of SiC power devices also allows their fabrication with much thinner and more highly doped drift layers, which greatly reduces the on-state resistance [30].

Moreover, the relation between the breakdown voltage and the doping concentration in a p-n junction is expressed as follow [31]:

$$V_B = \frac{\varepsilon_r E_C^2}{2qN_D} \quad \textbf{(1.11)}$$

where q is the charge of an electron and N_D is the doping concentration.

Accordingly, a higher electric breakdown field brings to power devices with higher breakdown voltages. In particular, the theoretical breakdown voltage of 4H-SiC is 46 times larger than that of a Si diode (assuming that the diodes are fabricated with the same doping concentration). As a result, high-voltage (≥ 1.2 kV) SiC unipolar switches, such as JFETs and MOSFETs, have become realistic to offer much faster switching speeds than the traditional high-voltage Si devices, which today have to be made using bipolar structures (e.g. BJT or IGBT), not sacrifying the conduction loss and even better increasing the efficiency.

Besides the mobility higher than silicon and the critical electric breakdown field, one of the most important electrical properties of SiC in high current and switching applications is the thermal conductivity, which is three times higher than the thermal conductivity of Si [12].

The high value of thermal conductivity allows the material to be more efficient in heat dissipation. This requirement is fundamental when operating at high temperature or at high current levels. The high temperature capability of SiC can reduce cooling requirements, which are a substantial portion of the total size and cost of a power conversion and distribution system. While actual Si transistors reach their normal operational temperatures approximately at 125°C, becoming highly susceptible to harsh environments, equivalent SiC devices promise to operate at temperature up to 600°C, and also at high power densities for both medium and high frequency switching applications [32]. Therefore, higher thermal conductivity, combined with wide band gap and high critical field, gives to SiC technology an advantage when high power is a desirable device feature [33].

Owing to all the aforementioned material properties, 4H-SiC devices are expected to drastically improve the distribution of usage of global electric power. In fact, 4H-SiC devices can be used in applications that require fast, efficient switching, such as industrial motor drives, high power DC data center power architectures, PFC (power factor correction), boost and high frequency DC/DC conversion circuits in industry, and computing and communications power systems.

1.3 References

[1] C. Kittel, Introduction to solid state physics, 6th ed: John Wiley & Sons, 1986.

[2] D.A. Neamen, Semiconductor Physics and Devices, Basic Principles, 3rd ed., Mc Graw Hill, 2003.

[3] P.Y. Yu, and M. Cardona, Fundamentals of Semiconductors. Physics and Material Properties, Springer, Berlin, 1995.

[4] W. F. Knippenberg, Philips Research Reports, vol.18, No. 3, pp.161-274, 1963.

[5] C.J. Schneer, Acta Crystallogr. vol.8, pp.279, 1955.

[6] H. Baumhauer, Z. Kristallogr. vol.50, pp.33, 1912.

[7] S.E. Saddow, and A. Agarwal, Advances in Silicon Carbide Processing and Applications, Artech House, Norwood, MA, 2004.

[8] H. Jagodzinskii, Acta Crystallogr. vol.2, pp. 201, 1949.

[9] W.J. Choyke and G. Pensl, Physical Properties of SiC. MRS Bulletin, vol. 22, pp 25-29, 1997.

[10] S. Nakashima and H. Harima Physica Status Solidi (a), vol.162 (1), 2001.

[11] Y. Liu, Ph.D. thesis, Auburn University (2006).

[12] J. Rozen, Ph.D. thesis, Vanderbilt University (2008).

[13] L. Patrick, W.J. Choyke, and D.R. Hamilton, Physical Review, vol. 137, no. 5A, pp. A1515-A1520, 1965.

[14] C. Persson e U. Lindefelt, Journal of Applied Physics, Vol. 82, no. 11, pp. 5496-5508, 1997.

[15] W. J. Choyke, D. R. Hamilton, and L. Patrick, Physical Review, Vol. 133, no. 4A, pp. A1163–A1166, 1964.

[16] P. G. Neudeck, J. B. Petit, and C. S. Salupo, in Proc. 2nd Int. High Temperature Electronic Conf., 1994, pp. 23-28.

[17] S.M. Sze, *"Physics of Semiconductor Devices"*, John Wiley & Sons, New York, 1981.

[18] N.T. Son, W.M. Chen, O. Kordina, A.O. Konstantinov, B. Monemar, E. Janzen, D.M. Hofman, D. Volm, M. Drechsler, and B.K. Meyer, Appl. Phys. Lett., Vol. 66, no. 9, pp. 1074-1076, 1995.

[19] N.T. Son, P.N. Hai, W.M. Chen, C. Hallin, B. Monemar, and E. Janzén, Physical Review B, Vol. 61, no.16, pp. R10544-R10546, 2000.

[20] A.H. Marshak, M.A. Shibib, J.G. Fossum, and F.A. Lindholm, IEEE Trans. on Electr. Dev., Vol. 28, no. 3, pp. 293-298, 1981.

[21] K. Järrendahl, and R. Davis, *Material Properties and Characterization of SiC, Semiconductors and Semimetals*, SiC Materials and Devices, Vol. 52, Y. S. Park, (ed.), 1998

[22] G.L. Harris, H.S. Henry and A. Jackson, *Carrier mobilities and concentrations in SiC*, in *Properties of Silicon Carbide*, edited by G.L. Harris, IEE INSPEC, London, UK, 1995, p. 63-68

[23] S.K. Powell, N. Goldsman, J.M. McGarrity, J. Bernstein, J.Appl. Phys. 92, 4053 (2002)

[24] D. Caughey and R. E. Thomas, *Proc. IEEE*, pp. 2192–2193, 1967.

[25] G. Choyke, W.J. Pensli, Mater. Res. Bull., 25-29, 1997

[26] W. J. Schaffer, G. H. Negley, K. G. Irvine, and J. W. Palmour, Proc. Mat. Res. Soc. Symp., vol. 339, pp. 595–600, 1994.

[27] H. Naik, T.P. Chow, Material Science Forum, 679-680, pp.595-598, 2011

[28] T.P. Chow, Microelectronic Engineering, 83, 112-122, 2006

[29] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics, 2nd ed.,* John Wiley & Sons, New York, 1995.

[30] K. Rottner, M. Frischholz, T. Myrtveit, D. Mou, K. Nordgren, A. Henry, C. Hallin, U. Gustafsson, and A. Schöner, Materials Science and Engineering B, 61–62, 330–338, 1999

[31] A. K. Agarwal, S. S. Mani, S. Seshadri, J. B. Cassady, P. A. Sanger, C. D. Brandt, and N. Saks, "SiC power devices," Naval Research Reviews, 51(1), pp. 14–21, 1999.

[32] M. Bhatnagar, and B.J. Baliga, "*Comparison of 6H-SiC, 3C-SiC, and Si for Power Devices"*, IEEE Trans. on Electr. Dev., Vol. 40, no. 3, pp. 645 – 655, 1993.

[33] J.B. Casady, and W. Johnson, "*Status of Silicon Carbide (SiC) as a wide bandgap semiconductor for high-temperature applications: a review and references cited*", Solid State Electron., Vol. 39, no. 10, pp. 1409-1422, 1996.

Chapter 2
Planar Power MOSFET for energy efficiency

As anticipated in the previous chapter, SiC is forecasted as the key material for the next generation of power switches.

Since 1980, the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) device is the most used semiconductor electronic device for power applications and represents the technological evolution of the integrated MOS. The increasing use of MOSFET devices is due mainly to the fact that it has a rather simple structure with low manufacturing costs. Thanks to its physical-chemical properties – such as high critical electric field, large energy gap, high thermal conductivity and finally the high electronic saturation velocity – SiC offers a response to the limits of Si for the development of devices that operate at high temperature and high voltages.

In this chapter, the main features and electrical behaviours of MOSFET devices are shown. In particular, comparing the figures of merit of 4H-SiC MOSFET and Si devices, the advantages of SiC highlight; indeed, it exhibits a better trade-off between the on-resistance and breakdown voltage, which allows to obtain a reduction of the power losses and an improvement in the efficiency of power MOSFETs devices.

2.1 Power applications and advantages of Silicon Carbide

Power Electronics plays a key role in the generation, storage, distribution cycle of the electric energy. Power devices are required for applications that operate over a broad spectrum of power levels [1]. *Figure 2.1* gives an overview of possible power applications, broken down into several categories, with respect to their current and voltage rating. As can be seen, the power applications can be found in all the range of power levels (from a few Ws to MWs), and they include many types of equipment (power supplies for computers, industrial and telecom systems, domestic appliances, motor drives, industrial converters, etc.) [2].

One third of the electricity produced in the world is lost in the final stage of power conversion, where power transistors play an important role. Wide Band Gap (WBG) semiconductors possess intrinsic properties that reduce losses in all power conversion processes. This is because they show lower conduction and switching losses as well as minimal leakage at high temperatures (as a consequence of the large gap and very low intrinsic carrier concentration).

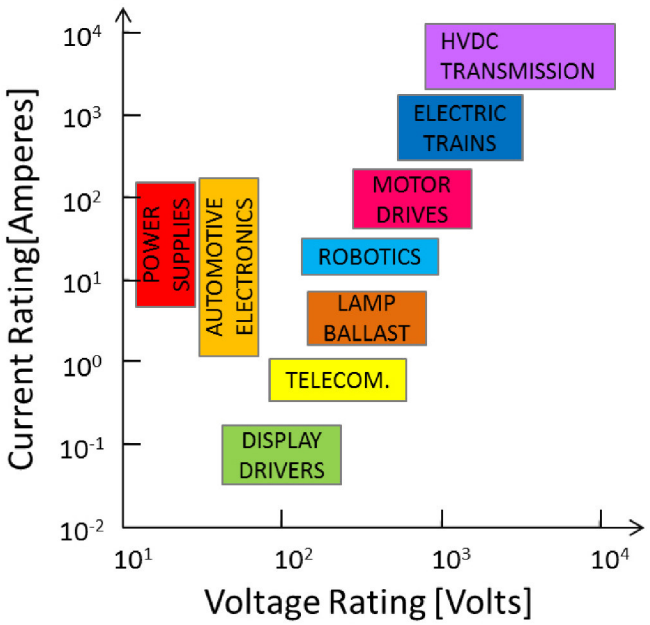


Figure 2. 1: *Potential field of applications for power devices, in a current vs voltage rating plot.*

Given that these transistors are the main devices in all power conversion processes, it is not surprising that microelectronic industry is showing a great interest in a technology that optimizes their performance.

The hardware of a power converter is based on power semiconductors as well as passive components (inductors and capacitors). When frequency is pushed higher, smaller inductors can be used and the overall size and weight are reduced. In this way, inductors will contain less copper and other materials and hence will be cheaper.

Silicon-based semiconductors show temperature limits, so it is necessary to spend extra money and energy on cooling requirements. Wide-band gap materials can operate more safely at high temperatures thanks to their high thermal conductivity (efficiency in dissipating the heat they generate).

Big data centers need power conversion to generate regulated DC voltages from the main grid. There are huge losses in the power room and a lot of heat dissipation, so every tiny saving makes a huge difference. One main problem posed by data centers is how to keep them cool. Extra electricity is consumed to get rid of the heat (fans, air-conditioning).

In the world of WBG materials, SiC is the most mature wide-band gap technology, even though it is more complex in principle than GaN; on the market 650 V and 1200 V diodes [3,4] are already available and first SiC MOSFETs appeared [3,5,6]. SiC is best exploited at voltages higher than 1200 V, but it will also be pushed in the future to reach voltages in excess of 6000 V.

For high-voltage and medium-high power range, the possible applications of SiC include solar inverters, railway transportation and electric vehicles. In fully electric and hybrid electric vehicles (EV and HEV) SiC can give longer battery life and a longer travel range with one battery charge. It is well placed to replace Si MOSFETs or IGBTs for both inverters and vehicle converters.

Any power device acts as a switch, i.e. when it is open it is in the "on" state. It is possible to reduce conduction losses by minimizing the resistance the device offers in this state, i.e. on-resistance. Furthermore, during the on/off switching phases there is inevitably some power loss. WBG technologies are also able to minimize power losses during turn-on and turn-off events even at higher frequencies because they make it possible to drastically reduce the size of magnetic components in the system.

As an example, the inductive turn-off losses versus temperature of a SiC MOSFET compared with the TFS (trench/field stop) and NPT (non-punch through) IGBTs *(Insulated Gate Bipolar Transistors)* and SiC MOSFETs are shown in *Figure 2.2 (a).* The turn-off losses of silicon devices are significantly higher than the SiC MOSFET and strongly increase with temperature. Also, the turn-on losses of the Si devices (IGBT or MOS) are higher than SiC MOSFETs, as it is shown in the *Figure 2.2 (b).*
In all cases the SiC MOSFET switching losses are significantly better than its Si competitors.

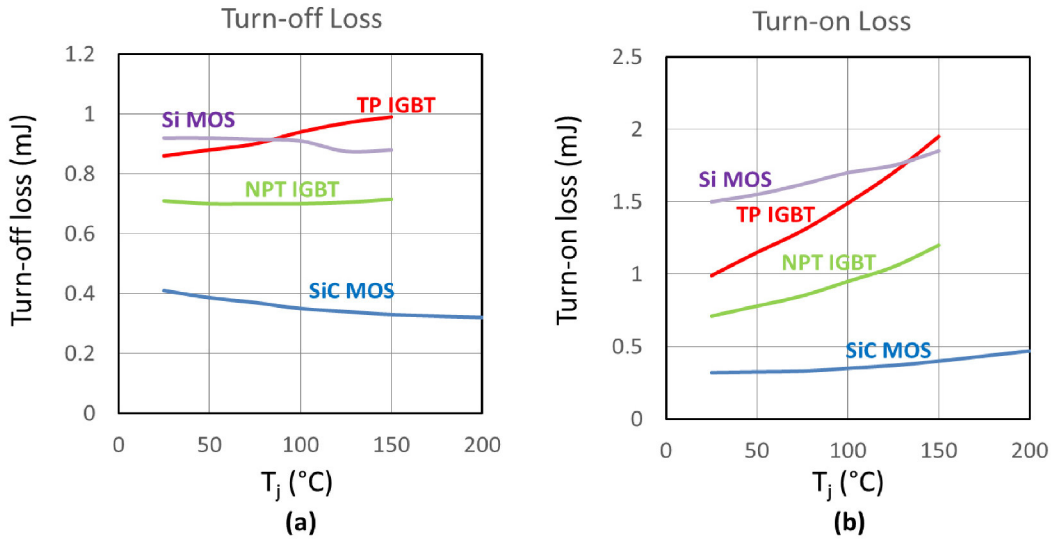


Figure 2. 2: *Inductive turn-off (a) and turn-on (b) losses versus temperature of SiC MOSFET compared with Si competitor devices.*

Therefore, SiC MOSFETs combine all three desirable characteristics of power switch, i.e. high breakdown voltage, low on-resistance and fast switching speed.

2.2 Power MOSFET in SiC and figures of merit

In Si technology, thyristors are favoured for the low frequency and very high power applications, IGBTs for the medium frequency and high power applications, and MOSFETs are typically restricted to lower power and high frequency applications. The structure which does overcome many of the voltage and on-resistance limitations of conventional MOS transistor is the power planar MOSFET with a double-diffused

technology, better known as D-MOS. This device began to appear in literature in the early 1970s and its structure made possible the revolution in discrete power MOS devices in Si [1].

Although excellent Si power MOSFETs devices are commercially available with breakdown voltages below 200 volts, the resistance of their drift region per unit of area increases rapidly at higher breakdown voltages approximately by the second power of the breakdown voltage, thus producing significant power losses in applications. As a result, IGBTs have been mainly used in devices with breakdown voltages of 600V or higher. IGBTs achieve lower on-resistance than MOSFETs by injecting minority carriers into the drift region, a phenomenon, called *conductivity modulation*. These minority carriers generate a current tail when the transistor is turned off, resulting in a significant switching loss.

The high breakdown field of SiC (which is up to ten times higher than Si) can make SiC DMOSFET more attractive than other semiconductor materials for field effect transistor operating at high voltage.

Compared to Si, both GaN and SiC exhibit largely better figures of merit for most of the key specifications, such as energy gap, electric field, electron mobility, and melting point, offering intrinsically better performance in terms of breakdown voltage, switching frequency and system efficiency [2].

In particular, SiC devices do not need conductivity modulation to achieve low on-resistance since they have much lower drift-layer resistance than Si devices. MOSFETs generate no tail current in principle. As a result, SiC MOSFETs have much lower switching loss than IGBTs, which enables higher switching frequency, smaller passives, smaller and less expensive cooling system. Compared to 600V-900V planar Si MOSFETs, SiC MOSFETs have smaller chip area (mountable on a compact package) and an ultralow recovery loss of the internal body diode.

For these reasons, SiC-MOSFETs are increasingly being used in power supplies for industrial equipment and inverters/converters for high-efficiency power conditioners.

The power MOSFET is a unipolar device. The current conduction occurs through the transport of majority carriers in the *drift region* without the presence of the injection of minority charge, typical in the operation of bipolar transistors (like IGBTs). A schematic cross section of a power MOSFET device with a vertical channel, known as ***DMOS,*** is reported below, in the *Figure 2.3*.

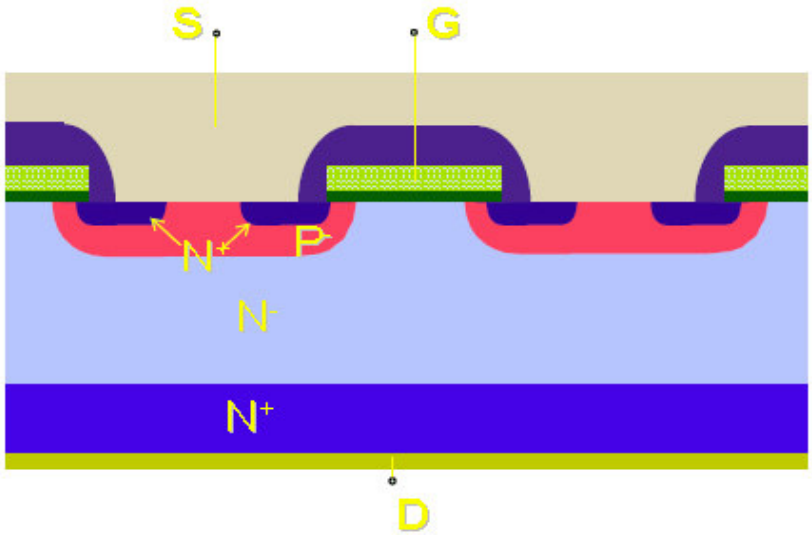


Figure 2. 3: *Cross section of power MOSFET device, known as DMOS.*

The region between the *Source* and *Drain*, called region of *JFET*, is under the influence of a metal electrode called *Gate*. The gate electrode is separated from the JFET region by an insulating layer, typically SiO_2. The structure of DMOS with the vertical channel, with source and drain on opposite sides, is particularly suitable for the power device, because it has a greater area available for the source region and also reduces the electric field close to the gate (dielectric breakdown field).

The device potential of a semiconductor material is often estimated in terms of ***figures of merit***.

Since SiC has a dielectric breakdown field strength (critical electric field) 10 times higher than that of Si, high breakdown voltage devices can be achieved with a thin drift layer with high doping concentration. It means that, at the same breakdown voltage, SiC devices have a significantly lower *specific on-resistance* $R_{on\text{-}sp}$ (on-resistance per unit area). In particular, the use of SiC can allow the minimization of the resistance of the drift region of the power device, R_D. Indeed, the resistance of the ideal drift region can then be related to the basic properties of the semiconductor material [7]. The solution of Poisson's equation leads to a triangular electric field distribution within a uniformly doped drift region with the slope of the field profile being determined by the doping concentration, shown in *Figure 2.4*.

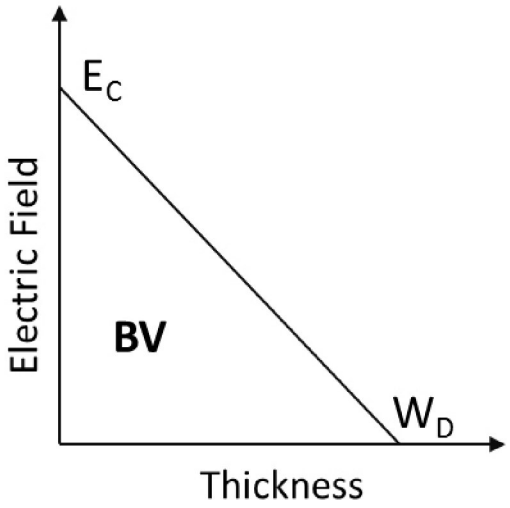


Figure 2. 4: *Ideal Electric field distribution in the drift region.*

The maximum voltage that can be supported by the drift region is determined by the maximum electric field (E_M) reaching the critical electric field (E_C) for breakdown for the semiconductor material. The critical electric field for breakdown and the doping concentration determine the maximum depletion width (W_D). The area of this triangle represents the breakdown voltage, BV.

The specific on-resistance $R_{on\text{-}sp}$ of the ideal drift region is commonly given by:

$$R_{on-sp} = \frac{W_D}{q\mu_n N_D} \tag{2.1}$$

where the depletion width under breakdown condition is given by:

$$W_D = \frac{2BV}{E_C} \tag{2.2}$$

BV being the desired breakdown voltage. Similarly, the doping concentration required to obtain the same breakdown voltage is expressed by the relation:

$$N_D = \frac{\varepsilon_S E_C^2}{2qBV} \tag{2.3}$$

Combining the above relations, the specific on-resistance of the ideal drift region is given by:

$$R_{on-ideal} = \frac{4BV}{\varepsilon_S \mu_n E_C^3} \quad \textbf{(2.4)}$$

The denominator of this equation ($\varepsilon_S \mu_n E_C^3$) is known as the *Baliga's Figure of Merit* (**BFOM**) for power devices [7] and represents the impact of the semiconductor material properties on the specific on-resistance. In particular, the specific on-resistance of the ideal drift region varies with the cubic power of the critical electric field (E_C^3). Hence, using wide band gap materials, like the SiC, a remarkable improvement of the on – resistance at the same breakdown voltage is possible. As an example, breakdown in 4H-SiC devices occurs when the electric fields are in the range of 2 – 3×10^6 V/cm (one order of magnitude larger than that for Si). As can be seen in *Table 2.1*, the BFOM of SiC is 464 times larger than in Si.

Besides the Baliga's figure of merit there are other figures of merit.

The Johnson's Figure of merit (**JFOM**) addresses the potential of a material for high frequency, voltage and power discrete amplifiers, according to [8]

$$JFOM = \frac{E_C^2 v_s^2}{4\pi^2} \quad \textbf{(2.5)}$$

The JFOM of 4*H*-SiC is up to 400 times better than Si and is only inferior to diamond. The Key's figure of merit (**KFOM**) instead considers the potentiality of a material for high frequency applications (relevant for MOSFETs). The KFOM takes into account the thermal limit of the high frequency devices performances imposed by semiconductors and it is given by [9]:

$$KFOM = k\sqrt{\frac{cv_s}{4\pi\varepsilon}} \quad \textbf{(2.6)}$$

where k, c, and ε are the thermal conductivity, the speed of light in vacuum, and the dielectric constant, respectively.

Table 2.1 summarizes the figures of merit for n-type 4H-SiC, 3C-SiC, diamond [10], GaN [11], GaAs [11] and Si [11]. All values are normalized with respect to Si.

	BFOM	JFOM	KFOM
Si	1	1	1
4H-SiC	464	400	4.17
3C-SiC	163	324	4.83
GaAs	14.6	1.78	0.32
GaN	1507	1600	3.04
Diamond	23000	8100	32.2

Table 2. 1: *Figures of merit of different semiconductors. The values are normalized with respect to Si.*

In *Figure 2.5* the specific on resistance for the ideal drift region of a unipolar device is reported as a function of the breakdown voltage. In particular, the theoretical value of Si is compared with the ideal values of the wide band gap materials. For example, a typical R_{on} value of 1.4 $\Omega\, cm^2$ obtained in a Si MOSFET becomes about 100 m $\Omega\, cm^2$ for a 4H-SiC MOSFET [12]. In theory, SiC can reduce the resistance per unit area of the drift layer to 1/300 compared to Si at the same breakdown.

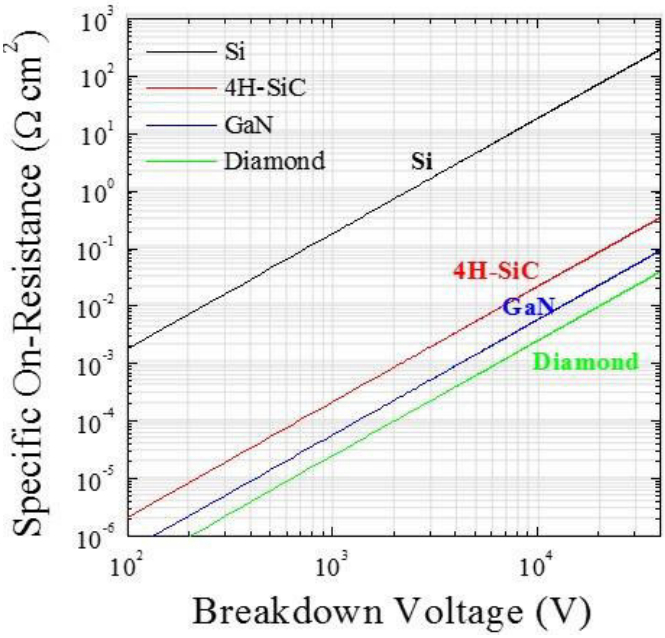


Figure 2.5: *Comparison of specific On-Resistance as a function of Breakdown Voltage for unipolar devices on different materials.*

Clearly, SiC exhibits a better trade-off between the R_{on} and breakdown voltage, which allows to obtain a reduction of the power losses and an improvement of the energy efficiency in the power MOSFETs devices. Indeed, the static power dissipation, known as *conduction loss*, in the power semiconductors is primarily dependent on their on-resistance. The conduction loss is the loss from an on-resistance of the transistor that is generated when the drain current goes through the body diode during dead time. In order to get the average value of the conduction loss, simply multiply the on-resistance (R_{on}) for the drain current. The conduction power losses of the MOSFET as a function of the on resistance can be expressed as:

$$P_{ON} = I_{on}^2 R_{DSon} \tag{2.7}$$

Notice that, I_{on} is the drain current when the MOSFET is on, and R_{DSon} is the drain-source resistance of the MOSFET when it is on. If the transistor is an ideal switch, there would be no conduction power loss. In order to reduce the conduction loss, on-resistance must be minimized. These aspects with Si technology result in an increase of the cost. Conversely, using 4H-SiC technology at the same breakdown voltage a

substantial decrease of Ron can be obtained and, consequently, a reduction of power losses.

2.2.1 MOSFET: basic operation principles and output characteristics

The basic MOSFET can be imagined just like a MOS-capacitor plus p-n junctions. The working mechanism of the MOSFETs is not complicated. *Figure 2.6* schematically reports the current flow within a planar power MOSFET. From *Figure 2.6*, it is easy to see that, if the gate voltage is not applied, no current flows from source to drain, because a reversed biased p-n junction blocks any electron flow, no matter the polarity of the source-drain voltage is. On the other hand, if gate voltage is not zero, the situation will be different. When a positive bias is applied to the gate, holes are repelled from the oxide/semiconductor interface and electrons simultaneously will move up to the interface. This movement creates a depletion layer (in the p-base region). With a more positive applied bias, the surface of the semiconductor inverts to produce an *n-type conductive region* on the surface of the P-base region, known as *inversion channel,* that connects the source N^+ and drift region N^- of the device. The current flows between the source and drain through the drift layer. Generally, the source terminal is grounded and voltage is applied to the drain terminal.

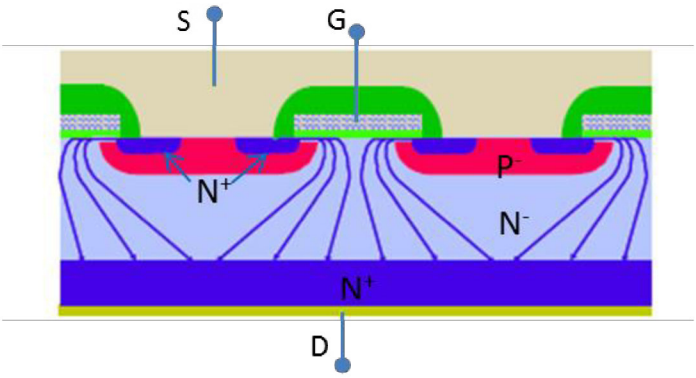


Figure 2. 6: *Schematic representation of the current flow within a power planar MOSFET.*

The voltage and the corresponding current are called drain voltage V_D and drain current I_D, respectively. The gate voltage is regarded as V_G. The voltage applied to the gate to

create the n-type inversion channel is an important parameter, which is called *threshold voltage*, V_{TH}. Simply speaking, the MOSFET will conduct if $V_G > V_{TH}$.

The typical output characteristic of a MOSFET in the conductive condition ($V_G > 0$) is reported in *Figure 2.7*. At low drain voltage, the behaviour is essentially resistive (*linear region)* and the device conduction resistance is determined exclusively by the slope of the characteristics. By increasing the drain voltage V_D, the current saturates as can be seen in the right area of the output characteristics of *Figure 2.7*, (*saturation region).*

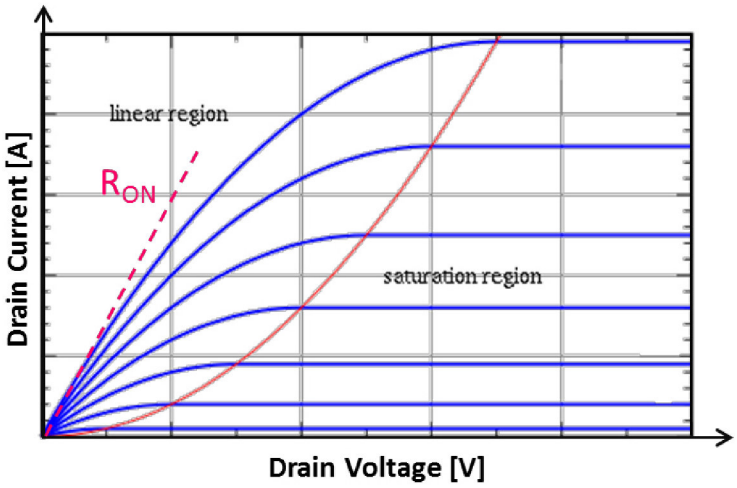


Figure 2. 7: *Typical I_D-V_D output characteristic of a power MOSFET.*

If the gate electrode is shorted to the source, $V_{GS} = 0$, the surface of the body region under the gate is not modulated in the charge, which is provided solely by the level of dopant. The SiC devices in this condition can support higher drain voltages, V_{DS}, than Si devices before reaching the avalanche of the junction, and will produce very small drain currents, i.e, *leakage current* of the device.

2.2.2 Contributions to the R_{on} in a planar MOSFET

The current flowing in a vertical power MOSFET device is limited by the total resistance between the source and drain terminals. This resistance, which represents the resistance (R_{ON}) of the device, is composed of different terms. The resistance of these regions must be included in the analysis of the total on – state resistance of the structure.

Figure 2.8 reports a schematic structure of the power planar MOSFET with the resistance components [13].

Then, the total specific on-resistance is given by:

$$R_{ON} = R_{CS} + R_A + R_{CH} + R_{JFET} + R_D + R_{subs} + R_{CD} \qquad \textbf{(2.8)}$$

where R_{CS} and R_{CD} are the specific contact resistance of source and drain terminals, respectively. In a first approximation, these contributions can be negligible. Moreover, the R_{CH} is the channel resistance, R_A is the accumulation region resistance, R_{JFET} is the resistance of the JFET region, R_D is the resistance of the drift region after taking into account current spreading from the JFET region and R_{subs} is the resistance of the N^+ substrate.

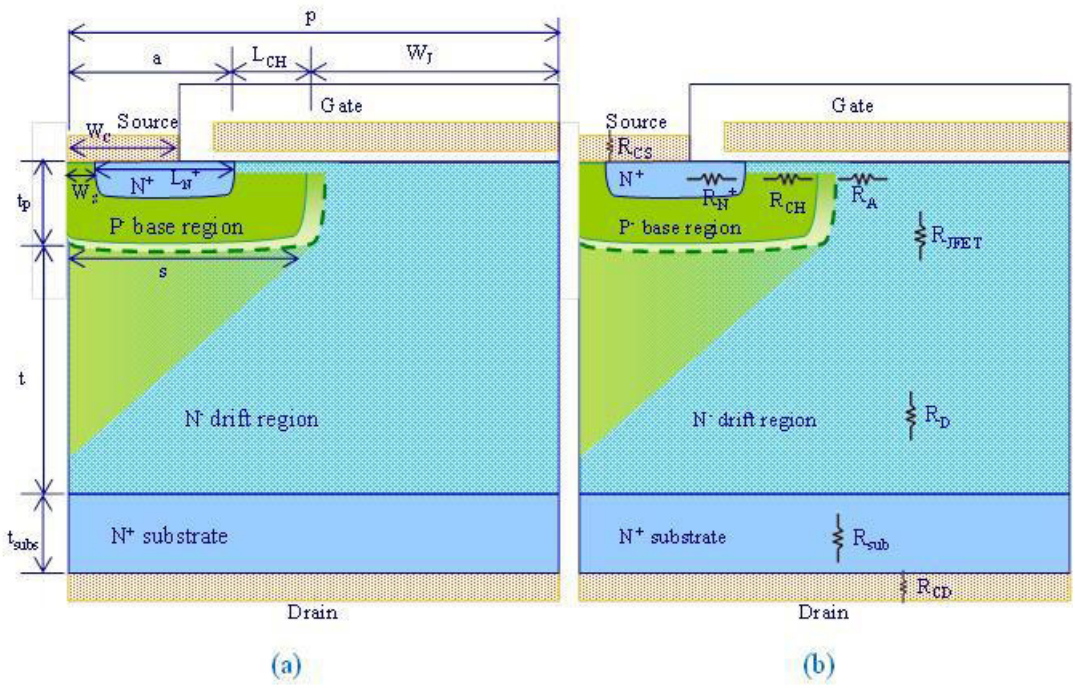


Figure 2. 8: *Schematic structure of the planar MOSFET. In particular, in (a) the geometrical components and in (b) the resistance components of R_{on} are reported.*

These resistances can be analytically modelled. The drain current flows through a channel region with a small cross-section before entering the JFET region. The current spreads into the drift region from the JFET region at a 45 degree angle and then becomes uniform. The dimension of "a" is fixed by the alignment tolerance during the device fabrication that typically is around 0.5 µm. The channel resistance is given by:

$$R_{CH} = \frac{L_{CH}p}{\mu_{inv}C_{ox}(V_G - V_{TH})} \quad \textbf{(2.9)}$$

where L_{CH} is the channel length as shown in Figure 2.7, μ_{inv} is the mobility for electrons in the inversion layer channel, C_{ox} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_{TH} is the threshold voltage.

Although an inversion layer mobility of 165 $cm^2V^{-1}s^{-1}$ has been observed in lateral MOSFET structures in 4H-SiC [14], the inversion layer mobility in high voltage 4H-SiC power MOSFET structure [15] is usually much lower, i.e. in the range 10 –20 $cm^2V^{-1}s^{-1}$.

The specific on – resistance contributed by the accumulation layer in a planar SiC MOSFETs is given by:

$$R_A = K_A \frac{(W_J - W_P)p}{\mu_{nA}C_{ox}(V_G - V_{TH})} \quad \textbf{(2.10)}$$

where the coefficient K_A has been introduced to account for the current spreading from the accumulation layer into the JFET region. A typical value for this coefficient is 0.6. In the case of n-channel 4H-SiC MOSFET structures, μ_{nA} is the accumulation layer mobility; a typical values is almost 4 times the channel mobility. In particular, in the case of n-channel 4H-SiC MOSFET structures, accumulation layer mobility values of 100–200 $cm^2V^{-1}s^{-1}$ have been experimentally observed [16]. Moreover, W_P is the "zero bias" depletion width for the JFET region. The "zero bias" depletion width in the JFET region can be computed by using its doping concentrations on both sides of the junction and the built-in potential V_{Pib}:

$$W_P = \sqrt{\frac{2\varepsilon_0\varepsilon_{SiC}V_{Pib}}{qN_D}} \quad \textbf{(2.11)}$$

The electrons entering from the channel into the drift region are distributed into the JFET region via the accumulation layer formed under the gate electrode. The current flow through the JFET region can be treated with a uniform current density. The specific on-resistance contributed by the JFET region in the planar SiC MOSFET structure can be obtained by using

$$R_{JFET} = \rho_D t_P \left(\frac{p}{W_J - W_P}\right) \quad \textbf{(2.12)}$$

where ρ_D is the resistivity of the JFET region given by

$$\rho_D = \frac{1}{q\mu_n N_D} \quad \textbf{(2.13)}$$

where μ_n is the bulk mobility appropriate to the doping level of the JFET region.
The resistance contributed by the drift region in the planar SiC MOSFET structure is enhanced above that of the ideal drift region due to current spreading from the JFET region. The drift region spreading resistance can be obtained by using:

$$R_{DRIFT} = \rho_D p \, ln\left(\frac{p}{W_J - W_p}\right) + \rho_D\left(t - p + W_J + W_P\right) \quad \textbf{(2.14)}$$

Finally, the substrate resistance contribution depends on the substrate resistivity and its thickness. This contribution is given by the relationship:

$$R_{sub} = \rho_{sub} t_{sub} \quad \textbf{(2.15)}$$

In *Figure 2.9*, the various on-resistance components have been modelled using the above analytic expression [2] for a 4H-SiC planar MOSFET, with a drift region doping concentration of $10^{16}cm^{-3}$ and thickness of 20µm:

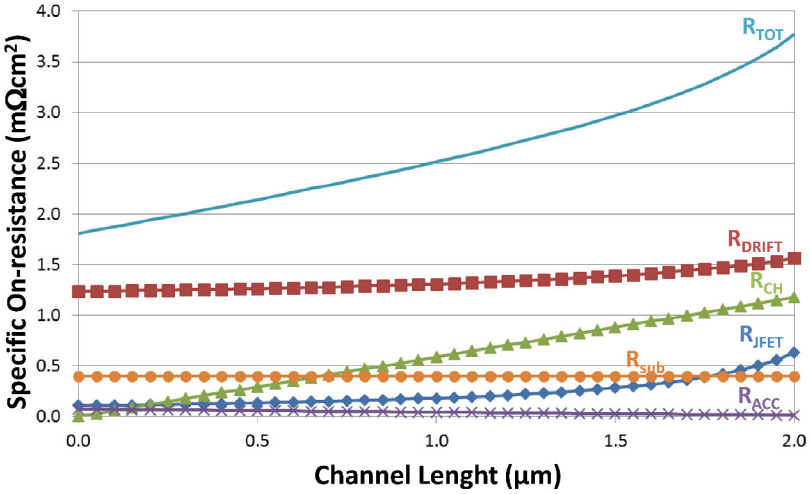


Figure 2. 9: *Components of the R_{on} for 4H-SiC planar MOSFET calculated assuming an inversion channel mobility of 100 $cm^2V^{-1}s^{-1}$.*

In *Figure 2.9* the different components to the total resistance have been determined assuming an inversion channel mobility of 100 $cm^2V^{-1}s^{-1}$.

However, the channel mobility values obtained in 4H-SiC MOS-devices are much lower, due to the large number of electrically active defects at SiO_2/SiC interface. In particular, the typical channel mobility values are about 20 $cm^2V^{-1}s^{-1}$, which implies a high channel resistance component and, hence, a remarkable on-resistance increase. The different components of the R_{on}, calculated for a channel mobility of 20 $cm^2V^{-1}s^{-1}$, are reported in the *Figure 2.10*.

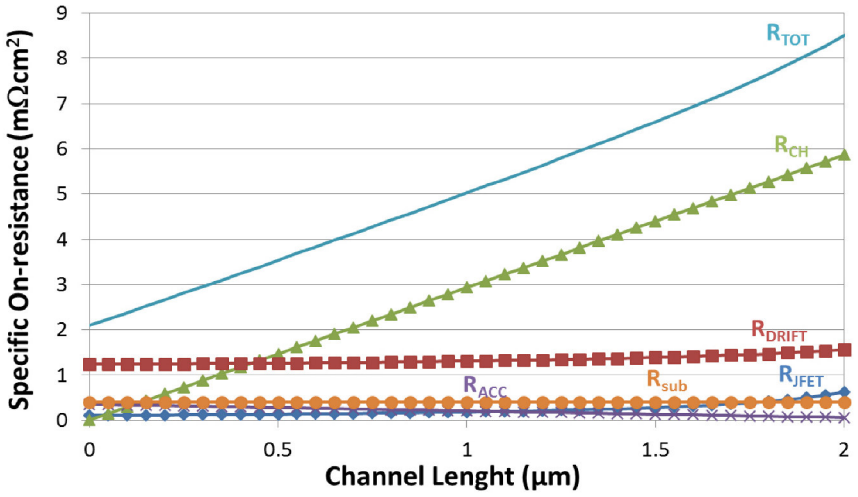


Figure 2. 10: *Components of the R_{on} for 4H-SiC planar MOSFET calculated assuming an inversion channel mobility of 20$cm^2V^{-1}s^{-1}$.*

Therefore, as a consequence of this behaviour, the on-resistance and, consequently, the on-state performances of SiC power MOSFETs are strongly limited by the channel resistance. In fact, the weakest building block in 4H-SiC MOSFETs technology is the channel fabrication.

2.3 Technology Issues for 4H-SiC MOSFET fabrication

Although the 4H-SiC MOSFET is considered to be significantly advantageous as compared to other types of power devices, some technical difficulties need to be overcome before it can achieve its full potential and it can replace silicon as the dominant semiconductor.

The persistent problems plaguing SiC device development are the realization of thermally stable Ohmic contacts to p-SiC with low resistivity and the notoriously low channel mobility in MOS devices. Both issues strongly impact the specific on – resistance of the devices. Not least, the gate oxide reliability under high temperature and high electric field is a fundamental open issue for SiC devices.

Regarding the Ohmic contact on p-type region, ion-implantation is the method of choice used for local doping of SiC [17, 2,18,19], since conventional diffusion techniques cannot be used, due to the small diffusivity of impurities in the material. As a matter of fact, ion-implantation doping of SiC is currently employed to fabricate several planar devices, like Schottky diodes, junction barrier Schottky (JBS) and metal-oxide-semiconductors field effect transistors (MOSFETs). However, in spite of the important and original progresses achieved in the last years, two closely linked physical issues still represent a concern for these devices, i.e., the p-type doping process by ion-implantation and the formation of Ohmic contacts on the implanted p-type regions. In particular, the reduction of the specific contact resistance of Ohmic contacts is required to minimize the total device series resistance (R_{on}) and, ultimately, to reduce the overall power dissipation of single device and/or complex power modules.

While for n-type doping of SiC an almost complete electrical activation of the implanted dopant ions (i.e., Phosphorous) can be achieved already upon annealing at 1500°C [18,20], p-type doping (i.e., Aluminium) requires annealing at higher temperatures (T = 1500-1800°C) to promote the electrical activation of the dopant in

substitutional lattice sites [18, 21, 22, 23]. Hence, efficient p-type doping by Al-implantation remains a challenging task, due both the high ionization energies of acceptors, and to the high thermal budget required to achieve the electrical activation of the implanted dopants and remove the lattice damage [17]. It has been shown that p-type implantation into 4H-SiC followed by high temperature activation annealing (1700 ºC – 1750 ºC) can cause a surface roughness phenomenon called "step bunching" due to loss of silicon from the surface [24, 25]. This latter, in turn, could affect the transport properties in the material and/or, ultimately, the electrical characteristics of metallic contacts formed on the implanted regions.

However, the major limiting factor in realizing efficient MOS gated power devices is the low channel mobility. This poor mobility is commonly attributed to the presence of the exponentially increasing interface states density towards the conduction band edge, resulting in substantial electron trapping and Coulomb scattering at the SiO_2/SiC interface [26]. The origin of these traps is linked to the imperfect nature of the SiO_2/SiC interface, like the presence of carbon clusters [27,28,29] and dangling Si and C bonds. Moreover, interface surface roughness may also play a major role in affecting channel mobility through interface roughness scattering of the electrons. This surface degradation can lead to extremely low channel mobility in 4H – SiC MOSFETs.

Recently, various approaches have been employed to improve the quality of the MOS interface for higher channel mobility. The most successful method is the annealing of the gate oxide in nitric oxide or nitrous oxide ambient [30,31].

In the next chapters, the influence of the morphology of p – type implanted region on the microstructure and electrical properties of Ohmic contacts, as well as the impact of surface- and gate-oxide-processing on the MOSFET channel mobility will be presented. These two aspects represent the largest part of the experimental work of this thesis.

2.4 References

[1] B.J. Baliga, “Fundamentals of Power Semiconductor Devices”, Springer Science, New York, 2008.

[2] B.J. Baliga, “Silicon Carbide Power Devices”, World Scientific Press, Singapore, 2005.

[3] www.st.com

[4] www.infineon.com

[5] www.cree.com

[6] www.rohm.com

[7] B. J. Baliga, "Semiconductors for High Voltage Vertical Channel Field Effect Transistors", J. Applied Physics, Vol. 53, pp. 1759-1764, 1982.

[8] E.O. Johnson, RCA Rv., 26, 163, 1965.

[9] R.W. Keyes, Proc. IEEE, 60, 225, 1972

[10] R.F. Davis, “Thin films and device of diamond, silicon carbide and gallium nitride”, Physica B 185, 1-15, 1992

[11] Y. Zhou, D. Wang, C. Ahyi, C-C. Tin, J. Willimas, M. Park, N. M. Williams and A. Hanser, Solid-State Electronics 50, 1744, 2006

[12] B.J. Baliga, IEEE Transaction on Electron Devices, vol. 43 (10), 1996.

[13] B.J. Baliga, “Advanced Power MOSFET Concepts”, Springer Science + Business Media, LLC 2010.

[14] S. Sridevan and B.J. Baliga, “Lateral N-channel Inversion Mode 4H-SiC MOSFETs”, IEEE Electron Device Letters, Vol. 19, pp. 228–230, 1998.

[15] S.H. Ryu, et al., “10-kV 5-A 4H-SiC Power DMOSFET”, IEEE International Symposium on Power Semiconductor Devices, Abstract 7.2, pp. 265–268, 2006.

[16] P.M. Shenoy and B.J. Baliga, “The Planar 6H-SiC ACCUFET”, IEEE Electron Device Letters, Vol. 18, pp. 589–591, 1997.

[17] Pensl G, Ciobanu F, Frank T, Krieger M, Reshanov S, Schmid F and Weidner M 2006 *SiC Materials and Devices,* Shur M, Rumyanstev S and Levinshtein M eds., Singapore, World Scientific, Vol. 1, pag. 1-41.

[18] Mitra S, Rao M V, Papanicolaou N, Jones K A, Holland O W, Vispute R D, Wilson SR 2004 *J. Appl. Phys*. **95** 69.

[19] Roccaforte F, Libertino S, Giannazzo F, Bongiorno C, La Via F, Raineri V 2005 *J. Appl. Phys* **97** 123502.

[20] Laube M, Schmid F, Pensl G, Wagner G, Linnarsson M, Maier M 2002 *J. Appl. Phys.* **92** 549.

[21] Saks N S, Agarwal A K, Ryu S-H, and Palmour J W 2001 *J. Appl. Phys.* **90** 2796.

[22] Negoro Y, Kimoto T, Matsunami H, Schmid F and Pensl G 2004 *J. Appl. Phys.* **95** 4916.

[23] Sundaresan S G, et al., 2008 *Solid-State Electronics* **52** 140.

[24] Rambach M, Bauer A J, and Ryssel H 2008 *Phys. Stat. Sol. (b)* **245** (7) 1315.

[25] M. A. Capano. S. Ryu, and J. A. Cooper, Jr., "Surface roughening in ion implanted 4H-Silicon Carbide", Journal of Electronic Materials, Vol. 28, pp.214, 1999.

[26] J. A. Cooper, M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, "Status and prospects for SiC power MOSFETs", IEEE Trans Electron Dev, Vol.49, pp.658-64, 2002.

[27] V. V. Afanasev, M. Bassler, G. Pensl, and M. Schultz, "Intrinsic SiC/SiO2 interface states", Physica Status Solidi (a), Vol.162, pp.321, 1997.

[28] V.V. Afanasev, F. Ciobanu, S. Dimitrijev, G. Pensl and A. Stesmans, J. Phys.: Condens. Matter 16, S1839 (2004).

[29] F. Ciobanu, G. Pensl, V. V. Afanas'ev, and A. Schoner, Mater. Sci. Forum 483-485, 693 (2005).

[30] Y. Wang, T. Khan, M. K. Balasubramanian, H. Naik. W. Wang, and T.P. Chow, IEEE Trans. Electron Devices 55(8), 2046 (2008).

[31] S.-H. Ryu, S. Dhar, S. Haney, A. Agarwal, A. Lelis, B. Geil, and C. Scozzie, Mater. Sci. Forum, 615-617, 743 (2009).

Chapter 3
Ohmic contacts on p-type SiC

The formation of a good Ohmic contact on implanted p-type regions is an important technological step in the fabrication of SiC power devices. In fact, like in other WBG semiconductors, also in p-type SiC the achievement of a low contact resistance is a challenge, due to the large Schottky barrier heights at the metal-semiconductor interface and the high ionization energy of the p-type dopants for SiC.
In this chapter, the influence of a different morphology and microstructure of Al-implanted 4H-SiC, resulting from two different high temperature annealing conditions, on the electrical and structural properties of Ti/Al Ohmic contacts is discussed. The electrical measurements show a lower specific contact resistance when using a protective carbon capping layer during the post – implantation annealing. The study of the temperature dependence of the specific contact resistance enabled the extraction of the barrier height. The electrical results were correlated with the microstructural analysis of the interface region.

3.1 Ohmic contacts for SiC devices

Good Ohmic contacts are important for the power transfer between the semiconductor and the external circuitry. A contact resistance that is significantly higher compared to the on-resistance of the device leads to a voltage drop at the metal-semiconductor interface, in turn resulting in decreased efficiency due to added resistive losses [1,2,3]. The most important characteristic of the Ohmic contacts is the specific contact resistance, ρ_c, an intrinsic interfacial property, which is independent of the contact region. In particular, a reduction of the specific contact resistance of Ohmic contacts is required to minimize the total device series resistance (R_{on}) and, ultimately, to reduce the overall power dissipation of single devices and/or complex power modules. However, the fabrication of low-resistance Ohmic contacts is difficult, because of the high metal/p-type SiC Schottky barrier and the high ionization energies of p-type dopants.

For n-type SiC several Ohmic contact solutions to achieve a low specific contact resistance have been studied in these years [4], discussing the current transport mechanisms [5]. Usually, the contact have been deposited on SiC material with a wide range of the doping concentration (obtained by epitaxial doping or by ion-implantation) and were subjected to annealing processes under a large variety conditions. Typically, annealed Ni has been the most widely used metal for Ohmic contact to n-type SiC [6]. In particular, the formation of low resistance ohmic contacts to n-type SiC is achievable by Ni_2Si contacts, formed by annealing Ni films above 950 ºC; it is the only stable silicide phase during the reaction between SiC and Ni [7]. The carbon present in the consumed silicon carbide layer should precipitate [8]. The first quantitative electrical data on the specific contact resistance of nickel silicide ohmic contact to n-type SiC were reported by Crofton et al., [9],who measured a good value of specific contact resistance of $\rho_c < 5\times10^{-6}\Omega cm^2$.

Thus, as result an Ohmic contact with reduced specific contact resistance is formed.

On the other hand, there is less consensus in literature on the mechanisms of Ohmic contacts and carrier transport to p-type SiC. Indeed, due to the wide band gap of SiC, the formation of Ohmic contact to p-type SiC with low Schottky barrier heights values is a crucial issue but less works are reported on Ohmic contact to the p-type with respect to the n-type materials [10,11,12].

A wide variety of metallizations under several annealing conditions [13], such as metal silicides [14] and metal carbides [15,16], have been investigated, often with controversial results. Due to the low Schottky barrier and to the possibility to use Aluminum to obtain p-type doping of SiC, Al-based alloyed contacts received much attention as Ohmic contacts to p-type SiC. Indeed, many literature works reported on Al-based Ohmic contacts and Al/Ti-based systems to p-type SiC [17,18,19]. Al/Ti contacts are generally non-Ohmic after deposition, while annealing temperatures above 900 ºC are required to obtain an Ohmic behaviour of the contact [18].

Many authors propose directly the use of annealed Ti/Al bi-layers or AlTi alloys. In *Table 3.1,* some literature data of the specific contact resistance of Ti/Al based contacts to p-type SiC have been reported.

Metal	N_A *(atm/cm^3)*	*Annealing*	ρ_c *[Ωcm^2]*	*Polytype*	*Ref.*
Al/Ti	1x10^{19} epi	900°C, 3min vacuum	6.4x10^{-4}	4H	[11]
Al/Ti/Al	4.8x10^{18} epi	1000°C, 2min vacuum	3.3x10^{-4}	4H	[10]
Al/Ti	1.3x10^{19} epi	1000°C, 2min vacuum	3x10^{-5}	4H	[20]
Al/Ti	2x10^{19} epi	1000°C, 5min Ar	1.5x10^{-5}	6H	[17]
Al/Ti	4x10^{19} Al-imp	1000°C, 2min Ar	3x10^{-5}	6H	[21]
Al/Ti	1-3x10^{19} epi	950°C, 2min N_2	2-3x10^{-5}	6H	[22]

Table 3. 1: *Specific contact resistance ρ_c of Al/Ti based Ohmic contacts on p-type SiC.*

Crofton et al. [17] reported a first quantitative investigation on the electrical properties of Al/Ti contacts on p-type SiC. In particular, the contacts were annealed at 1000°C, which resulted into an Ohmic behaviour with a low specific contact resistance ρ_c = 1.5×10^{-5} Ωcm^2 at a high doping level (N_A=2×10^{19}cm^{-3}). In general, most of these studies were focused on epitaxial layers, showing that the specific contact resistance is strongly depending on the carrier doping level of the substrate [17]. However, as it will be explained in the next paragraph, for specific devices application it is important to study the behavior of these contacts on p-type implanted regions. Even if the use Al/Ti bi-layers is largely diffused to obtain Ohmic behaviour on p-SiC, many aspects related to the Ohmic contact formation on the implanted p-type SiC and to the current transport mechanisms have not been fully explained yet.

Ion-implantation is the method of choice used for local doping of SiC [2,23,24,25], since conventional diffusion techniques cannot be used, due to the small diffusivity of impurities in the material. As a matter of fact, ion-implantation doping of SiC is currently employed to fabricate several planar devices, like Schottky diodes, junction barrier Schottky (JBS), metal-oxide-semiconductors field effect transistors (MOSFETs). However, in spite of the significant progresses achieved in the last years, two closely linked physical issues still represent a concern for these devices, i.e., the p-type doping process by ion-implantation and the formation of Ohmic contacts on the implanted p-type regions.

While for n-type doping of SiC an almost complete electrical activation of the implanted dopant ions (i.e., Phosphorous) can be achieved already upon annealing at 1500°C [24, 26], Aluminium (Al) implantation for p-type doping, requires annealing at

higher temperatures (T = 1500-1800°C) to promote the electrical activation of the dopant in substitutional lattice sites [24,26,27]. However, efficient p-type doping by Al-implantation remains a challenging task, due both the high ionization energies of acceptors, and to the high thermal budget required to achieve the electrical activation of the implanted dopants and remove the lattice damage [2,3].

It is well known that the surface morphology of SiC can be strongly modified by the high thermal budgets necessary for the electrical activation of implanted dopants [28]. At high temperatures (~ 1500 °C) preferential evaporation of Si from the surface starts to occur, giving rise to a peculiar roughening of the surface ("step bunching"), characterized by the formation of large terraces parallel to the original miscut angle. This step bunching is greatly enhanced in the regions subjected to high implantation doses [29,30], and could affect the transport properties in the material and/or the electrical characteristics of metallic contacts formed on these implanted regions. In order to reduce this detrimental effect, the surface of SiC can be protected during post-implantation annealing by using a capping layer, mostly a carbon capping layer formed by a pyrolyzed photoresist film, which is then removed after annealing and before any other processing step of the wafer [31,32].

Although a variety of metals have been used to form Ohmic contacts to p-type SiC, metallization schemes based on Ti-Al layers have given the most promising results in terms of specific contact resistance both on epitaxial and implanted layers [33,4,34,21,10], as already mentioned above. However, while most of these studies were focused on epitaxial p-type SiC layers, the impact of the surface morphology of implanted SiC (which in turn is influenced by the post-implantation annealing conditions during devices fabrication) on the properties of Ti/Al Ohmic contacts was not fully addressed so far. In few cases a homogenous interface could be obtained and a carrier transport mechanism was proposed [35].

In this thesis, due to the importance of this topic, the morphology, microstructure and carrier transport mechanism in alloyed Ti/Al Ohmic contacts to p-type Al-implanted 4H-SiC were studied. In particular, it will be shown that the Al/Ti/SiC interface is not uniform on implanted 4H-SiC. An improvement of the SiC surface morphology before metal deposition can be achieved and it leads to a reduction of the Ti/Al roughness and of the specific contact resistance of the annealed Ti/Al Ohmic contacts. Combining temperature dependent electrical measurements with a microstructural analysis of the

interfacial region allowed us to model the electrical behavior of the non-uniform contacts.

3.2 Specific contact resistance in metal/semiconductor Ohmic contacts

Metal/semiconductor contacts are designated either as *Ohmic* or as *rectifying* (or *Schottky*). Ohmic contacts are characterized by linear and symmetric current-voltage (I-V) characteristics, with a voltage drop that is insignificant compared to the one caused by the on-resistance of the device [1]. Conversely, a rectifying contacts, display strongly non-linear *I-V* behaviour, where the current flows only under positive bias voltage conditions and conduction is blocked under reverse bias. In order to introduce the important physical parameters which affect the contact behaviour, the classical description of the Schottky barrier formation is reported.

Figure 3.1 shows the energy band diagram of a metal and a *p*-type semiconductor according to the *Schottky model,* in the case $\phi_m<\phi_s$ before (a) and after (b) they are brought into contact.

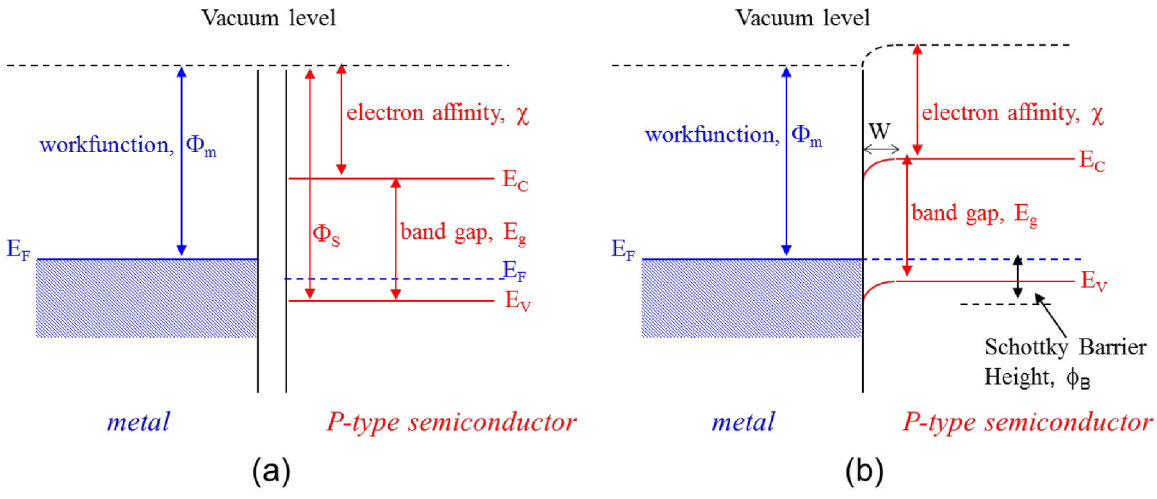


Figure 3. 1: *Energy band gap for a metal/semiconductor (p-type) contact, in the case $\phi_m<\phi_s$ before (a) and after (b) they are brought into contact, showing a formation of a rectifying contact with a Schottky barrier height $q\phi_B$.*

The work function of a solid is the energy required to move an electron from the Fermi level of the material to the vacuum level. The metal work function Φ_m and the semiconductor work function Φ_s are indicated in the band diagrams in *Figure 3.1(a)*. The semiconductor electron affinity, χ_s, is the potential difference between the bottom of the conduction band E_C and the vacuum level. When the materials are brought into contact (*Figure 3.1(b)*), holes flow from p-type semiconductor to metal, leaving a negatively charged acceptor region behind, W, and the Fermi levels in the two materials align in order to reach thermal equilibrium. In this way the energy bands in the semiconductor will be lowered near the contact by an amount of V_{bi} . For metal contacts on p-type material, the Schottky barrier height $q\Phi_B$ is correlated to the difference between the metal work function $q\Phi_m$ and the semiconductor electron affinity $q\chi_s$ by:

$$q\Phi_B = E_g - q(\Phi_m - \chi_s) \qquad \textbf{(3.1)}$$

where E_g is the gap.

Clearly,the large forbidden energy gap of SiC (3.2eV for 4H-SiC) together with the electron affinity of material (4eV) leads to a position of the valance band more than 7eV away from the vacuum level. Hence, since most metals have work functions in the range 4-5 eV, it is difficult to find metals forming a low Schottky barrier to p-SiC. To remedy this problem, the use of alloyed metallic compounds and specific annealing conditions can be required to achieve interfaces with low barrier height values [36,37,38]. Obviously, this must be always combined with the use heavily doped material. In this way, the holes can tunnel through the thin barrier and the Ohmic contact is formed.

The contact resistance R_C is the physical parameter which characterizes the resistance of metal-semiconductor interface. However, the most useful quantity used to define the performance of an Ohmic contact is the *specific ohmic contact,* ρ_c. It is independent of the contact area (the unit is Ωcm^2) and, hence, is useful to compare contacts with different sizes.

The most common method to determine the specific contact resistance is the *Transmission Line Model (TLM)* [39]. The linear TLM technique consist of measuring the *I-V* behaviour of an array of identical rectangular metallic pads, overlying the layer to be characterized, of length *L* and width *W*, separated by different pad distances *d*.

A schematic of the specific measurement setup used in this thesis is illustrated in *Figure 3.2 (a)*, and *I-V* curves measured at the different pad distances are presented in *Figure 3.2 (b)*.

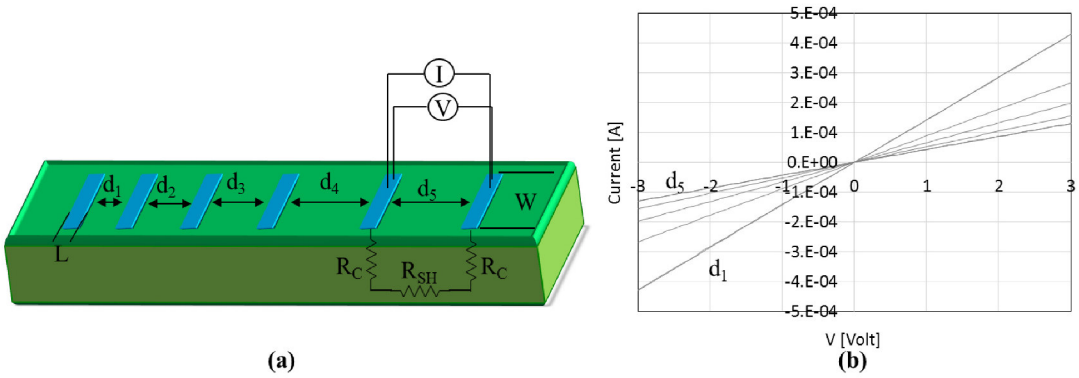


Figure 3. 2: *(a) A schematic of the TLM measurement setup; (b) I-V curves measure at different pad distances.*

The total resistance R_T between two adjacent pads depends on the contact resistance R_C and on the semiconductor sheet resistance R_{SH} according to:

$$R_T = 2R_C + \left(\frac{R_{SH}}{W}\right) d \qquad \textbf{(3.2)}$$

By reporting the total resistance R_T as a function of distance d, a liner plot is obtained, at shown in *Figure 3.3*, in which the intercept with the y-axis is $2R_C$, while the intercept with x-axis is $2L_T$. L_T is the *transfer length*, defined as the distance from the contact edge at which the current density drops to *1/e* of its original value.

Hence, the effective contact area, i.e., the fraction of the geometric area which takes part to the current condition, is given by:

$$A_C = WL_T \qquad \textbf{(3.3)}$$

The semiconductor sheet resistance R_{SH} can be extracted from the slope of the plot R_T vs d.

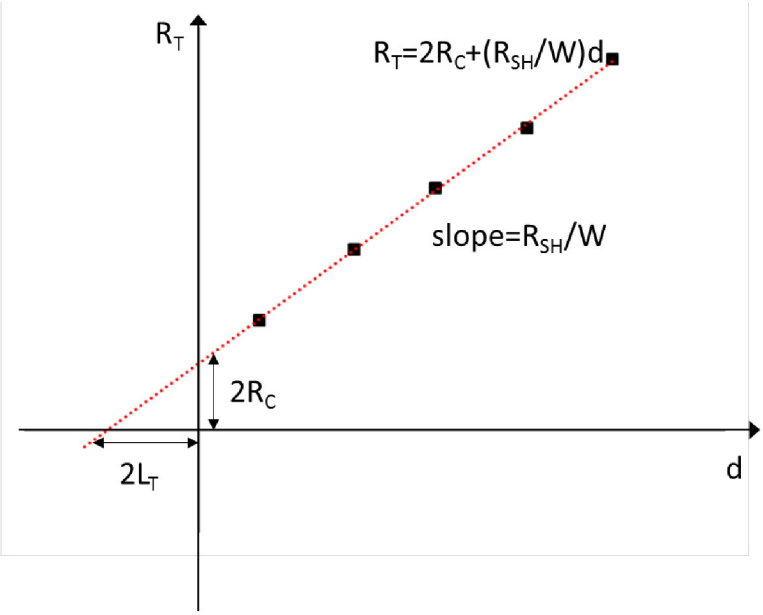


Figure 3. 3: *Plot of the total resistance R_T as a function of the distance between the pads d, from which the contact resistance R_C, the sheet resistance R_{SH} and the transfer length L_T can be determined.*

The specific contact resistance can then finally be obtained from:

$$\rho_C = R_C W L_T tgh\left(\frac{L}{L_T}\right) \quad \textbf{(3.4)}$$

Two cases lead to simplifications of equation (3.4).

For $L << LT$, $tgh(L/LT) \approx L/LT$ and

$$\rho_C = R_C W L \quad \textbf{(3.5)}$$

On the other hand, for "electrically long contacts" ($L>>L_T$), the specific contact resistance can be obtained by the product of the contact resistance and the effective contact area:

$$\rho_C = R_C W L_T \quad \textbf{(3.6)}$$

For the contact in this work, $L>>L_T$ and consequently the approximation in equation (3.6) was used to extract the specific contact resistance values.

3.3 Experimental Details

As previously reported by other authors [21,40,41], a different Ti/Al ratio can lead led to remarkable differences in elemental distribution, interface chemistry, surface roughness and reproducibility of Ti/Al Ohmic contacts to p-type SiC. In this work the thickness of the metal layers was chosen basing on the common evidence, that an Al-rich condition is essential to yield low contact resistance in alloyed Ti/Al systems [33,42].

Linear transmission line model (TLM) [43] structures were fabricated for the macroscopic electrical characterization of both the p-type doped material and the Ohmic contacts, to determine the sheet resistance R_{SH} and specific contact resistance ρ_c.

For the experiment, an N-type 4H-SiC epitaxial layers, 6 µm-thick with a doping concentration of 1×10^{16} cm^{-3}, grown on heavily doped n^+-type substrates, were used. The samples were implanted with Al-ions at 400 °C, using multiple energies (30-80 keV) at two different doses of $1.3\times10^{14}cm^{-2}$ and $1.3\times10^{15}cm^{-2}$ to form an almost uniform dopant profile extending over a depth of approximately 175 nm. Al-ion implantation was performed in selected regions, defined by a lithographic process. Post–implantation annealing at 1700 °C was carried out for electrical activation of the dopant, *with* and *without* a protective carbon capping layer previously formed on the sample surface. The capping layer was removed after the high-temperature activation annealing. The ohmic contacts were formed sputtering Ti (100nm)/Al (300nm) bi-layers on the p-type Al-implanted regions, followed by a rapid annealing at 950 °C.

The main steps of the fabrication flow chart of the TLM structures are reported in the *Table 3.2*:

Processes	Description	
Wafer cleaning		
Photolithography for the formation of p-region at high temperature (T = 400ºC)	Dielectric deposition and the definition of the body region	
Multiple ion implantation of Aluminum	Doping dose between 10^{14}-10^{15} cm^{-2} and the implantation energy varies from 30 keV to 200 keV.	
Deposition of carbon capping layer in the wafer *with cap*	Photoresist	
Dopant activation annealing	*Without cap:* @1700 ºC in Ar +SiH_4	*With cap:* @1700 ºC in Ar
Removal of capping layer in the wafer *with cap*	Low temperature oxidation process + HF etch	
Oxide deposition	Intermediate oxide formation	
Photolithography for the formation of contacts	Contacts definition	
Formation of Ti/Al contacts on p-implanted SiC	Sputter Ti (100nm)/Al (300nm)	
	RTA 950 ºC, 60" in N_2	

Table 3. 2: *Main steps of the fabrication flow chart of TLM structures.*

The TLM structures, (rectangular pads of 100 µm x 200 µm) were defined by optical lithography and sequential wet etch of the two metal layers in the clean room equipment of CNR-IMM. The distances *d* between the metallic pads vary from a minimum of 10 µm to a maximum of 50µm.

In the *Figure 3.4* a picture of the TLM structures after the contacts definition is shown.

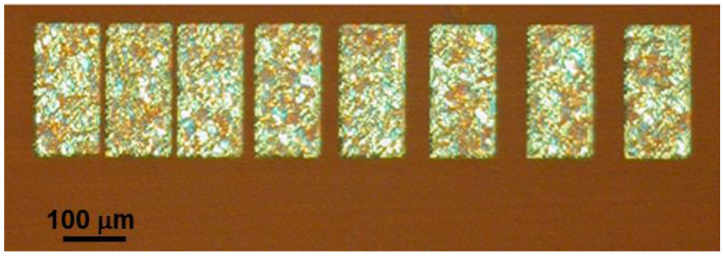


Figure 3. 4: *Picture of the TLM structure fabricated and characterized in this thesis.*

A schematic (in cross section) of the structure used in this work is reported in the *Figure 3.5*:

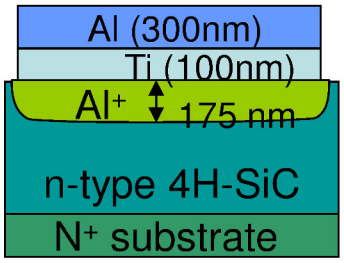


Figure 3. 5: *Schematic cross section of the analysed structures.*

Current voltage (I-V) measurements were carried out using a four points Karl Suss Microtec probe station equipped with a HP 4156B parameter analyzer. The measurement temperature was varied in the range of 25–150 °C, using a Lakeshore 331 temperature controller connected to the chuck.

The surface morphology and the microstructure of both Ohmic contacts and implanted layers were investigated employing several techniques, including atomic force microscopy (AFM), transmission electron microscopy (TEM), and X-ray diffraction (XRD).

3.4 Surface morphology of implanted 4H-SiC and Ti/Al Ohmic contacts

The surface morphology of the Al-implanted 4H-SiC regions and of the Ti/Al Ohmic contacts were monitored by AFM before and after any treatment.

After Al-implantation at high dose ($1.3\times10^{15}cm^{-2}$), but before the post-implantation annealing at 1700°C, the samples exhibited a quite flat surface with a mean surface roughness (root mean square, RMS) of 1.14 nm; this RMS value is slightly increased with respect to the RMS of the as-grown material (0.9 nm). A similar behaviour was observed in the sample implanted at low dose ($1.3\times10^{14}cm^{-2}$). Important changes of the RMS were observed after high temperature post-implantation annealing. *Figures 3.6(a)* and *3.6(b)* show the AFM scans taken over 20×20 μm^2, for the samples implanted at high dose and annealed at 1700°C, either *without* or *with* the protective carbon capping layer. The scans were acquired after removal of the capping layer. As can be observed, the RMS of the samples has increased after high-temperature annealing. However, while the sample annealed without capping layer shows a significant increase of the RMS up to a value of 18.9 nm and a pronounced "step bunching" is present on the sample surface (*Figure 3.6a*), the morphology of the sample annealed with the capping layer remained quite well preserved, with RMS value of 2.4 nm (*Figure 3.6b*). After high-temperature activation annealing at 1700°C and removal of the capping layer, Ti/Al bi-layers were sputtered on the 4H-SiC surface. Hence, rapid annealing at 950°C was carried out to achieve Ohmic characteristics of the contacts. The surface morphology of the annealed contacts is shown in *Figures 3.6(c)* and *3.6(d)* (for the contacts formed on SiC samples annealed *without* and *with* capping layer, respectively).

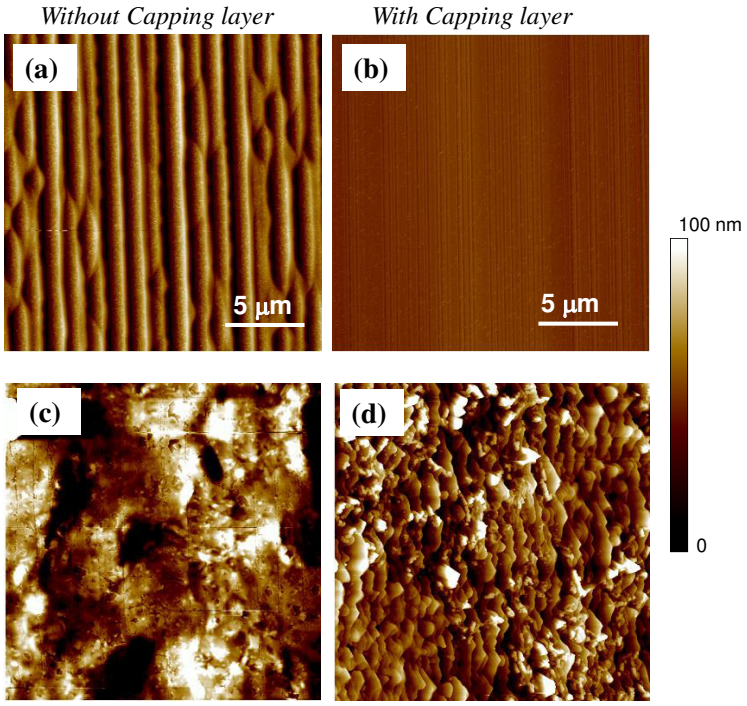


Figure 3. 6: *AFM scans of Al-implanted 4H-SiC surface for samples implanted at high-dose and annealed at 1700°C "**without**" capping layer (a) and "**with**" capping layer (b). AFM scans of alloyed Ti/Al contacts formed on Al-implanted 4H-SiC surface for samples annealed "**without**" capping layer (c) and "**with**" capping layer (d).*

It is evident that the alloyed Ti/Al contacts exhibit a large surface roughness, which is clearly influenced by the large RMS of the underlying implanted SiC. In fact, it can be noticed that the higher is the roughness of SiC, the higher is the roughness of the alloyed Ti/Al contacts formed on it. The RMS values of the contacts formed on the sample implanted at high dose were 44.0 nm and 22.8 nm, *without* and *with* the use of capping layer, respectively. A similar RMS trend was observed also in the case of low dose implantation.

The results of the morphological AFM analysis, both for the SiC surface and Ti/Al Ohmic contacts, are summarized in *Table 3.3*. Clearly, the significant reduction of the surface roughness of the contacts can represent an advantage during SiC device fabrication, especially when the lithographic definition of critical geometries is required.

	High – dose		**Low – dose**	
as–grown 4H-SiC	0.9 nm		0.9 nm	
As-implanted 4H-SiC	1.14 nm		1.10 nm	
	Without Cap	**With Cap**	**Without Cap**	**With Cap**
Implanted and annealed (1700°C) 4H–SiC	18.9 nm	2.4 nm	9.0 nm	1.3 nm
Alloyed (950°C) Ti/Al contacts	44.0 nm	22.8 nm	43.5 nm	20.8 nm

Table 3. 3: *Surface roughness (RMS) of 4H-SiC and alloyed Ti/Al contacts for the different implantation/annealing conditions.*

3.5 Specific contact resistance of Ti/Al Ohmic contacts

The electrical properties of the contacts, evaluated by conventional TLM analysis carried out at room temperature, showed a different electrical behaviour of the alloyed Ti/Al Ohmic contacts, depending on whether the capping layer was used or not. The results of TLM analysis are summarized in *Table 3.4*. The reported values are the average of several measurements performed on 10 different patterns fabricated in various regions of the sample surface.

	With cap		**Without cap**	
	High-dose	**Low-dose**	**High-dose**	**Low-dose**
$\rho_C(\Omega cm^2)$	1.45×10^{-4}	7.52×10^{-4}	3.51×10^{-4}	3.70×10^{-3}

Table 3. 4: *Specific contact resistance ρ_c of alloyed Ti/Al contacts measured at room temperature for the different implantation/annealing conditions.*

In particular, Ti/Al contacts formed on the capped sample exhibit, on average, a lower specific contact resistance with respect to those formed on the uncapped sample.

As an example, for the samples implanted at high dose specific contact resistance values of $\rho_c = 1.45\times10^{-4}$ Ωcm^2 and $\rho_c = 3.51\times10^{-4}$ Ωcm^2 were measured for the capped and uncapped sample, respectively. On the other hand, for the low implantated dose $\rho_c = 7.52\times10^{-4}$ Ωcm^2 and $\rho_c = 3.70\times10^{-3}$ Ωcm^2, for the capped and uncapped sample, respectively. Beside the practical advantage coming from the reduction of contact roughness, mentioned in the last paragraph, other important implications are related to the reduction of the specific contact resistance. In particular, considering that such Ti/Al alloyed contacts can be used as metallization to p-type SiC in implanted p-n junctions or can be integrated in more complex devices (like JBS or MOSFETs), it is possible to estimate the impact of the reduction of ρ_c on the total specific series resistance R_{ON} of the p-n diode. Taking into account the different contributions to the series resistance (like the specific contact resistance ρ_c, the resistance of the p-type Al-implanted layer, and the contribution of the n-type epitaxial layer and substrate [44]), the experimentally observed reduction of ρ_c achieved when using a capping layer should result into an overall reduction of R_{ON} between 12% and 60%, depending on the implanted dose. This latter, in turn, can consequently lead to a reduction of the power dissipation or can give the possibility to reduce device area.

Higher values of ρ_c (ranging from 8×10^{-4} Ωcm^2 to 2×10^{-3} Ωcm^2) were reported by Ito *et al.* [45] for alloyed Ti/Al contacts formed on p-type 4H-SiC, doped by ion-implantation with a similar Al-concentration (~1×10^{19} cm^{-3}). The experimental values of ρ_c determined by the TLM showed a dispersion in the order of 20%. This latter could be ascribed to the electrical inhomogeneity of the metal/SiC interfacial region, as will be also demonstrated by a structural analysis in the paragraph 3.4. A similar spread in the values of ρ_c in Ti/Al alloyed contacts on p-type ion implanted 6H-SiC was also found by Moscatelli *et al.* [21] , who pointed out that the specific contact resistance is expected to be highly sensitive even to small variations of the doping concentration.

Clearly, the results reported in this paragraph demonstrate that the electrical properties of alloyed Ti/Al Ohmic contacts can be improved when the contacts are formed on smoother SiC surfaces. Similarly, it was recently reported that the improved morphology of SiC surfaces, achieved using a protective graphite disk during the post-implantation annealing, leads to an improvement of the specific contact resistance ρ_c

and uniformity also in the case of Ti/AlNi/W contacts [46]. However, an exhaustive explanation of this behaviour was not given in that work.

One could simply correlate the improvement of the specific contact resistance observed when using a capping layer to the better surface morphology of the alloyed Ti/Al bi-layer observed by AFM (*Figures 3.6c* and *3.6d*). However, the transport properties of the annealed Al/Ti/SiC system are related, to a large extent, to the nanoscale electro-structural properties of the interfacial region, including both the metal and the underlying implanted 4H-SiC. Hence, other experimental electrical and structural measurements (presented in the next paragraphs) were carried out in order to give a clearer physical scenario explaining our result.

3.6 Temperature dependence of the electrical properties of implanted 4H-SiC and Ti/Al Ohmic contacts

Firstly, the macroscopic electrical properties of the Al-implanted 4H-SiC (averaged over the entire implanted thickness) were monitored by means of both TLM analysis and room temperature Hall measurements.

The values of the sheet resistance R_{SH} of the implanted layer, determined by TLM analysis, are reported in *Table 3.5*.

	With cap		**Without cap**	
	High-dose	**Low-dose**	**High-dose**	**Low-dose**
R_{SH}(Ω/sqr)	24.84×10^3	76.56×10^3	25.45×10^3	80.50×10^3

Table 3. 5: *Sheet resistance R_{SH} of Al-implanted 4H-SiC measured at room temperature for the different implantation/annealing conditions.*

As can be seen, R_{SH} did not significantly depend on the use of the capping layer during high-temperature activation annealing, but it mainly depends on the Al-implanted dose.

Indeed, in the samples implanted at high dose the sheet resistance was in the order of 25 kΩ/sqr, while in the samples implanted at low dose was in the range 76-80 k Ω/sqr.

Room temperature Hall measurements allowed to estimate the free hole concentration in the implanted layer. Assuming a uniformly implanted layer of thickness t_{imp} = 175 nm, free holes concentration values of 6.63×10^{17} cm^{-3} and of 6.42×10^{17} cm^{-3} were determined for the samples implanted at high dose and annealed with and without capping layer, respectively. On the other hand, in the samples implanted at low – dose hole concentration values of 1.01×10^{17} cm^{-3} and of 9.96×10^{16} cm^{-3} were found respectively for the samples annealed with and without capping layer. The values of the Hall mobility, determined using a Hall scattering factor of 0.8 [47], were in the order of 17 $cm^2V^{-1}s^{-1}$ and 37 $cm^2V^{-1}s^{-1}$ for the high and the low implantation dose, respectively. Hence, as already observed for the sheet resistance, also the mobility is not influenced by the surface morphology.

The high values of sheet resistance and low free hole concentration determined at room temperature can be associated to an incomplete activation of the implanted Al dopant atoms. In fact, the free hole concentration p is only a small fraction of the implanted concentration, due to the high energy of the acceptor levels (~190 meV) [48] or to an incomplete activation of the implanted Al [49]. As a consequence, in some devices applications, like in the case of a JBS where p-type implanted stripes are integrated inside a n-type drift region, the high sheet resistance imposes a constraint in the layout, consisting in the need of a good Ohmic metallization over the entire stripe, in order to avoid any undesired potential drop and excess of series resistance under high current operation [23].

The sheet resistance R_{SH} of the implanted layer was determined by TLM analysis as a function of the temperature, performing TLM measurements varying the sample temperature between 25°C and 150°C. The results are shown in *Figure 3.7* for the sample implanted at high dose and annealed *with* or *without* the capping layer.

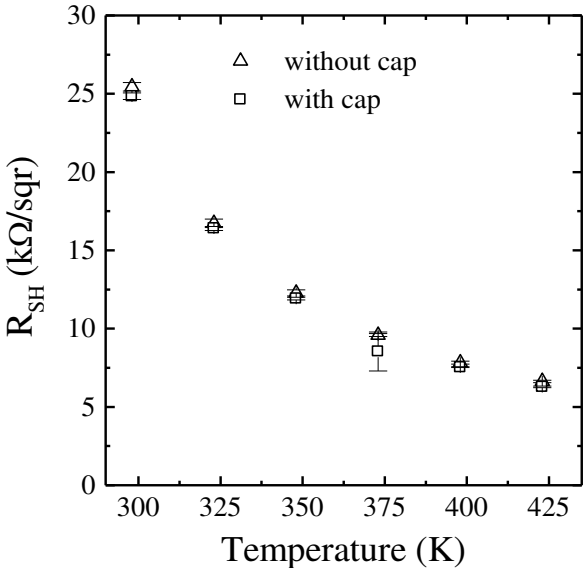


Figure 3. 7: *Sheet resistance R_{SH} of implanted 4H-SiC as a function of the measurement temperature for the high implantation dose and annealing at 1700°C "with" and "without" capping layer.*

In both samples R_{SH} decreases in a similar way with increasing measurement temperature T, from around 25 kΩ/sqr at room temperature to 6.6 kΩ/sqr at 425 K.

For a uniformly implanted layer of thickness t_{imp}, the temperature dependent sheet resistance $R_{SH}(T)$ is related to the free hole concentration $p(T)$ and to the holes mobility $\mu_p(T)$ by the relation:

$$R_{SH}(T) = \frac{1}{q\mu_p(T)p(T)t_{imp}} \tag{3.7}$$

where q is the elementary charge.

For a p-type semiconductor the net free hole density $p(T)$ depends both on the acceptor concentration N_A and on the concentration of compensating donor centres N_D [50]. In particular, in the examined temperature range, the temperature dependence of free hole concentration $p(T)$ can be expressed by a simplified form [28,43]:

$$p(T) \approx \frac{(N_A - N_D)N_V}{gN_D}\exp\left(-\frac{E_A}{kT}\right) \tag{3.8}$$

where N_V is the effective density of states in the valence band, g the degeneracy factor for acceptors (usually taken as 4), k is the Boltzmann constant, T the absolute temperature and E_A the ionization energy of acceptors referred to the top of the valence band.

The mobility μ_p depends both on N_A and on the temperature T. This dependence can be described by the following relation [51]:

$$\mu_p(T, N_A) = \mu_p(300, N_A)\left(\frac{T}{300}\right)^{-\beta(N_A)} \tag{3.9}$$

where $\mu_p(300, N_A)$ is the mobility at T=300 K and $\beta(N_A)$ is an empirical parameter which depends on the implanted doping concentration.

Hence, using the expression of N_V [43], the literature value $\beta(N_A)$ = 2.56 for our doping conditions [51], and the experimental value of $\mu_p(300, N_A)$ determined by Hall measurements, it is possible to combine the equations (**3.8**) and (**3.9**) with the expression of the sheet resistance (Eq. (**3.7**)), demonstrating that R_{SH} follows a thermally activated dependence as:

$$R_{SH} = T^{1.06}\frac{gN_D}{N_A - N_D}\frac{h^3}{2(2\pi m^*)^{3/2}}\frac{300^{-\beta}}{qt_{imp}\mu_p(300, N_A)}\exp\left(\frac{E_A}{kT}\right) \tag{3.10}$$

Hence, reporting in a semilogarithmic plot $\frac{R_{SH}}{T^{1.06}}$ as a function of the inverse of the absolute temperature should give an Arrhenius dependence, from which the activation energy can be determined.

Figure 3.8 reports the semilogarithmic plot of $\frac{R_{SH}}{T^{1.06}}$ as a function of q/kT, determined from the data in *Figure 3.7*, for the samples implanted at high dose and annealed with and without capping layer. As it can be seen, the experimental data follows an Arrhenius law according to equation (**3.10**). From a linear fit, it was possible to determine the values of the activation energy E_A of 144 meV for the sample annealed with capping layer and 141 meV for the sample annealed without capping layer.

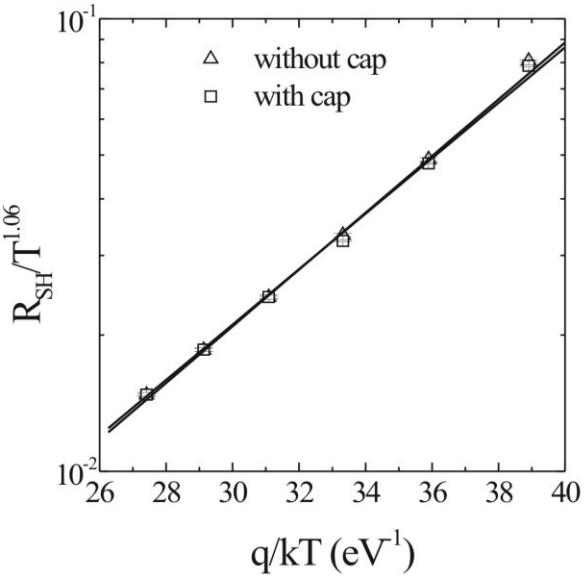


Figure 3. 8: *Semilogarithmic plot of as a function of q/kT for the samples implanted at high-dose and annealed at 1700°C "**with**" and "**without**" capping layer.*

Clearly, all the electrical results presented above provided average information on the properties of the implanted layer (like the sheet resistance, free carrier concentration, mobility activation energy of the dopant), indicating that all these macroscopic quantities are not significantly affected by the surface morphology obtained in our conditions. However, in order to get further physical insights into the properties of Ohmic contacts, namely on the current transport at the Al/Ti/SiC interface, we monitored the temperature dependence of the specific contact resistance. In fact, in a metal/semiconductor system this dependence is typically related to fundamental physical parameters, like the barrier height Φ_B and the doping density N [52]. In particular, the barrier height is extremely sensitive to the interfacial properties (like the microstructure, presence of different phases, uniformity and surface inhomogeneity of the dopant activation). Such an analysis provided interesting information to understand the different electrical behaviour of the contacts fabricated on implanted SiC annealed with or without the capping layer.

The specific contact resistance ρ_c as a function of the temperature T, for the samples implanted at high-dose (with and without capping layer) is shown in *Figure 3.9*.

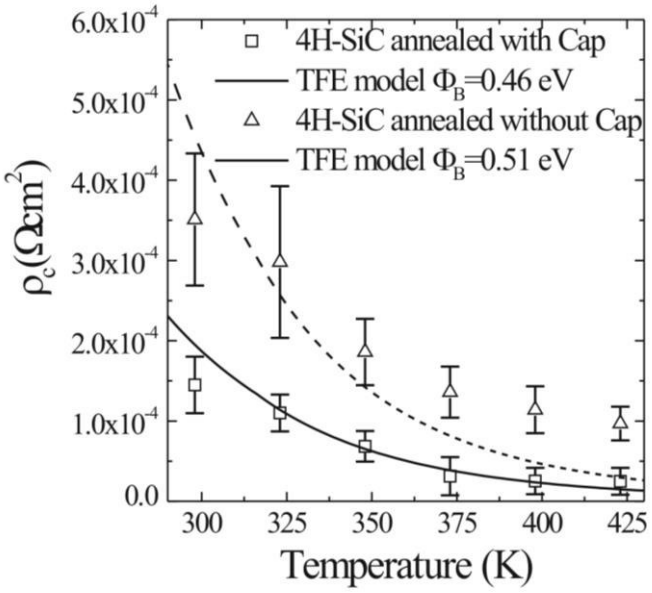


Figure 3. 9: *Specific contact resistance ρc as a function of the measurement temperature for alloyed Ti/Al contacts formed on 4H-SiC implanted at high-dose and annealed at 1700°C "**with**" and "**without**" capping layer. The fits obtained using TFE model for the both samples implanted at high dose and annealed at 1700 °C "**with**" and "**without**" protective capping layer are also reported.*

First of all, it can be observed that the values of ρ_c for the Ti/Al Ohmic contacts formed on 4H-SiC surfaces implanted and annealed with capping layer are lower than those measured in the samples without capping layer in the entire examined temperature range. Moreover, in both cases the specific contact resistance ρ_c decreases with increasing measuring temperatures *T*. In particular, for Ti/Al contacts formed on capped 4H-SiC surface, ρ_c decreased from 1.45×10^{-4} Ωcm^2 at room temperature to 2.49×10^{-5} Ωcm^2 at 150°C. On the other hand, for the Ti/Al contact formed on the uncapped 4H-SiC ρ_c decreased from 3.51×10^{-4} Ωcm^2 to 9.69×10^{-5} Ωcm^2 in the same temperature range.

According to the classical treatment, the dominant carrier transport mechanism in metal/semiconductor interface depends on the doping density of the semiconductor *N*, and is related to a characteristics energy E_{00} defined by [53]:

$$E_{00} = \frac{h}{4\pi}\left(\frac{N}{m^{*}\varepsilon}\right)^{\frac{1}{2}} \qquad \textbf{(3.11)}$$

where h is the Planck's constant, m^* is the hole effective mass and ε the dielectric permittivity of SiC.

E_{00} gives the relationship between the temperature T and the semiconductor net doping ($N = N_A - N_D$). The ratio kT/qE_{00} quantifies the ratio between the thermionic emission (TE) current and other contributions like the thermionic field emission (TFE) or the field emission (FE) one. A comparison of the thermal energy kT with E_{00} calculated for our doping levels and temperature range leads to $kT/qE_{00} \approx 0.86 - 1$. Hence, TFE can be assumed to be the dominant carrier transport mechanism.

According to the TFE model, the specific contact resistance can be expressed as [53,54]:

$$\rho_C = \left(\frac{1}{qA^*}\right)\frac{k^2}{\sqrt{\pi(\phi_B + V_n)E_{00}}}\cosh\left(\frac{E_{00}}{kT}\right)\times\left[\sqrt{\coth\left(\frac{E_{00}}{kT}\right)}\right]\exp\left(\frac{\phi_B + V_n}{E_0} - \frac{V_n}{kT}\right) \quad \textbf{(3.12)}$$

where

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right) \quad \textbf{(3.13)}$$

In the equation (3.12) A^* is the Richardson constant and V_n the energy difference between the conduction band edge and the Fermi level.

The experimental data, reported in figure 4 were fitted using the expression of the TFE model, and the Schottky barrier height Φ_B and the doping concentration N were considered as fit parameters. Since the experimental results showed in the previous paragraph indicated that the average electrical properties of the implanted layer are almost independent on the use of the capping layer, a reasonable physical assumption is to consider the same value of N for both cases. Basing on this assumption, the experimental data for the two cases were fitted simultaneously, imposing constrain of having the same parameter N.

For our calculation we used the values of $\varepsilon = 9.7\varepsilon_0$, ε_0 being the permittivity of free space, $A^* = 146$ A/cm^{2}K [55], and $m^* = 0.91\ m_0$ [56], with m_0 the electron mass.

For the sample annealed with capping layer a good fit of the experimental data was obtained using the TFE model, from which the values of $N=(2.0\pm0.1)\times10^{19}$ cm^{-3} and $\Phi_B=(0.46\pm0.01)$ eV were determined.

The value of N determined by the fit with the TFE model, that corresponds to an electrical activation of the dopant of around 20%, is in good agreement with previous experimental measurements of Al electrical activation in 4H-SiC obtained under similar doping conditions [57]. Few works reported the experimental values of the barrier height for Ti-Al based contacts to p-type implanted 4H-SiC, and these values critically depend on the contact formation conditions (e.g., metal thickness, deposition technique, doping and annealing conditions). As an example, using temperature dependent TLM measurements Scorzoni *et al*. [58] found a value of $\Phi_B=0.82$ eV on p-type ion implanted 4H-SiC for a doping concentration of 4×10^{19} cm-3, while Crofton *et al.* [59] modeled the dependence of ρc on N_A assuming a barrier height of 0.37 eV. None of them, however, considered the incomplete activation of implanted Al.

By applying the TFE model considering the same doping concentration N, also for the sample annealed without capping layer, a higher Schottky barrier height ($\Phi_B=0.51\pm0.01$) eV was determined.

On the basis of this analysis, it can be concluded that TFE is the dominant transport mechanism in our Ti/Al Ohmic contacts. Furthermore, the reduction of the specific contact resistance, observed in the sample annealed with the capping layer, can be associated to a lowering of the Schottky barrier from 0.51 eV to 0.46 eV. However, it cannot be ruled out that local differences in the electrical activation of implanted Al-ions in the near-surface region occurring when using a capping layer, observed by scanning probe microscopy measurements in the absence of metal contacts [57], can play a role in the improvement of the values of ρ_c. Furthermore, the deviations of the experimental data from model can be associated to the presence of an inhomogeneous metal–SiC interface, not considered in the classical TFE mechanism.

3.7 Microstructure of Ti/Al Ohmic contacts

In order to explain the different electrical behavior and to corroborate the information gained from the temperature dependence of ρ_c, the microstructure of the samples was evaluated by XRD analysis combined with cross-sectional TEM investigation.

Figure 3.10 shows XRD patterns of Ti/Al contact after annealing at 950 °C for the sample at high dose with capping layer. The main feature that can be deduced from the XRD patterns is the formation of a ternary compound Ti_3SiC_2 and of the Al_3Ti phase and the presence of unreacted Al.

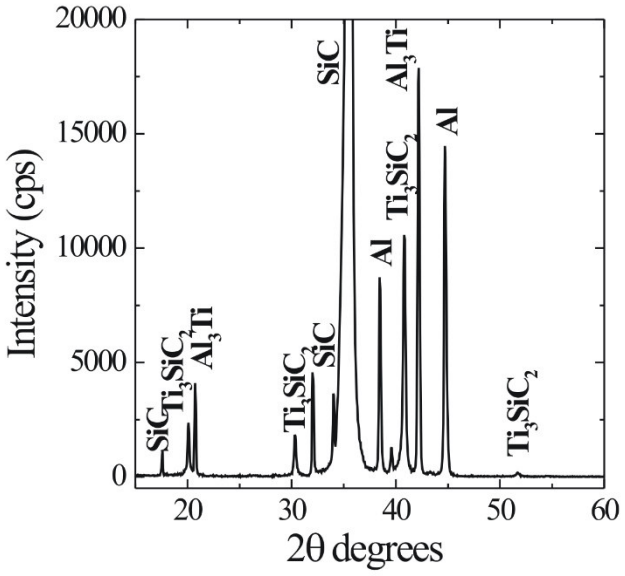


Figure 3. 10: *XRD analysis of a Ti/Al contact after annealing at 950 °C formed on implanted 4H-SiC*

The same phases were observed in the sample annealed without capping layer (not shown). The phases observed by XRD in the alloyed contacts are in agreement with the predictions of the phase diagram of the Al-C-Ti-Si quaternary system, which indicates the coexistence of Ti_3SiC_2 and other compounds (like Al_4C_3 or Al_3Ti) upon annealing at 1000°C [60]. The presence of Al_4C_3, experimentally observed by Johnson et al [10], has not been detected in our samples, probably due to different annealing conditions.

Cross section TEM analysis, allowed the evaluation of contacts microstructure in the proximity of the interface, being relevant to understand the electrical properties

determined by TLM analysis. *Figures 11(a)* and *11(b)* show the cross sectional TEM micrographs for samples implanted at high dose and annealed at 1700°C without and with a capping layer, respectively.

The combination of XRD (*Figure 3.10*) and Energy Filtered TEM (EFTEM) analysis (this latter not shown in this wok) allowed to identify the elemental composition of the grains inside the reacted metal layer. The brighter regions in the TEM micrographs have been generically indicated as "Al-rich regions", since the chemical analysis showed a predominance of Al, without the possibility to rule out the presence of small amount of Ti. Hence, according to the XRD analysis, inside these regions both pure Al and Al_3Ti may coexist. Furthermore, the ternary phase Ti_3SiC_2 is observed in both samples, resulting from the interaction of Ti with SiC at such high temperatures [60].

However, while in the sample without capping layer (*Figure 3.11a*), large Ti_3SiC_2 grains are located close to the interface with SiC and interrupted by small Al-rich regions, in the sample with capping layer (*Figure 3.11b*), larger Al-rich regions are found, in some parts forming an almost continous interfacial layer.

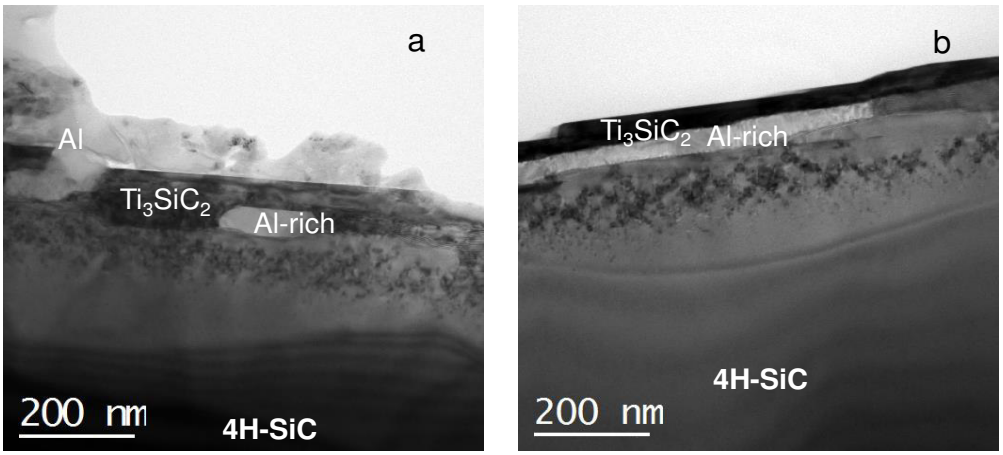


Figure 3. 11: *Cross sectional TEM micrographs of the interfacial region for samples implanted at high dose and annealed at 1700°C "**without**" capping layer **(a)** and "**with**" capping layer **(b)**.*

Large agglomerates, already observed by AFM, were visible by TEM imaging in some places on the contact surface, and can be due to an excess of liquid Al, frozen when cooling down the samples after annealing. Below the metal/SiC interface, a high density

of extended defects can be observed, which was likely formed as a result of the high dose implant followed by high temperature annealing. The presence of these defects is one of the causes of the high sheet resistance measured in the implanted material.

Evidently, TEM analysis has showed a strongly inhomogeneous interface, where the interfacial morphology and microstructure are affected by the roughness of the implanted SiC. Although Ti was originally in contact with SiC, annealing of the contacts resulted in the formation of Ti_3SiC_2 interrupted by Al-rich regions. On the other hand, Tsukimoto *et al.* [34] found an irregular surface and interface morphology of the annealed Ti/Al system, attributing them to an anisotropic growth process of hetero-epitaxial Ti_3SiC_2 layers onto off-axis SiC layers. However, the ternary phase totally covered the area of the SiC substrate in their case. An inhomogeneous interfacial microstructure, similar to that of our samples, was found also by Parisini *et al.* [61], who detected the presence of titanium compounds and Al or Al_3Ti agglomerates, but did not report any correlation with the electrical measurements.

3.8 Ohmic contacts for MOSFETs devices

In order to simplify the device processes, Ohmic contacts with the same metal layer on both n- and p-type are required to fabricate MOSFETs devices.

Indeed, the device fabrication as well as its layout will be extremely simplified by forming Ohmic contacts with a single metal deposition and a unique post-annealing technique (for n- and p-type regions).

In particular, Nichek Silicide (Ni_2Si) can be used to form good Ohmic contacts on n-type SiC and, can form also reasonable contacts on heavily p-type SiC layers. Hence, Ni_2Si can significantly improve the fabrication process and the layout of a MOSFETs (acting as contact for source, drain and body regions).

It is known that the formation of low resistance Ohmic contact to n-type SiC is achievable using Ni and the specific contact resistance values in the range of $\rho_c \sim 10^{-6} \Omega cm^2$ can be obtained after the Nickel silicide (Ni_2Si) formation.

Using the standard Ni contacts also for p-type, typical values obtained are reported in *Table 3.6*:

	Without Cap	With Cap
ρ_c of Ti/Al	$1.45\times10^{-4}\ \Omega cm^2$	$3.51\times10^{-4}\ \Omega cm^2$
ρ_c of Ni_2Si	$1.87\times10^{-3}\ \Omega cm^2$	$1.40\times10^{-3}\ \Omega cm^2$

Table 3. 6: *Specific contact resistance ρ_c of alloyed Ti/Al and Ni_2Si contacts to p-type SiC for different annealing conditions.*

It must be pointed out that alloyed Ti/Al contacts enabled an improvement of ρ_c with respect to nickel silicide (Ni_2Si) contacts. In this latter case, almost no dependence of ρ_c on the use of a capping layer (ρ_c ~ 1.4-1.9×10^{-3} Ωcm^2) was observed, since the formation of Ni_2Si is associated to the consumption of part of the SiC surface [62].
Surely, to simplify the device fabrication processes a single material is necessary. Therefore this approach was successfully applied to both lateral and vertical MOSFET on 4H-SiC for the remaining experiments. In particular, in chapters 4 and 5, the Ohmic contacts on both the p- and n-type implanted regions of the devices have been fabricated using Ni_2Si.

3.9 Conclusion

In summary, in this chapter the carrier transport mechanism in alloyed Ti/Al Ohmic contacts to p-type Al-implanted 4H-SiC was modelled considering transport mechanism at inomogeneous interfaces. It has been shown that the morphology of implanted SiC after high temperature (1700°C) annealing strongly influences both the surface flatness and the electrical characteristics of alloyed Al/Ti Ohmic contacts formed on it. In particular, improving the SiC surface morphology using a protective cap during post-implantation annealing resulted in a reduction of the roughness even if a uniform interface, similar to epitaxial substrates, cannot be achieved. Anyway a lowering of the specific resistance ρ_c of alloyed Ti/Al Ohmic contacts was achieved. This result could not be correlated to macroscopic electrical properties of the implanted layer, that were independent of the surface conditions. However, the temperature dependence of the ρ_c has indicated that thermionic field emission is the dominant transport mechanism through the metal/SiC interface, and that a reduction of the barrier

height occurs in the contacts formed on smoother SiC surface and explains the lower specific contact resistance. As a matter of fact, TEM analysis shows an inhomogenous interface, different in the two cases, which can justify the different macroscopically measured Schottky barrier heights.

The practical implications of an improved Ohmic contact morphology and specific contact resistance, with respect to the possible applications to SiC device processing and performances have been discussed.

3.10 References

[1] S.M.Sze, *Physics of Semiconductor Devices*, 2nd Ed., John Wiley & Sons, New York 1981.

[2] G. Pensl, F. Ciobanu, T. Frank, M. Krieger, S. Reshanov, F. Schmid, M. Weidner, *SiC Materials and Devices*, **vol. 1**, 1 – 41, M. Shur, S. Rumyantesev and M. Levinshtein eds, World Scientific, Singapore, (2006).

[3] F. Roccaforte, F. Giannazzo, V. Raineri, *J. Phys. D: Appl. Phys*. **43**, 223001 (2010).

[4] F. Roccaforte, F. La Via, V. Raineri, *International Journal of High Speed Electronics and Systems*, **15 (4)**, 781-820 (2005).

[5] I. P. Nikitina, K. V. Vassilevski, N. G. Wright, A. B. Horsfall, A. G. O'Neill and C. M. Johnson, *J. Appl. Phys*. **97**, 083709 (2005).

[6] S. Y Han, K. H. Kim, J. K. Kim, H. W. Jang, K. H. Lee, N K. Kim, E. D. Kim, J. L. Lee, *Appl. Phys. Lett.* **79**, 1816-1818 (2001).

[7] F. Roccaforte, F. La Via, V. Ranieri, L. Calcagno, P. Musumeci, *Appl. Surf.Sci.* **184**, 295-298 (2001).

[8] F. La Via, F. Roccaforte, A. Makhtari, V. Raineri, P. Musumeci, L. Calcagno *Microelectronic Engineering* **60**, 269–282 (2002).

[9] J. Crofton, P. G. McMullin, J. R. Williams, M.J. Bozack, *Appl. Phys. Lett.* **77**, 1317-1319 (1995).

[10] B.J. Johnson, M.A. Capano, *J.Appl. Phys*. **95**, 5616-5620 (2004).

[11] N.A. Papanicolau, A. Edwards, M.V. Rao, W.T. Anderson, *Appl. Phys. Lett*. **73**, 2009-2011 (1998).

[12] J.R. Waldrop, *J.Appl. Phys*., **75** 4548-4550 (1998).

[13] Y. Luo, F. Yan, K. Tone, J. Zhao, and J. Crofton, in *Silicon Carbide and Related Materials 1999* (Trans Tech Publications, Zuricho), **338–342**, 1013–1016, (2000).

[14] N. Lundberg and M. Ostling, *Solid-State Electron.* **39**, 1559 (1996).

[15] S. Lee, C. Zetterling, E. Danielsson, M.Ostling, J. Palmquist, H. Hogberg, and U. Jansson, *Appl. Phys. Lett.* **77**, 1478 (2000).

[16] S.-K. Lee, C.-M. Zetterling, M. Ostling, J.-P. Palmquist, and U. Jansson, *Microelectron. Eng.* **60**, 261 (2002).

[17] J. Crofton, P. A. Barnes, J. R. Williams and J. A. Edmond *Appl. Phys. Lett.* **62**, 384 (1993).

[18] J.C. Viala, N. Peillon, F. Bosselet, J. Bouix, *Materials Science and Engineering* **A229 95-113**, (1997).

[19] K.V. Vassilevski, G. Constantinidis, N. Papanicolaou, K. Zekentes, I.P. Nikitina, A.I. Babanin, *Materials Science Forum* **338-342**, 1017-1020 (2000).

[20] J. Crofton, L. Beyer, J. R. Williams, E.D. Luckowski, S.E. Mohney, *Solid-State Electronics* **41**, 1725-1729 (1997).

[21] F. Moscatelli, A. Scorzoni, A. Poggi, G.C. Cardinali, R. Nipoti. *Semicond. Sci. Technol.* **18**, 554-559 (2003).

[22] V.A. Dmitriev, K. Irvine, M. Spencer, G. Kelner, *Appl. Phys. Lett.* **64**, 318-320 (1994).

[23] B.J. Baliga *Silicon Carbide Power Devices*, Singapore, World Scientific (2005).

[24] S. Mitra, M.V. Rao, N. Papanicolaou, K. Jones, O.W. Holland, R. D. Vispute, S.R. wilson, *J. Appl. Phys.* **95**, 69 (2004).

[25] F. Roccaforte, S. Libertino, F. Giannazzo, C. Bongiorno, F. La Via, V. Ranieri, *J. Appl. Phys*. **97**, 123502, (2005).

[26] M. Laube, F. Schmid, G. Pensl, G. Wagner, M. Linnarsson, M. Maier *J. Appl. Phys.* **92,** 549 (2002).

[27] N. S. Saks, A. K. Agarwal, S.-H. Ryu, and J. W. Palmour *J. Appl. Phys.* **90,** 2796 (2001).

[28] M. Rambach, A. J. Bauer, H. Ryssel *Phys. Stat. Sol. (b)* **245** (7), 1315 (2008).

[29] G. Brauer, W. Anwand, W. Skorupa, S. Brandstetter, C. Teichert, *J. Appl. Phys.* **99** 023523 (2006).

[30] F.Giannazzo, M. Rambach, D. Salinas, F. Roccaforte, V. Raineri *Mater. Sci. Forum* **615-617,** 457 (2009).

[31] K.V. Vassilevski, N.G. Wright, A.B. Horsfall, A. G. O'Neill, M.J. Uren, K. P. Hilton, A. G. Masterton, A. J. Hydes, C.M. Johnson *Semicond. Sci. Technol*. **20**, 271 (2005).

[32] R. Nipoti, F. Mancarella, F. Moscatelli, R. Rizzoli, S. Zampolli, M. Ferri *Electrochem. Solid-State Lett.* **13**, H432 (2010).

[33] J .Crofton, S. E. Money, J. R. Williams, T. Isaacs-Smith *Solid-State Electronics* **46,** 109 (2002).

[34] S. Tsukimoto, T. Sakai, T. Onishi, K. Ito, M. Murakami, *J. Electronic Materials* **34,** 1310 (2005).

[35] Z. Wang, M. Saito, S. Tsukimoto, Y. Ikuhara *Advaced Materials* **21**, 4966 (2009).

[36] K. Vassilevski, K. Zekentes, G. Constantinidis, N. Papanicolaou, Irina P. Nikitina, A.I. Babanin, Mat. Sci. Forum, 338-342, (2000) 1017.

[37] R. Konishi, R. Yasukochi, O. Nakatsuka, Y. Koide, M. Moriyama, M. Muratami, Mater. Sci. and Eng. B98 (2003) 286.

[38] H. W. Jang, S. Y. Kim, J-L. Lee, J. Appl. Phys. 94 (2003) 1748.

[39] G.K. Reeves, H.B. Harrison, *IEEE Electron Device Lett.* **3**, 111-113 (1982).

[40] S. E. Mohney, B. A. Hull, J. Y. Lin, J. Crofton *Solid-State Electronics* **46**, 689 (2002).

[41] L. Kolaklieva, R. Kakanakov, I. Avramova, T. Marinova *Mater. Sci. Forum* **556-557**, 725 (2007).

[42] S. Tsukimoto, K. Ito, Z. Wang, M. Saito, Y. Ikuhara, M. Murakami *Materials Transactions* **50,** 1071 (2009).

[43] D. K. Schroder *Semiconductors Materials and Device Characterization*, 3rd ed., New York, John Wiley & Sons, p. 135 (2006).

[44] F. La Via, G. Galvagno, F. Roccaforte, A. Ruggiero, L. Calcagno, *Appl. Phys. Lett.* **87**, 142105 (2005).

[45] K. Ito, S. Tsukimoto, M. Murakami *Science and Technology of Advanced Materials* **7**, 496 (2006).

[46] B. H. Tsao, S. Liu, J. Scofield *Mater. Sci. Forum* **457-460**, 841 (2004).

[47] G. Pensl, F. Schmid, F. Ciobanu, M. Laube, S. A. Reshanov, N. Schulze, K. Semmelroth, H. Nagasawa, A. Schöner, G. Wagner *Mater. Sci. Forum* **433 – 436**, 365 (2003).

[48] J. Pernot, S. Contreras, J. Camassel *J. Appl. Phys.* **98**, 023706 (2005).

[49] F. Giannazzo, F. Roccaforte, V. Raineri *Appl. Phys. Lett.* **91**, 202104 (2007).

[50] S. M. Sze, *Semiconductor Devices: Physics and Technology*, 2nd ed., New York, John Wiley & Sons Inc (2001).

[51] H. Matsuura, M. Komeda, S. Kagamihara, H. Iwata, R. Ishihara, T. Hatakeyama, T. Watanabe, K. Kojima, T. Shinohe, T. Arai *J. Appl. Phys.,* **96**, 2708 (2004).

[52] F. Iucolano, F. Roccaforte, A. Alberti, C. Buongiorno, S. Di Franco, V. Raineri *J. Appl. Phys.* **100**, 123706 (2006).

[53] F.A. Padovani, R. Stratton *Solid – State Electron* **9**, 695 (1966).

[54] A.Y.C. Yu *Solid-State Electronics* **13**, 239 (1970).

[55] F. Roccaforte, F. La Via, V. Raineri, R. Pierobon, E. Zanoni *J. Appl. Phys.* **93**, 9137 (2003).

[56]N.T. Son, P.N. Hai, W.M. Chen, C. Hallin, B. Monemar, E. Janzén *Phys. Rev. B* **61**, R10544 (2000).

[57] M.H. Weng, F. Roccaforte, F. Giannazzo, S. Di Franco, C. Bongiorno, M. Saggio, V. Raineri *Mater. Sci. Forum* **645-648**, 713 (2010).

[58] A. Scorzoni, F. Moscatelli, A. Poggi, G.C. Cardinali, R. Nipoti *Mater. Sci. Forum* **457-460**, 881 (2004).

[59] J. Crofton, L.M. Porter, J.R. Williams *Phys. Stat. Sol. (b)* **202**, 549 (1997).

[60] J.C. Viala, N. Peillon, F. Bosselet, J. Bouix *Mat. Sci. Eng.,* **A229**, 95 (1997).

[61] A. Parisini, A. Poggi, R. Nipoti *Mater. Sci. Forum* **457-460**, 837 (2004).

[62] F. Roccaforte, F. La Via, V. Raineri, P. Musumeci, L. Calcagno, G.G. Condorelli, Appl. Phys. A **77,** 827 (2003).

Chapter 4
Channel mobility in 4H-SiC MOSFET

Interfaces and surfaces are fundamental aspects to reach the expected optimal performances in high power electronic devices. In particular, the SiO_2/4H-SiC interface is the main building block of a MOSFET. Its structural and electrical quality has a direct impact on the channel mobility and on the channel resistance component (and on the total device on-resistance).

In this chapter, the influence of the surface morphology and mechanism limiting the channel mobility in MOSFETs fabricated in Al-implanted 4H-SiC have been investigated. In particular, the mobility behavior was investigated for devices fabricated using two different post-implantation annealing (with and without a protective capping layer). Moreover, the temperature dependence of the channel mobility has showed that the Coulomb scattering is the main mechanism limiting the electron transport in the channel.

The electrical analyses were correlated with the microstructural investigations of the interface region SiO_2/4H-SiC.

4.1 Channel mobility: a critical issue for 4H-SiC MOSFETs

One the keys of the success of Si based MOS technology is the excellent interfacial characteristics between the silicon and its native thermal oxide. In Si/SiO_2 interface, the oxide and interfacial traps can be erased with simple and adequate post oxidation annealing and the traps can be generally neglected. Conversely, a high density of interface states is typically measured in SiO_2/SiC interfaces, most probably due to the presence of carbon cluster, silicon sub-oxide bonds or intrinsic defects in the near – interfacial oxide layers [1,2]. These interface states have been indicated as the origin of the commonly observed low channel mobility in SiC MOSFETs [3].

It has been reported that the interface trap density at the SiC/SiO_2 interface ranges from 10^{11} to $10^{13} cm^{-2}eV^{-1}$ [3], while the interface trap density of Si/SiO_2 is 10^9 $cm^{-2}eV^{-1}$. The higher interface trap density results in lower inversion channel mobility of MOSFETs. It is unclear whether the worse interface quality comes from the intrinsic SiC/SiO_2 system or the thermal oxidation process. However, in the last 20 years, to mitigate the mobility

problem, different post-oxidation annealing (POA) of the gate oxide have been explored. Among them, annealing in NO and N_2O ambient resulted the most efficient to provide channel mobility values in the range of 20 – 50 $cm^2V^{-1}s^{-1}$ [4,5,6,7,8] and to considerably improve the devices performances.

Even higher values (up to 150 $cm^2V^{-1}s^{-1}$) were achieved using annealing in alumina furnaces or in phosphorus oxychloride ($POCl_3$) ambient, but they introduce an undesired high density of mobile charges in the gate oxide, thus preventing their practical use for devices [9,10, 11]. An additional issue in vertical 4H-SiC power MOSFETs is related to the selective doping by ion- implantation (used for the formation of source, drain and body regions). These processes, however, require high temperature post-implantation annealing (up to 1800 °C for the p-type layers) for electrical activation of the dopant species [12,13,14,15], which can degrade the surface channel morphology. In this case, the surface can be preserved during post implantation annealing with a carbon capping layer [16,17,18]. This aspect was already discussed also for the Ohmic contacts in chapter 2.

The effect of these post implantation annealing treatments on the channel mobility remains controversial. In particular, *Haney et al.,*[19] observed that the channel mobility is not significantly affected by post-implantation annealing in the range 1200 °C - 1800 °C, using capping layer. On the other hand, *Naik et al.* [20] recently reported that the process with a carbon capping layer leads to a lower inversion electron mobility, pointing out that interfacial traps are not the limiting scattering mechanism, but rather that an increased surface roughness induced by the cap is responsible for the lower mobility. Occasionally, in the presence of a pronounced “step bunching”, an anisotropy of the drain current was observed and ascribed to the different interface roughness appearing to the carriers in the different directions [21].

Clearly, understanding the impact of post-implantation treatments on MOSFETs performances still remains a critical and open issue.

For all these reasons, an important part of this thesis was focused on the mechanisms limiting the channel mobility in implanted 4H-SiC MOSFETs, comparing two different post-implantation annealing (*with* and *without* a protective carbon capping layer).

4.2 *Lateral MOSFET: mobility and threshold voltage*

In *Chapter 2* the channel resistance (R_{CH}) has been recognized as one of the main contributors to the R_{DSon} of SiC MOSFETs. The channel resistance, in turn, depends on the value of the channel mobility. However, the series resistance of a vertical power MOSFETs is composed by different contributions, and it is not simple to isolate the contribution of the channel resistance. Therefore, in this thesis *lateral MOSFETs* were studied as test vehicles to extract the channel mobility and to study the limiting mechanisms to the carriers transport. In general, for an appropriate geometry, the resistance of a lateral MOSFET is almost uniquely determined by the channel resistance, provided that the source-drain contact resistance is negligible (long channel). In *Figure 4.1* the schematic cross section of lateral n-MOSFET (a) and the schematic diagram (b) are reported. Length and width of the channel are indicated with *L* and *W*, respectively.

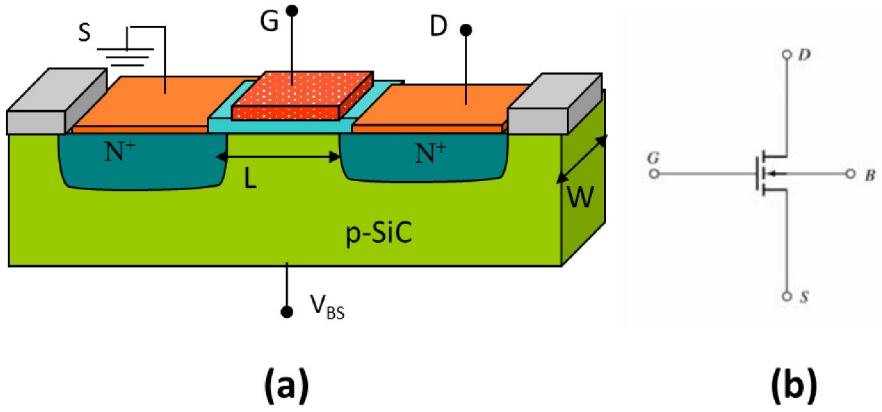


Figure 4. 1: *Schematic cross section of lateral n-MOSFET* ***(a)*** *and the MOSFETs electrical schematic diagram* ***(b).***

In this structure S, G, D and B are source, gate, drain and body terminal, respectively. The two N^+ zones, called source and drain, are heavily doped by ion-implantation. The body region instead is a P-type implanted layer with a lower doping. The current flows between source and drain layer in the body region forming the channel region.

A metal electrode is deposited onto the gate oxide layer. Ohmic contacts are formed on the source, drain and body regions, typically by metal deposition followed by thermal annealing.

The working mechanism of the MOSFETs is not complicated. If no voltage is applied to the gate, no current flows from source to drain, because a reversed biased p-n junction blocks any electron flow, no matter the polarity of the source-drain voltage. However, if gate voltage is not zero, the situation will be different. As can be seen in *Figure 4.1*, the body is p-type semiconductor material; therefore negative gate voltage will make holes accumulate at the oxide-semiconductor (O/S) interface, and current cannot flow along the interface in the p-type semiconductor. However, when positive voltage is applied on gate, holes are repelled from the O/S and electrons simultaneously will move up to the interface. This movement creates a depletion layer. With more positive voltage applied, the surface of the semiconductor inverts to produce an n-type channel that connects the S/D regions of the device. If a voltage exists between the source and drain terminals, a current flow will be observed. Generally, the source terminal is grounded and voltage is applied to the drain terminal. The voltage and corresponding current are called drain voltage and drain current, respectively, or simply V_D and I_D. Gate voltage is noted by V_G [22].

The voltage applied to the gate to create the n-channel is an important quantity, called threshold voltage, V_{TH}. Simply speaking, the MOSFET will conduct if $V_G > V_{TH}$. Above V_{TH}, if a small drain voltage is applied, a current will flow from the source to the drain through the conductive channel proportional to the drain voltage. This is the *linear region* in the characteristic of a MOSFET (dashed line in the left in *Figure 4.2(a)*). As the drain voltage increases, the current does not increase linearly, because the channel conductivity decreases with the drain voltage. When the pinch-off point is reached, the current saturates and the effective channel length is reduced. This is the *saturation region* in the characteristic of a MOSFET (dashed line in the right in *Figure 4.2(a)*). Between the two dashed lines, there is the *non-linear region* [22].

In *Figure 4.2* simulated drain characteristics of a MOSFET *(a)* and a schematic of the three different conditions of operation *(b)* have been depicted.

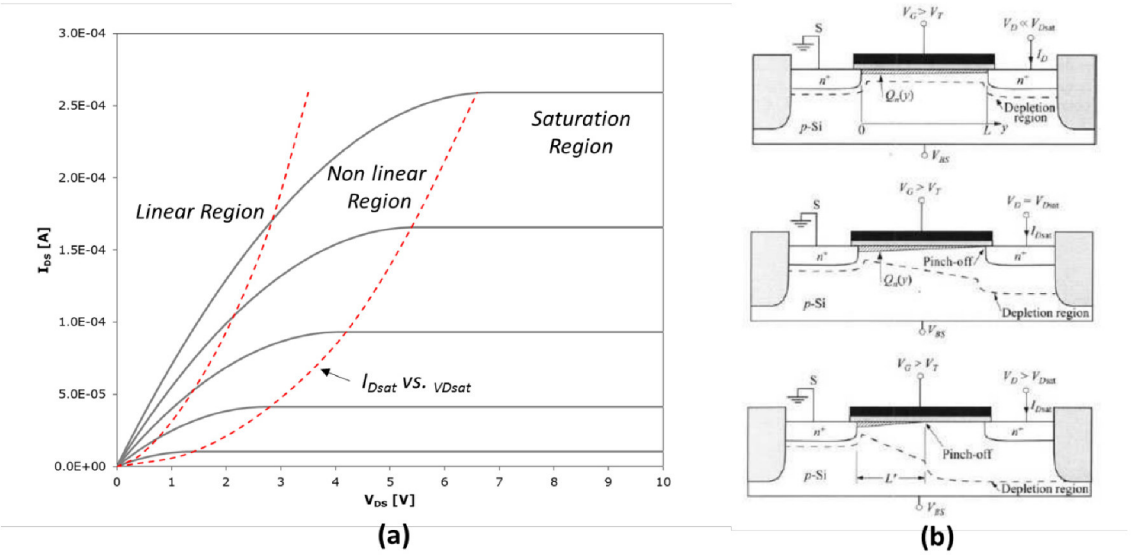


***Figure 4. 2**: (**a**) Simulated drain characteristics (I_D vs. V_D) of a MOSFET. The dashed lines separate the linear, non-linear and saturation region; (**b**) MOSFET operated in linear region (low V_D), at onset of saturation and beyond saturation.*

The current, for a channel of length L and width W, is continuous and constant and it is given by [22]:

$$I_D = \frac{W}{L}\int_0^L |Qn(y)|v(y)dy \qquad \textbf{(4.1)}$$

where $Q_n(y)$ is the inversion charge and $v(y)$ is the average carrier velocity. Integrating the equation (4.1) and assuming in the channel the carrier velocity constant, $v = \mathcal{E}\mu_n$ (with $\mathcal{E}$ and μ_n the constant electric field and channel mobility, respectively), the complete expression of drain current is:

$$I_D = \frac{W}{L}\mu_n C_{ox}\left\{\left(V_G - V_{FB} - 2\psi_B - \frac{V_D}{2}\right)V_D - \frac{2}{3}\frac{\sqrt{2\varepsilon_{Sic}\varepsilon_0 qN_A}}{C_{ox}}\left[(V_D + 2\psi_B)^{3/2} - (2\psi_B)^{3/2}\right]\right\} \textbf{(4.2)}$$

where C_{ox} is the oxide capacitance, V_{FB} is the flatband voltage that includes the effect of fixed charge, Q_{ox} and Ψ_B is the bulk potential.

This equation (4.2) explains clearly the *Figure 4.2(a)*: for a given V_G the drain current first increases linearly with drain voltage, then gradually levels off and finally approaches a saturated value.

In the *linear region*, for $V_D << (V_G - V_{TH})$, the equation **(4.2)** reduces to:

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_G - V_{TH} - \frac{V_D}{2}\right)V_D \approx \frac{W}{L}\mu_n C_{ox}\left(V_G - V_{TH}\right)V_D \qquad \textbf{(4.3)}$$

where the expression for threshold voltage is:

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{4\varepsilon_{SiC}\varepsilon_0 q N_A \phi_B}}{C_{OX}} \qquad \textbf{(4.4)}$$

Qualitatively, V_{TH} is the gate bias beyond flat-band just starting to induce an inversion charge sheet.

For the *saturation region* it is possible to obtain the equation for the saturation current:

$$I_{Dsat} = \frac{Z}{2ML}\mu_n C_{ox}\left(V_G - V_{TH}\right)^2 \qquad \textbf{(4.5)}$$

where M and K are functions of doping concentration and oxide thickness:

$$M = 1 + \frac{K}{2\sqrt{\psi_B}} \quad and \quad K = \frac{\sqrt{\varepsilon_{SiC}\varepsilon_0 q N_A}}{C_{ox}} \qquad \textbf{(4.6)}$$

Finally, the *non-linear region* between these extreme cases is:

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_G - V_{TH} - \frac{MV_D}{2}\right)V_D \qquad \textbf{(4.7)}$$

In a lateral n-MOSFET with a channel length, L, and width W, such as reported in *Figure 4.1*, two important parameters are the threshold voltage, expressed in the equation **(4.4)**, and the channel mobility. Both can be extracted from the I-V transfer characteristics.

The drain current I_D in the saturation region is expressed by the equation **(4.5)** and the drain current is directly proportional to $(V_G\text{-}V_{TH})^2$. Then, the equation **(4.5)** is equivalent to:

$$\sqrt{I_D} \cong \sqrt{\frac{W\mu_n C_{ox}}{2L}} V_G - \sqrt{\frac{W\mu_n C_{ox}}{2L}} V_{TH} \qquad \textbf{(4.8)}$$

Plotting the $\sqrt{I_D}$ versus V_G, in the region above the threshold (saturation region), it is possible to extract by means of a linear fit of the experimental data, the voltage V_{TH} from the coefficients of the fit:

$$\sqrt{I_D} \cong mV_G + q \quad \text{and} \quad V_{TH} = -\frac{q}{m} \qquad \textbf{(4.9)}$$

In *Figure 4.3* the $\sqrt{I_D}$ versus V_G plot and the linear fit to determine the threshold voltage are reported.

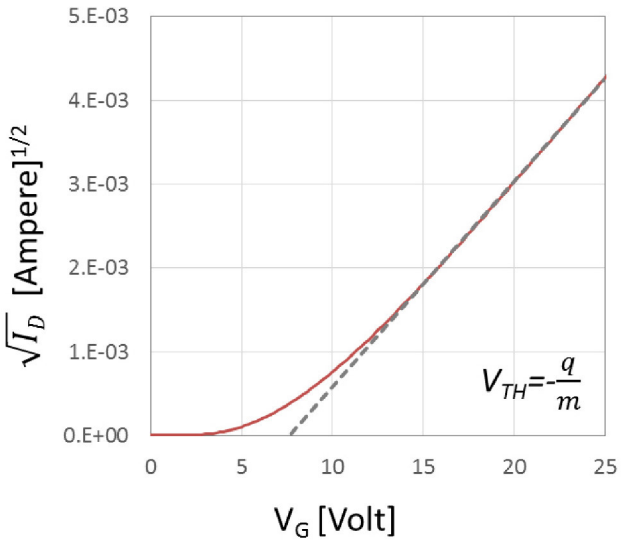


Figure 4. 3: *The $\sqrt{I_D}$ versus V_G plot and the linear fit to determine the Threshold Voltage V_{TH}.*

In the linear region the drain current is expressed by the equation **(4.3)**. In this relation μ_n is the channel mobility μ_{CH}. The channel mobility can be defined in two different ways [23].

The first approach is through the *effective mobility*, μ_{eff}. The effective mobility, usually measured at low drain voltage (50-100 mV), is determined by the drain conductance:

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=constant} \tag{4.10}$$

Therefore the effective mobility is given by the relation [23]:

$$\mu_{eff} = \frac{g_d L}{W C_{ox}(V_{GS} - V_{TH})} \tag{4.11}$$

The conductance g_d can be obtained from the linear fit of the I-V characteristics of the MOSFET for small values of V_{DS}.

In the *Figure 4.4* the typical trend of effective mobility versus V_G-V_{TH} is reported:

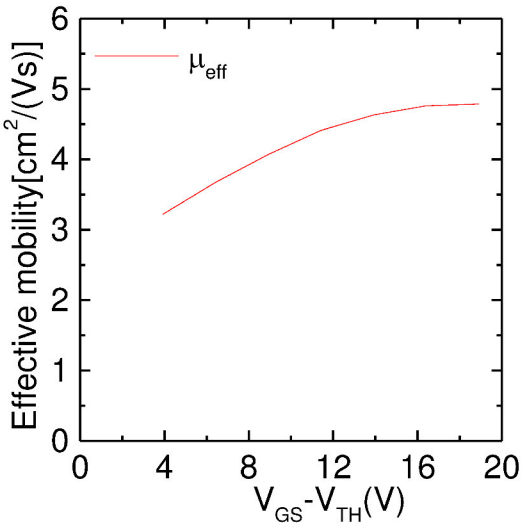


Figure 4. 4: *Effective mobility trend versus V_G-V_{TH}*

On the othe hand, the *field-effect mobility* is determined from the trasconductance, defined by:

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=constant} \tag{4.12}$$

gm is the derivation of the drain current as a function of the gate voltage.
Considering the transfer characteristics in the linear region (low V_D ~ 200mV), such as reported in *Figure 4.5 (a)*, the derivative is the trasconductance, *Figure 4.5 (b):*

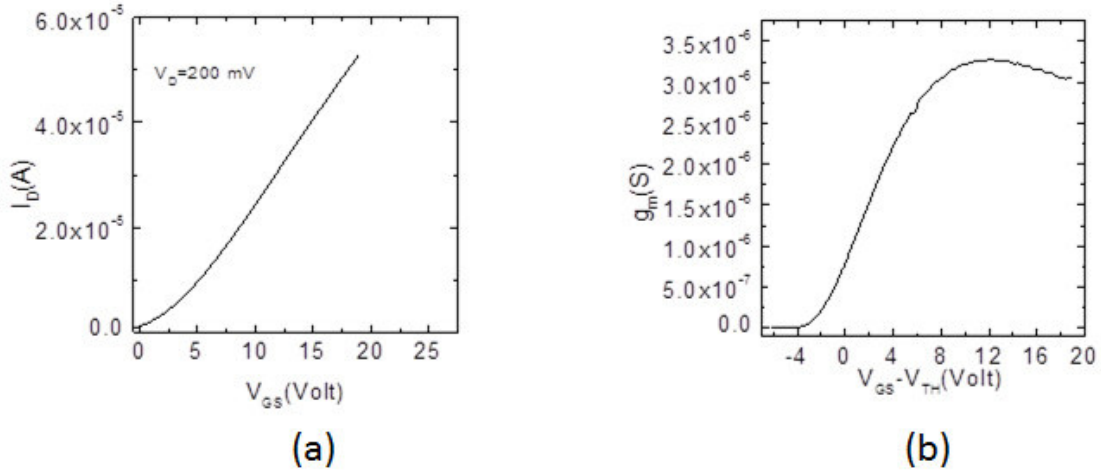


Figure 4. 5: (a) *Transfer characteristics in the linear region and* ***(b)*** *trasconductance, gm.*

In particular, the trasconductance is expressed by [23]:

$$g_m = \frac{W}{L}\mu_{ch}C_{ox}V_{DS} \tag{4.13}$$

Solving this equation respect to the channel mobility we have:

$$\mu_{FE} = \frac{g_m L}{WC_{ox}V_{DS}} \tag{4.14}$$

The field effect mobility, defined by (4.14), is reported in *Figure 4.6* as a function of the gate bias:

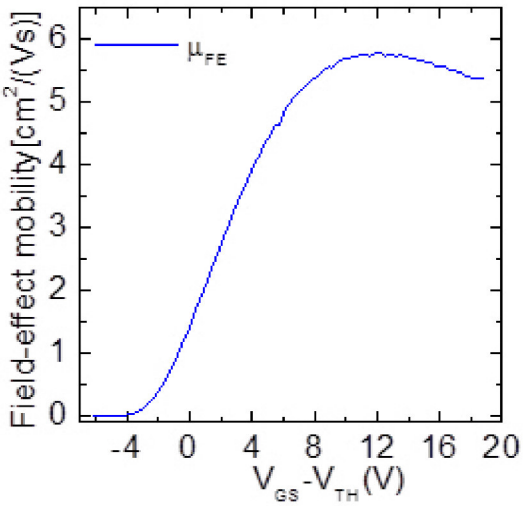


Figure 4. 6: *Field-effect mobility*

It can be observed the discrepancy between μ_{eff} and μ_{FE}. This difference is due to the neglect of the electrical field dependence of the mobility in the derivation of the equation (4.14) [23].

Therefore, the field-effect mobility μ_{FE} is a figure of merit for comparing device performance and is typically used to describe 4H-SiC MOSFETs.

In this chapter, when channel mobility is extracted, we refer always to the *field-effect mobility*.

4.3 Fabrication of 4H-SiC lateral MOSFETs

This paragraph describes fabrication steps and the experimental procedures used to realize the lateral n-MOSFET and MOS capacitors.

For this study, nitrogen doped (n-type) 4H-SiC epitaxial layers with doping concentration of 10^{16} cm^{-3}, grown onto heavily doped n^+-type substrate with a 4°-off axis misorientation toward <11-20> direction, were used. The processing steps were performed in R&D line at ST Microelectronics of Catania.

Figure 4.7 schematically reports the layout of the lateral n-MOSFET with a channel length L=40 µm and a width W=16 µm, used in this thesis.

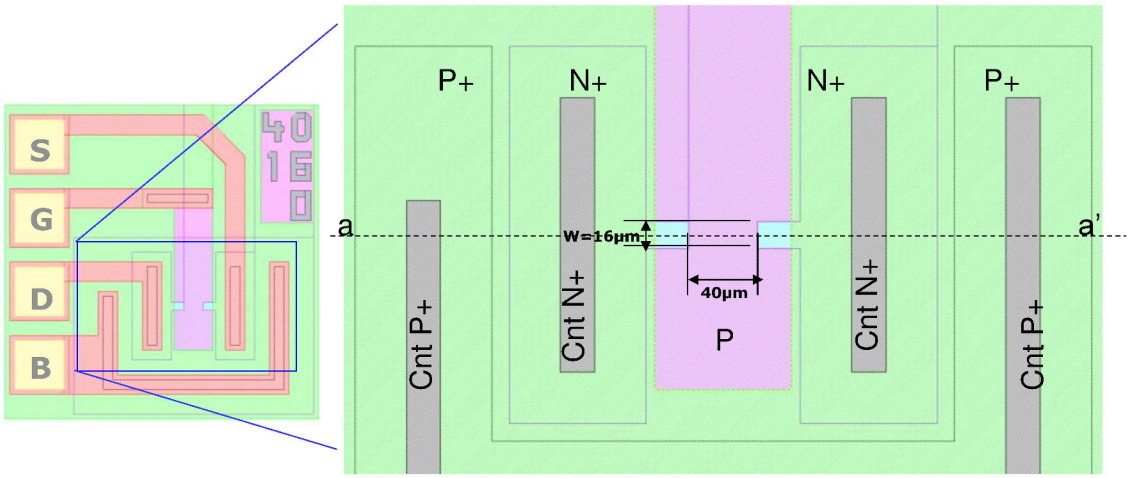


Figure 4. 7: *Layout of lateral n-MOSFET with a channel length L=40 µm and a width W=16 µm.*

The MOSFET has four distinct metal pads to electrically contact the structure (indicated with S, D, G and B in the left side of *Figure 4.7*. The dimension of the pads is 120 µm × 120 µm. In the right side of the *Figure 4.7* a zoomed view of the channel region of the device is shown.

A schematic cross section of the MOSFET device (along a-a' line of *Figure 4.7*) is reported in *Figure 4.8*.

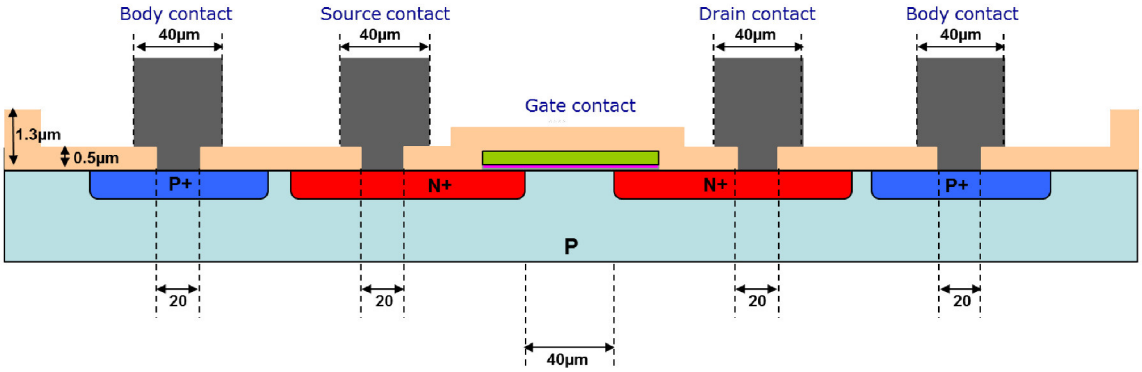


Figure 4. 8: *Schematic cross section of the lateral MOSFET device used in our experiments.*

Al implantation was used to create the body region with a doping concentration around $10^{17}cm^{-3}$, while the source and drain region were formed by heavy P-implantation. These implantations were followed by two different dopant activation annealing both at 1650 ºC, either *with* or *without* a protective carbon capping layer on the samples surface.

The main steps of the fabrication flow chart of the MOSFETs devices are reported in the *Table 4.1*:

Step	**Processes**	**Description**	
1	Wafer cleaning		
2	Photolithography for the formation of body region	Dielectric deposition and the definition of the body region	
3	Multiple ion implantation of Aluminum at high temperature (T = 400ºC)	Doping dose between 10^{12}-10^{13} cm^{-2} and the implantation energy varies from 30 keV to 400 keV.	
4	Photolithography for the formation of source/drain region	Dielectric deposition and the definition of the source/drain regions	
5	Heavy multiple ion implantation of Phosphorous at high temperature (T = 400ºC)	Doping dose between 10^{14}-10^{15} cm^{-2} and the implantation energy varies from 30 keV to 160 keV	
6	Photolithography for the formation of p-region at high temperature (T = 400ºC)	Dielectric deposition and the definition of the body region	
7	Multiple ion implantation of Aluminum	Doping dose between 10^{14}-10^{15} cm^{-2} and the implantation energy varies from 30 keV to 200 keV.	
8	Deposition of carbon capping layer in the wafer *with cap*	Photoresist	
9	Dopant activation annealing	*Without cap:* @1650 ºC in Ar +SiH_4	*With cap:* @1650 ºC in Ar
10	Removal of capping layer in the wafer	Low temperature oxidation process +	

	with cap	HF etch
11	Formation of gate oxide	Oxide deposition (th=300Å)
12	Post oxidation annealing	N_2O ambient T=1150 °C
13	Gate formation	Deposition of Polysilicon
		Photolithography and etch for the gate definition
14	Oxide deposition	Intermediate oxide formation
15	Photolithography for the formation of contacts of *body*, *source* and *drain*	Contacts definition
16	Formation of Nickel contacts on SiC	Sputter Ni (th=1000 Å)
		RTA 1000 ºC, 60" in N_2
		Unreacted Ni removal by HNO_3
17	Formation of contact on Polysilicon	Photolithography and etch for the polysilicon contact definition
18	Front metallization	Sputter of Ti/Al (th = 1000Å/3µm)
		Photolithography and etch of metal layers

Table 4. 1: *Schematic flow chart for the fabrication of lateral MOSFETs.*

In particular, the rows 8 and 10 have been integrated only in the wafer processed with capping layer. While the different doping activation (*with* and *without* cap) has been reported in the row 9.

The importance of Ohmic contacts on p-type regions has been pointed out in chapter 3. Therefore after the capping layer removal, the surface roughness of the p-type region, where the inversion channel forms, was monitored by the atomic force microscopy (AFM), measuring the surface heights distribution root mean square (RMS); the surface morphology was performed using a Digital Instrument D3100 equipment of the CNR-IMM laboratory. The RMS values are 0.36 nm and 1.75 nm, in the sample annealed *with* and *without* capping layer, respectively. In *Figure 4.9* the AFM scans of p-type 4H-SiC implanted regions are shown.

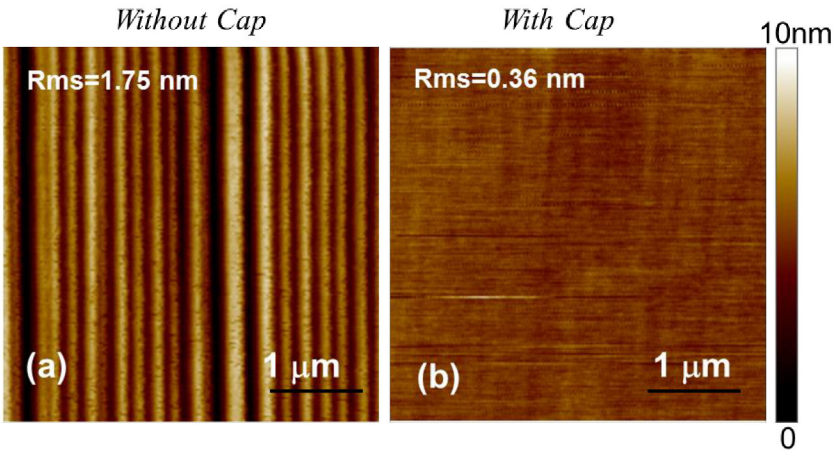


Figure 4. 9: *AFM images acquired in the surface of the p-type regions annealed* ***(a)*** *without and* ***(b)*** *with a protective carbon capping layer. The scans were performed after the capping layer removal.*

Then, a 30 nm-thick SiO_2 layer was deposited by plasma enhanced chemical vapour deposition as gate dielectric, followed by post-deposition-annealing at 1150 ºC in a N2O.

Finally, nickel silicide was used for Ohmic contacts for both p-type and n-type, formed by rapid thermal annealing at 950 ºC for 60 s.

Using the same flow, MOS capacitors have been realized simultaneously on the same wafers; they have been used (as we will see in the next paragraphs) to study electrically the quality of interface SiO_2/SiC.

The electrical characterization was performed in a Karl-Suss probe station using an Agilent B1500A parameter analyzer. The MOSFET characteristics were measured at different temperature in the range of 298-423 K, using Lakeshore 331 temperature controller connected to the chuck. The C-V measurements on the MOS capacitors were carried out at variable frequency in the range of 1 kHZ – 1 MHz. All of these measuring equipments are present in the ST Microelectronics laboratories of Catania.

4.4 *Electrical characterization of the lateral MOSFET*

First of all, the electrical characterization of the lateral MOSFET was performed in order to assess the mobility and the threshold voltage behaviour.

In a lateral MOSFET the I-V measurements were carried out in different points of the wafer. Here, we report the I-V curves that are representative of the experimentally observed trend over the wafer.

Figure 4.10 shows the typical I_{DS}-V_{DS} characteristics at room temperature for different values of the gate bias V_{GS} for 4H-SiC MOSFETs processed *with* (*red dashed line*) and *without* (*blue line*) a protective carbon capping layer during post-implantation annealing.

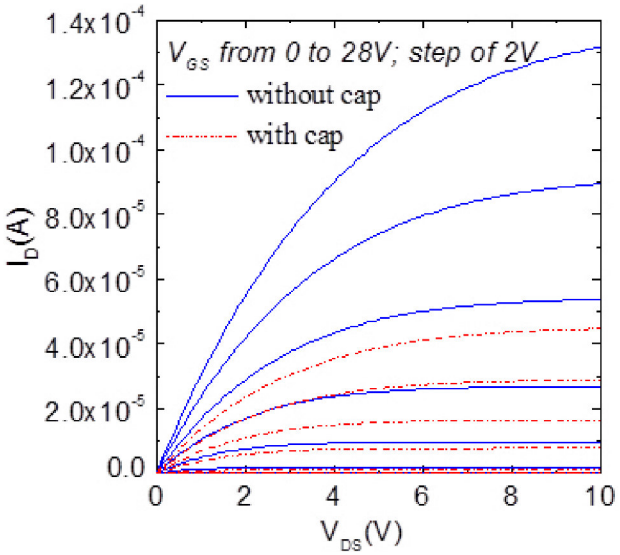


Figure 4. 10: *I_{DS}-V_{DS} characteristics of 4H-SiC MOSFETs processed with or without capping layer.*

As can be seen, a higher drain current is measured in MOSFETs processed without capping layer.

From transfer characteristics (I_D-V_G) of 4H-SiC lateral MOSFET in the linear region (at V_{DS} = 200mV), *Figure 4.11 (a)*, the channel mobility μ_{FE} was determined [23], using the relation **(4.14)**. The channel mobility for two different samples subjected to an annealing at 1650 ºC, is shown in *Figure 4.11 (b)*.

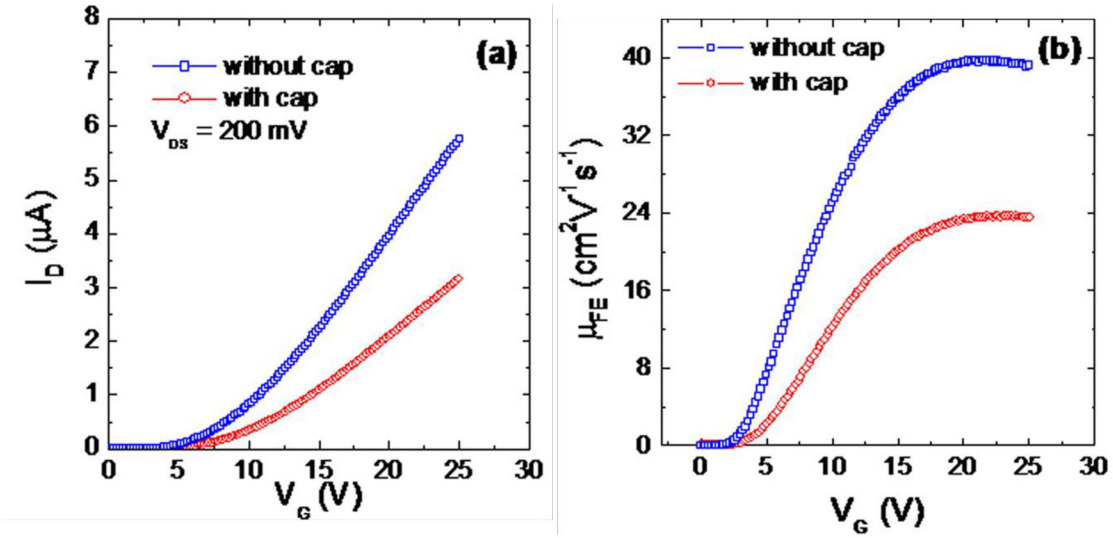


Figure 4. 11: *(**a**) Drain current (I_D) as a function of gate bias (V_G) for lateral 4H-SiC MOSFETs processed either with or without using capping layer during post-implantation high-temperature annealing; (**b**) Field effect mobility (μ_{FE}) as a function of V_G determined by the MOSFETs transfer characteristics for to different annealing conditions.*

Evidently, as expected from the current behaviour, the field effect mobility is higher in the device annealed without capping layer. In particular, the value of the peak mobility determined at room temperature were 40 and 24 $cm^2V^{-1}s^{-1}$, for the samples processed *without* and *with* capping layer, respectively.

Furthermore, considering the $\sqrt{I_D}$ versus V_G plot, in the *Figure 4.12*, a higher threshold voltage of 7.15 V was extracted for the device annealed with capping layer with respect to that annealed without capping layer of 6.28V, (the method used is described in the *paragraph 4.3*).

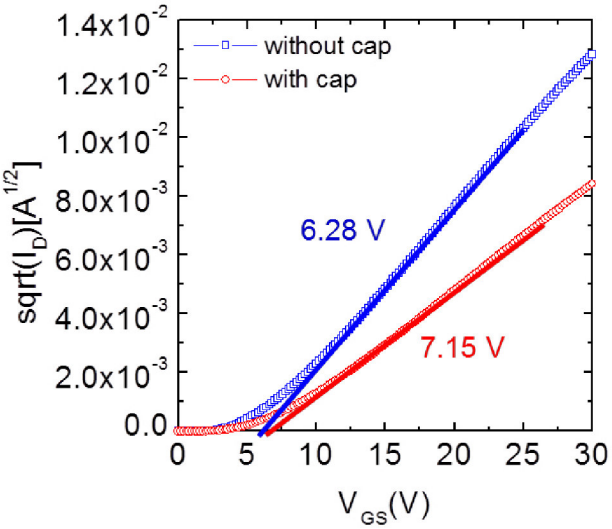


Figure 4. 12: *The $\sqrt{I_D}$ versus V_G plot for two different devices processed with (red dots) and without (blue squares) capping layer. In the figure also the linear fits are shown for two samples to extract the threshold voltage.*

Since a higher channel mobility (40 $cm^2V^{-1}s^{-1}$) is measured in the sample with the largest roughness (RMS = 1.75 nm), it can be inferred that the surface roughness scattering is not the limiting factor to the carrier transport in the channel. This hypothesis is consistent with recent results demonstrating that the electronics quality of the SiO_2/4H-SiC interfaces is not correlated to the miscut angle (i.e., to density of terraces determining the surface roughness), but is rather associated to the presence of carbon –related electronics states [24].

4.5 Temperature dependence of the channel mobility

To investigate the factors limiting the channel mobility, its temperature dependence has been studied in the range between 298 and 423 K for the two different samples. In *Figure 4.13*, the inversion channel mobility μ_{FE} is reported as a function of the temperature. In the entire temperature range the device processed with a capping layer exhibits a lower channel mobility than that of the sample processed without the capping layer. The mobility increases with increasing temperature, with a dependence proportional to $T^{+0.55}$ and $T^{+0.44}$ for the sample annealed with and without capping layer, respectively. This dependence suggests that the phonon-scattering is not the dominant degradation mechanism, as phonon-scattering mobility decreases with temperature.

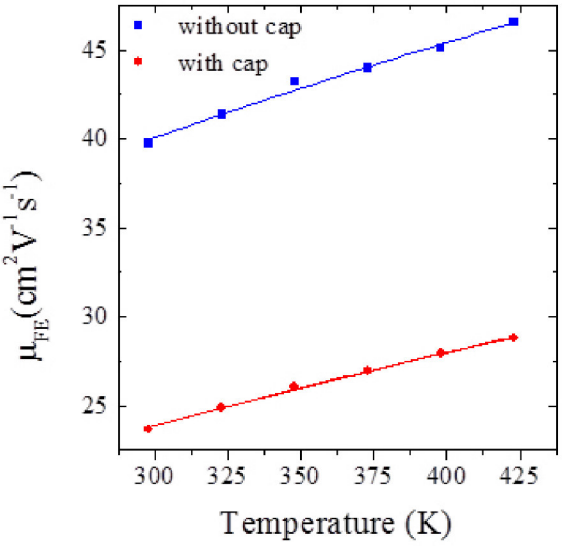


***Figure 4. 13**: Field-effect mobility μ_{FE} as a function of temperature T for 4H-SiC lateral MOSFETs annealed either with or without a capping layer.*

In order to consider different scattering phenomena and to explain the results, the experimental values of the mobility were compared with the values calculated considering the other possible scattering mechanisms.

According to the mobility model recently adapted by Pérez-Tomàs *et al.* [25] to the case of 4H-SiC, the total inversion layer mobility can be described by the combination of several factors:

$$\mu_{inv} = \left(\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right)^{-1} \qquad \textbf{(4.15)}$$

taking into account the bulk mobility factor (μ_B), the acoustic-phonon scattering (μ_{AC}), the surface roughness scattering (μ_{SR}), and the Coulomb scattering (μ_C) due to the presence of interface charges. The different contributions to the mobility for both samples were calculated using the material parameters given in Ref. [26] and are reported in *Figure 4.14* together with the experimental data.

In particular, in the temperature range 300-450K the bulk mobility μ_B decreases from 612 to 280 $cm^2V^{-1}s^{-1}$, while the acoustic-phonon scattering term μ_{AC} from 332 and 222 $cm^2V^{-1}s^{-1}$. It is worth noting that both terms depend on the material properties, but not

on the insulator/SiC interface [25]. The contribution to the surface scattering μ_{SR} was calculated using the experimental RMS values, determined by AFM analysis in the two cases (0.36 nm and 1.75 nm). Due to the dependence of this term on the reverse of the square of the roughness [27], in the sample without capping layer μ_{SR} is significantly lower than in the sample annealed with capping layer. Furthermore, μ_{SR} is only slightly dependent on the temperature in this range.

Since the measured mobility values (24 and 40 $cm^2V^{-1}s^{-1}$) are much smaller than the ones calculated considering the above mechanisms (exceeding 300 $cm^2V^{-1}s^{-1}$ in any case), it can be concluded that bulk-scattering, acoustic-phonon scattering and surface roughness are not the limiting factors for the carrier transport in the channel. As a matter of fact, all these contributions decrease with increasing temperature *T*, while the experimental mobility values increase with *T*.

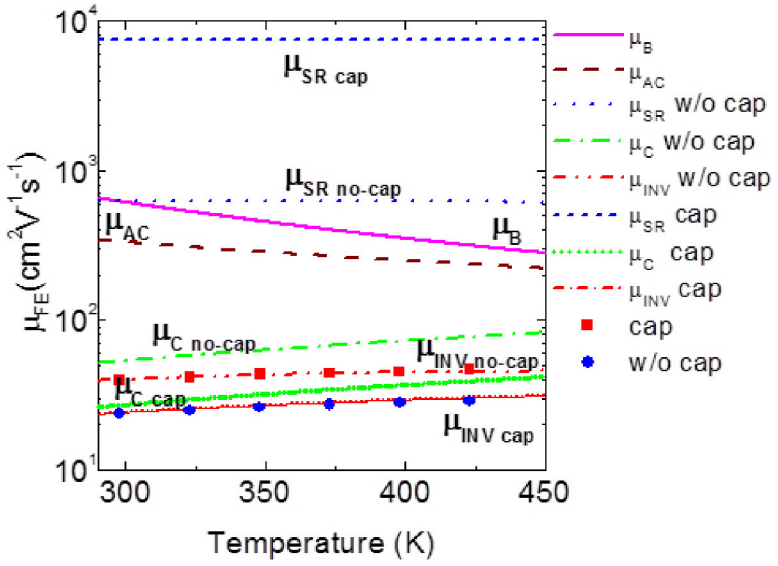


Figure 4. 14: *Inversion channel mobility contributions calculated considering the different scattering mechanisms as a function of the temperature. The experimental data for 4H-SiC MOSFETs annealed without capping layer and with capping layer are also reported.*

On the other hand, the temperature dependent Coulomb scattering term in equation *(4.16)* can be expressed as [28]:

$$\mu_C(T) = NT^{\alpha} \frac{Q_{inv}^{\beta}}{Q_{trap}} \quad \textbf{(4.16)}$$

where Q_{inv} is the inversion charge per unit area, β is an empirical coefficient, Q_{trap} is the trapped charge per unit area, T is the absolute temperature, α is a temperature coefficient and N is a proportionality constant [25]. For our calculation we used the literature values of $\alpha = 1$, $\beta = 1$ [29] and N = 7.525×10^{-3} $cm^2V^{-1}s^{-1}K^{-\alpha}$ [25].

Hence, the total inversion channel mobility curves were calculated with the complete expression reported in equation ***(4.16)***, using the interfacial trapped charges (Q_{trap}) in the Coulomb term μ_C as a free parameter in order to match the simulated curves with the experimental data points.

As can be seen, for both samples a good agreement between the simulated curves and the experimental data was obtained. In particular, from the simulation a higher density of trapped charges at the interface (Q_{trap}= $5\times10^{11}/cm^2$) was found for the device processed with the capping layer with respect to the device processed without cap (2.8×10^{11} $/cm^2$). This difference is qualitatively consistent with the variation of the threshold voltage of 0.87 V observed in the two samples. This result is also confirmed by the trend of the *sub-threshold swing S* extracted from the I_{DS}-V_{GS} curves showed in *Figure 4.15,* which is related to the interfacial quality [4, 23]. The sub-threshold swing, reported in equation (**4.17**), is another important device characteristic in the sub-threshold region, defined as the change in the gate voltage V_{GS} required to reduce the sub-threshold current by one decade.

$$S = \frac{dV_{GS}}{d(logI_D)} \quad \textbf{(4.17)}$$

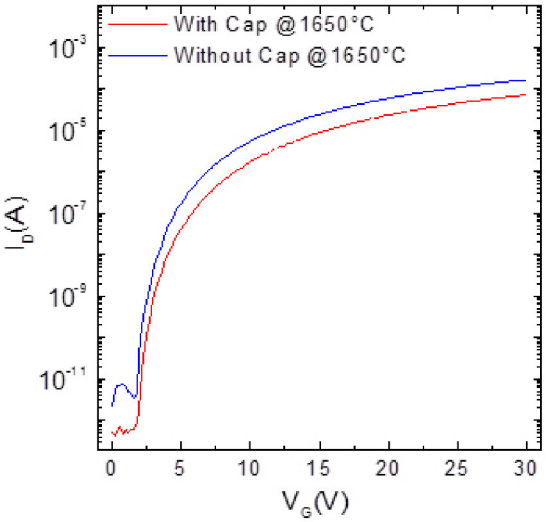


Figure 4. 15: *I_{DS}-V_{GS} curves in logarithmic scale, for the two devices processed with (red line) and without (blue line) a protective carbon capping layer, used to extract the sub-threshold swing.*

Fitting the I_{DS}-V_{GS} curves in the linear region, a value of S = 480 mV/decade was found in the device annealed *with* capping layer, larger than the value measured for the MOSFET annealed *without* capping layer (S = 390 mV/decade).
Recently, the inversion channel mobility degradation at SiO2/4H-SiC interfaces has been associated with the formation of an interfacial transition layer, characterized by an excess of carbon [30].

Hence, we monitored the quality of the samples by high resolution TEM analysis of the gate oxide/4H-SiC interface. The micrographs are shown in *Figures 4.16(a) and 4.16(b),* for the sample processed without and with the capping layer, respectively. As can be seen, in both cases, the images reveal an almost perfect structural quality of the interface region, since the atomic stacking of 4H-SiC is visible and no interfacial transition layer is visible. This result is in agreement with other literature works in which the formation of such interfacial disordered layer was not observed [31,32,33].

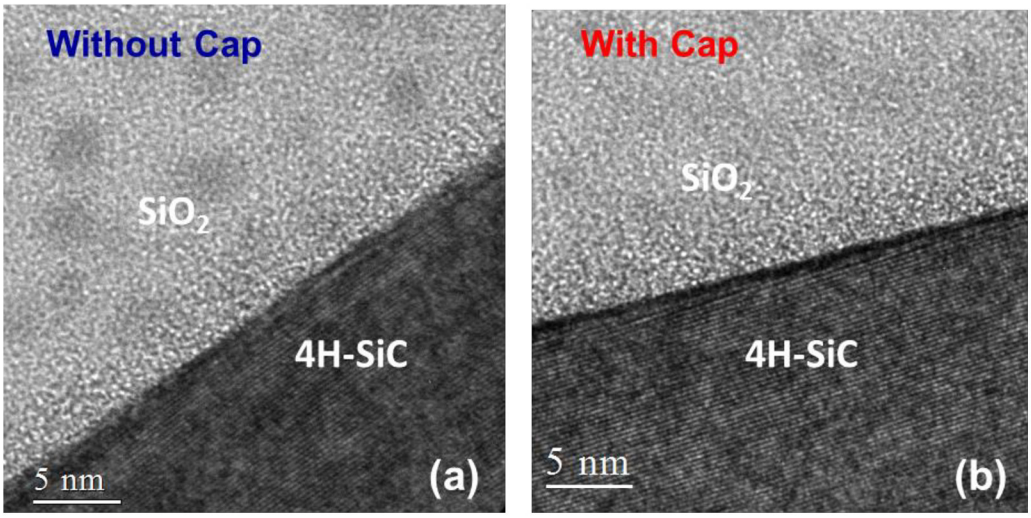


Figure 4. 16: *High resolution transmission electron microscopy images of the gate region (SiO2/4H-SiC interface) in the lateral MOSFET processed under the two different conditions. The images were taken along the [1-100] zone axis, which is perpendicular to the [0001] direction of 4H-SiC.*

The validity of the results was further confirmed by a direct measure of the density of the interface states (D_{it}), performed on n-type MOS fabricated in the same wafers (processed with or without the protective carbon capping layer). The measure of the density of the D_{it} has been performed using the conductance method [22]. In fact, measuring the D_{it} in n-type MOS capacitors is useful for understanding the mobility behaviour of n-channel MOSFETs, since electrons moving in the inversion layer are strongly affected by the interface states located near the conduction band edge.

Figure 4.17(a) shows the energy distribution of the interface state density for both the MOS processed protecting the semiconductor surface with the capping layer and without the capping layer, respectively. In both cases, the density of the interface states decreases when moving inside the band gap. The maximum D_{it} values are measured for both samples close to the conduction band edge and they are 3.6×10^{11} $cm^{-2}eV^{-1}$ and 7.2×10^{11} $cm^{-2}eV^{-1}$ for the sample treated without and with the capping layer, respectively. Furthermore, in *Figure 4.17(b)*, the measured C-V characteristics for the two samples are compared to the calculated ideal C-V curve.

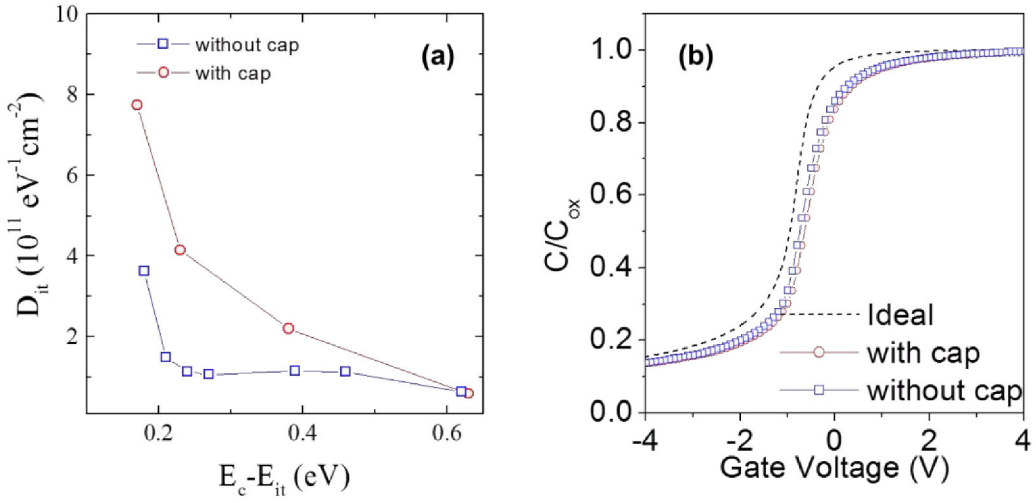


Figure 4. 17: *(a) Interface state density (D_{it}) measured on the 4H-SiC MOS fabricated on the same wafers and (b) the normalized C-V curves of MOS structures processed with and without capping layer. The experimental C-V curves have been compared with an ideal theoretical C-V characteristic.*

Clearly, a lower density of interface states in the sample annealed without cap explains the higher channel mobility. Indeed, it is also worth noting that the values of D_{it} and the corresponding channel mobility found in our MOSFETs follow the experimental trend of the correlation curve μ_{FE} vs D_{it} reported in literature [8]. It is also interesting to observe that the integral over the band gap of the D_{it} profiles gives values in the order of 10^{11} cm^{-2}, in good agreement with the parameter used to fit the temperature behaviour of the mobility. The higher trapped charges density found in the smoother interface might related to a different efficiency in the nitrogen incorporation at interface during N_2O process.

4.6 Temperature dependence and instability of threshold voltage

In spite of the considerable progress in device performance, one of major reliability concerns in SIC devices is the instability of the threshold voltage in MOS transistors and capacitors under normal operation conditions. This instability is attributed to transient trapping of channel electrons in interface traps [4,34]. To further examine this

aspects in our devices (*with* and *without* capping layer), the temperature dependence of the threshold voltage has been measured. From the threshold voltage expression, equation (4.4), we can obtain the theoretical temperature dependence of the threshold voltage, V_{TH}:

$$\frac{dV_{TH}}{dT} = \left(1 + \frac{\sqrt{4q\varepsilon_{SiC}N_A}}{\varepsilon_{ox}/t_{ox}} \frac{1}{2\sqrt{|\phi_B|}}\right)\left(\frac{|\phi_B|}{T} - \frac{K_B}{q}\left(\frac{3}{2} + \frac{E_G}{2K_BT}\right)\right) \qquad \textbf{(4.18)}$$

where ϕ_B is the bulk potential, ε_{ox} and ε_{SiC} are the dielectric constant of SiC and oxide, E_g is the band gap of SiC, N_a is the acceptor doping concentration, T is the temperature expressed in Kelvin, K_B is the Boltzmann constant and q is the electron charge. Using equation (4.18), we have obtained a theoretical dV_{TH}/dT value of -2mV/K.

In *Figure 4.18* the temperature dependence of threshold voltage for the two devices processed with and without capping layer is reported.

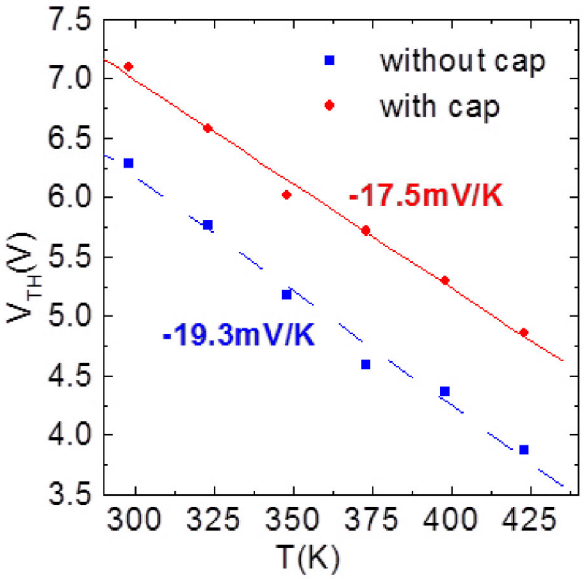


Figure 4. 18: *Temperature dependence of the threshold voltage for the two different MOSFETs devices processed with (red dots) and without (blue squares) a protective carbon capping layer. The dV_{TH}/dT for the MOSFETs with two different processed surface are also reported.*

Experimental values of dV_{TH}/dT much larger than theoretical predictions have been obtained.

Specifically, the dV_{TH}/dT values for the MOSFETs processed with and without capping layer are -17.5 mV/K and -19.3 mV/K, respectively. The larger dV_{TH}/dT value is due to the presence of a significant amount of interface states D_{it}. Wang et al. [4] showed that the larger dV_{TH}/dT value indicates a more rapidly decreasing D_{it}. Therefore, this result agree with the lower D_{it} found with the temperature mobility behavior for the MOSFETs devices processed without capping layer.

Finally, positive V_{TH} even with increasing temperature has been observed in both devices, preserving normally-off behavior with the temperature.

Hence, basing on those experimental evidences, it can end up that the peculiar surface morphology of the channel region which depends on the post-implantation annealing condition, can result into different values of D_{it} and, in a different channel mobility.

4.7 A different approach to increase the mobility: $POCl_3$ annealing

About a decade after the introduction of NO or N_2O annealing, *Okamoto et al.* have proposed another post – oxidation annealing (POA) technique that significantly reduces D_{it} at SiO_2/4H-SiC interface, introducing phosphorous (P) at the interface by flowing gas through a $POCl_3$ bubbler during POA [10]. The advantages and drawbacks of this approach have been experimentally investigated.

In this paragraph the effects of a POA in nitrous oxide (N_2O) and in phosphorus oxychloride ($POCl_3$) ambient on the electrical properties of SiO_2/4H-SiC interface have been compared.

As usual, lateral n-MOSFETs and MOS capacitors were fabricated as test vehicle to extract the field effect channel mobility and to study the electrical properties of the interface. The fabrication steps to realize these structures are the same of that described in the *paragraph 4.4.* In particular, a 45 nm-tick SiO_2 layer was deposited as a gate oxide and subjected to POA either in a N_2O or a $POCl_3$ ambient.

Considering the I_{DS}-V_{DS} characteristics of the 4H-SiC lateral MOSFETs subjected to POA of the gate oxide in N_2O or a $POCl_3$, shown in *Figure 4.19*, a significantly higher drain current is measured in the devices treated in $POCl_3$.

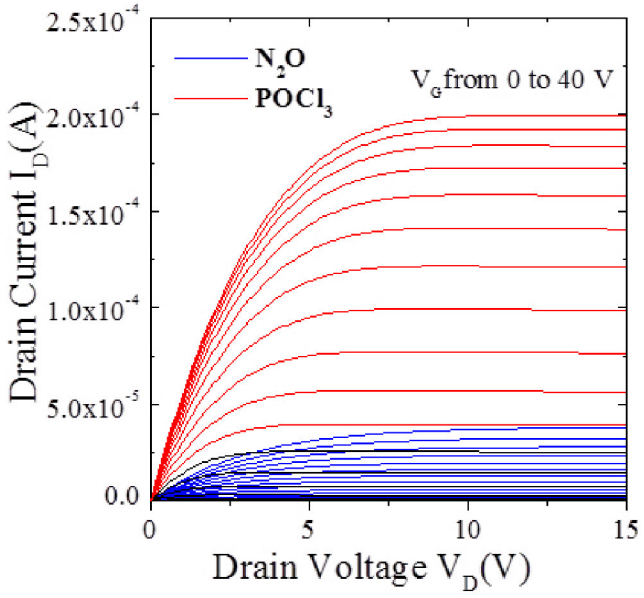


Figure 4. 19: *I_{DS}-V_{DS} characteristics of 4H-SiC lateral MOSFETs with a 45 nm thick SiO_2 gate oxide, subjected to POA in N_2O (blue line) and in $POCl_3$ (red line).*

Since the source-drain regions were created in the same condition and with the same implants, the difference in the characteristics can be mainly attributed to the difference in channel conductivity. Therefore, from the transfer characteristics in the linear region (V_{DS}=200mV), the channel mobility can be extracted. In *Figure 4.20*, the field effect channel mobility of the MOSFETs at room temperature is reported as a function of the gate bias. As can be seen, the maximum values of the mobility (peak mobility) were 19 $cm^2V^{-1}s^{-1}$ and 108 $cm^2V^{-1}s^{-1}$, for the devices subjected to POA in N_2O and $POCl_3$, respectively.

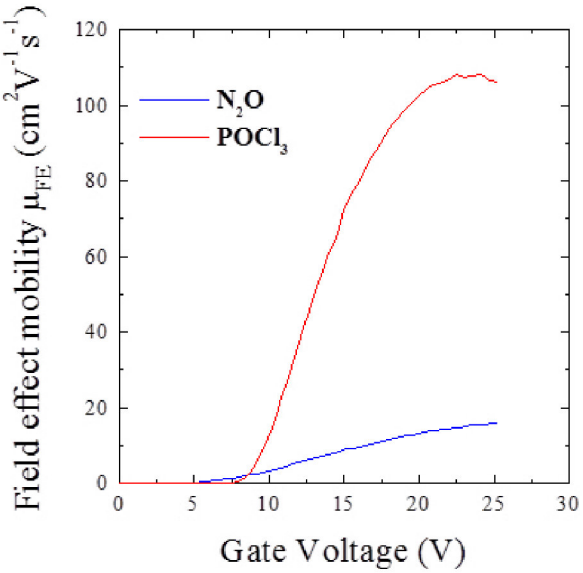


Figure 4. 20: *Field effect mobility (μ_{FE}) as a function of the gate bias for 4H-SiC MOSFETs: comparison of the devices processed with POA in N_2O (blue line) and $POCl_3$ (red line).*

The huge increasing of the channel mobility in the devices processed with $POCl_3$ was accompanied by a reduction of the D_{it} close to the conduction band edge. In particular, the values of D_{it} at about E_c-E_{it}=0.2 eV, determined by the C-V analysis of the MOS capacitors, were $5.7x10^{11}$ $eV^{-1}cm^{-2}$ for the $POCl_3$ and $1.8x10^{12}$ $eV^{-1}cm^{-2}$ for N_2O case.

In order to determine the mechanism governing the carrier transport in the MOSFETs channel for two different POA condition (N_2O vs. $POCl_3$), the temperature dependence of the field effect mobility was measured in the range 298 - 423 K and it is shown in the *Figure 4.21*.

It is worth noting that a different behaviour is observed. In fact, while in the MOSFET annealed in N_2O the channel mobility increases with the temperature from 19 $cm^2V^{-1}s^{-1}$ at room temperature to 25 $cm^2V^{-1}s^{-1}$ at 423K, the MOSFET annealed in POCl3 exhibits an opposite trend; in particular, the channel mobility decreases from 108 $cm^2V^{-1}s^{-1}$ at room temperature to 75 $cm^2V^{-1}s^{-1}$ at 423K.

To clarify the dominant mechanisms in two cases, the different physical components of the mobility have been considered (*Equation 4.15*) [25]. In particular, the bulk mobility (μ_B), the acoustic-phonon scattering (μ_{AC}) and surface roughness scattering (μ_{SR}) decrease with the temperature, while the only term that increase with the temperature is the Coulomb scattering (μ_C). Therefore, the experimental data have been fitted using a

simple power law ($\mu_{FE} \propto T^{\alpha}$); the fits are shown in *Figure 4.21* too. The observed temperature dependence can be expressed by a proportional law of $T^{+0.81}$ for N_2O annealing and $T^{-0.95}$ for $POCl_3$. This result indicates a different dominant scattering mechanism in the channel. In particular, in the case of POA in N_2O, the Coulomb scattering is the dominant mechanism in the channel (this is again consistent with the results previously shown). While, for a gate oxide annealed in $POCl_3$, the decreasing mobility with temperature suggests that the phonon scattering dominates over the other components.

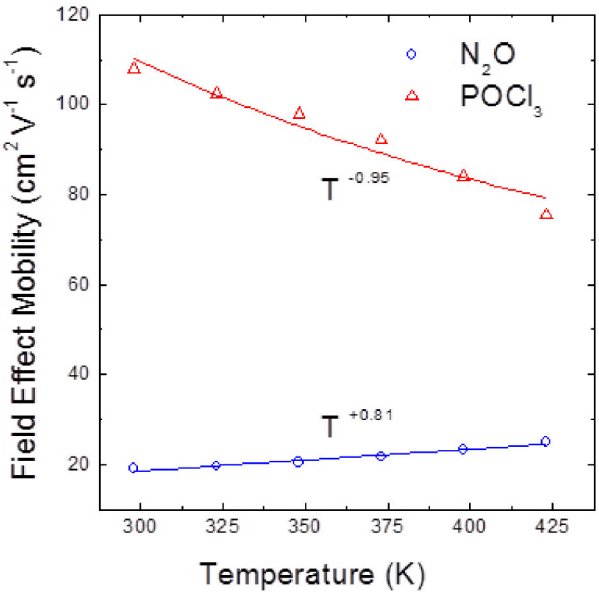


Figure 4. 21: *Temperature dependence of the field effect mobility measured in 4H.-SiC lateral MOSFETs subjected to POA in N_2O or in $POCl_3$. The continuous line is fit obtained using a power law $\mu_{FE}\, T^{\alpha}$, with α is equal to +0.81 and -0.95, respectively.*

In spite of the huge increase of the channel mobility occurring in the device processed in $POCl_3$, an instability of the electrical behaviour of the MOS capacitors has been observed [35] and an "unstable" threshold voltage under stress has been observed using $POCl_3$ in the MOSFETs device. In particular, in order to have an additional information on the reliability of the gate oxide, the stability of the flat band voltage V_{FB} of MOS capacitors was monitored by cyclically repeating C–V measurements, sweeping the bias from accumulation to depletion with increasing starting voltages at each C–V curve. Under these conditions, the electric field in the oxide is increased at each sweep. The variation of the flat band voltage (ΔV_{FB}) determined in a representative set of C–V

curves with respect to the initial value is reported in *Figure 4.22* as a function of the increasing electric field applied to the gate oxide. Evidently, while the sample annealed in N_2O shows only a slight increase of ΔV_{FB} (<0.3 V), different behaviour is shown by the sample annealed in $POCl_3$. In fact, in this case a large flat band voltage variation ΔV_{FB} = 2 V is observed already below 5 MV/cm. These effects can be associated to a strong phosphorous incorporation in the gate oxide, causing a degradation of the electrical properties [36].

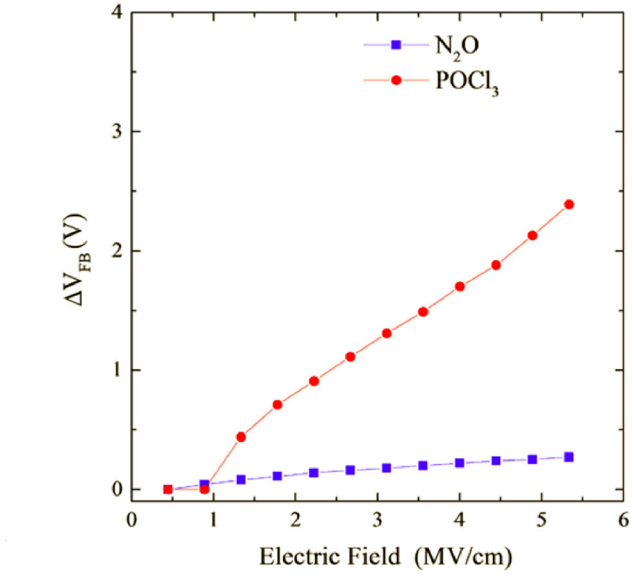


Figure 4. 22: *Variation of the flat band voltage ΔV_{FB} as a function of the increasing electric field applied to the gate oxide for the two different post-oxide annealing conditions.*

The use of the POA in $POCl_3$ ambient is limited by the possible problems on oxide reliability, hence this technique cannot be easily implemented in the fabrication of the vertical power device. However, the effects of phosphorus at SiO_2/SiC interfaces represent a milestone for silicon carbide research, not only because of mobility improvements, but also because it shines light on the nature of passivation at the atomic level. In particular, an eventual effect of a sub-surface SiC doping by phosphorus is under investigation. Hence, the effect of phosphorous in the channel region is under study to obtain an improvement of the channel mobility without a degradation of the oxide.

4.8 Conclusion

In this chapter the morphological and structural properties of the SiO_2/4H-SiC interfaces with the channel mobility in a lateral implanted MOSFET have been correlated. In particular, it has been demonstrated that the inversion channel mobility in Al-implanted lateral 4H-SiC MOSFETs is not limited by the interface roughness arising from post-implantation annealing. In fact, regardless of the interfacial roughness measured by AFM, Coulomb scattering is the main limiting mechanism of the mobility, due to the presence of trapped charges at the SiO_2/SiC interface. Moreover, a lower D_{it} have been measured in the sample with a higher channel mobility. The higher trapped charges density found in the smoother interface can be related to a different efficiency in the nitrogen incorporation at interface during N_2O process.

Finally, it has been studied a different approach to increase the channel mobility subjecting the gate oxide to POA in $POCl_3$ ambient. In particular, the higher channel mobility and its different temperature behaviour observed in the sample annealed in POCl3 were correlated to a reduction of the interface traps density.

Clearly, under practical point of view it is worth to remind that the oxide reliability is strongly affected by either a poor surface morphology of the underlying SiC or using $POCl_3$ annealing. Hence, an optimal compromise between the channel mobility and oxide reliability can be identified to realize a power device.

4.9 References

[1] V.V. Afanas'ev, F. Ciobanu, S. Dimitrijiev, G. Pensl, and A. Stesmans, *J. Phys.: Condens. Matter* **16**, S1839 (2004).

[2] F. Ciobanu, G. Pensl, V. V. Afanas'ev and A. Schoner, *Mater. Sci. Forum* **483-485**, 693 (2005).

[3] V.V. Afanas'ev, M. Bassler, G. Pensl, M. Schulz, *Phys. Status Solidi A* **162**, 321 (1997).

[4] Y. Wang, T. Khan, M.K. Balasubramanian, H. Naik, W. Wang and T. Paul Chow, *IEEE Trans. Electron Devices*, **55(8)**, 2046 (2008).

[5] S.-H. Ryu, S. Dhar, S. Haney, A. Agarwal, A. Lelis, B. Geil, C. Scozzie, *Mater. Sci. Forum* **615-617**, 743 (2009).

[6] G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, R.K. Chanana, R.A. Weller, S.T. Pantelides, L.C. Feldman, O.W. Holland, M.K. Das, J.W. Palmour, *IEEE Electron Devices Lett*. **22**, 176 (2001).

[7] C.Y.Lu, J.A. Cooper, T. Tsuji, G. Chung, J.R. Williams, K. McDonald, L.C. Feldman, *IEEE Electron Devices Lett.*, **50**, 1582 (2003).

[8] J. Rozen, A.C. Ahyu, X. Zhu, J.R. Williams, L.C. Feldman, *IEEE Electron Devices Lett.* **58**, 3808 (2011).

[9] F. Allerstam, G. Gudjönsson, H. Ö. Ólafsson, E. Ö. Sveinbjörnsson, T. Rödle, R. Jos, *Semiconductor Sci. Technol*. **22**, 307 (2007).

[10] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, T. Fuyuki, *IEEE Electron Devices Lett.* **31**, 710 (2010).

[11] F. Allerstam, H. Ö. Ólafsson, G. Gudjónsson, D. Dochev, E. Ö. Sveinbjörnsson, T. Rödle and R. Jos, *J. Appl. Phys.* **101**, 124502 (2007).

[12] N. S. Saks, A. K. Agarwal, S.-H. Ryu, and J. W. Palmour, *J. Appl. Phys.* **90,** 2796 (2001).

[13] S. Mitra, M.V. Rao, N. Papanicolaou, et al., *J. Appl. Phys.* **95**, 69 (2004).

[14] F. Giannazzo, F. Roccaforte, V. Raineri, *Appl. Phys. Lett*. **91**, 202104 (2007).

[15] M. Rambach, A. J. Bauer, and H. Ryssel, *Phys. Stat. Sol. (b)* **245**, 1315 (2008).

[16] R. Nipoti, F. Mancarella, F. Moscatelli, R. Rizzoli, S. Zampolli, M. Ferri, *Electrochem. Solid-State Lett.* **13,** H432 (2010).

[17] A. Frazzetto, F. Giannazzo, R. Lo Nigro, S. Di Franco, C. Bongiorno, M. Saggio, E. Zanetti, V. Raineri, F. Roccaforte, *Nanoscale Research Letters*, **6**, 158 (2011).

[18] A. Frazzetto, F. Giannazzo, R. Lo Nigro, V. Raineri, F. Roccaforte, *J. Phys. D: Appl. Physics* **44**, 255302 (2011).

[19] S. Haney, A, Agarwal, *Journal of Electronic Materials*, **37(5)**, 666 (2008).

[20] H. Naik, K. Tang, T.P. Chow, *Mater. Sci. Forum*, **615-617**, 773 (2009).

[21] K. K. Lee, T. Ohshima, A. Ohi, H. Itoh and G. Pensl, *Jap. J. Appl. Phys.* **45,** 6830 (2006).

[22] S.M. Sze, *Physics of Semiconductor Devices*, 2nd Ed., John Wiley &Sons, New York (1981).

[23] D.K. Schroder *Semiconductors Materials and Device Characterization* 3rd ed., Wiley, New York (2006).

[24] H. Saitoh, A. Seki, A. MAnabe, T. Kimono *Mater. Sci. Forum*, **556-557**, 659 (2007).

[25] A. Pérez-Tomás, P. Brosselard, P. Godignon, J. Millán, N. Mestres, M.R. Jennings, J.A. Covington, P.A. Mawby, *J. Appl. Phys*. **100**, 114508 (2006).

[26] A. Pérez-Tomàs, P. Godignon, N. Mestres, J. Millàn, *Microelectronic Enineering* **83**, 440-445 (2006).

[27] G. Mazzoni, A.L. Lacaita, L.M. Perron, A. Pirovano, *IEEE Trans. on Electron Devices* **46**, 1423 (1999).

[28] A. Pérez-Tomàs, M.R. Jennings, P. A. Mawby, J. A. Covington, P. Godignon, J. Millan N. Mestres, *Materials Sci. Forum* **556-557**, 835 (2007).

[29] E. Arnold and D. Alok *IEEE Trans. Electron Devices* **48**, 1870 (2001).

[30] T.L. Biggerstaff, C.L. Reynolds, T. Zheleva, A. Lelis, D. Habersat, S. Haney, S.-H. Rryu, A. Agarwal, G. Duscher, *Appl. Phys. Lett.* **95**, 032108 (2009).

[31] E. Pippel, J. Woltersdorf, H. Ö. Ólafsson, and E. Ö. Sveinbjörnsson, *J. Appl. Phys.* **97**, 034302 (2005).

[32] H. Watanabe, T. Hosoi, T. Kirino, Y. Kagei, Y. Uenishi, A. Chanthaphan, A. Yoshigoe, Y. Teraoka, and T. Shimura, *Appl. Phys. Lett.* **99**, 021097 (2011).

[33] A. M. Beltran, S. Schamm-Chardon, V. Mortet, M. Lefebvre, E. Bedel-Pereira, F. Cristiano, C. Strenger, V. Häublein, and A. J. Bauer, *Mat. Sci. Forum* **711**, 134 (2012).

[34] A.J. Lelis**,** D. Habersat, R. Green, and N. Goldsman, *Materials Science Forum* **600-603**, 807-810 (2009).

[35] P. Fiorenza, L.K. Swanson, M. Vivona, F. Giannazzo, C. Bongiorno, S. Lorenti, A. Frazzetto F. Roccaforte, *Mat. Sci. Forum* **778-780**, 623-626 (2014).

[36] P. Fiorenza, L.K. Swanson, M. Vivona, F. Giannazzo, C. Bongiorno, A. Frazzetto, F. Roccaforte *Appl. Phys. A* **115**, 333–339 (2014).

Chapter 5
4H-SiC vertical power MOSFET

In the previous chapters some relevant scientific challenges of SiC MOSFET technology have been described. All the previously investigated processing steps have been implemented in a vertical MOSFETs, to obtain the best performance in term of power switch.

In this chapter, an overview of the results on 4H-SiC vertical power MOSFET (VMOS), fabricated in STMicroelectronics front end line site of Catania (Italy), is given. In particular, a preliminary static and dynamic characterization, advantages and most important device parameters of 4H-SiC power MOSFET are provided.

The results reported in the following paragraphs can be a first start up for the future research activities for the next generation of power devices in SiC.

5.1 Background

In the previous chapters, it has been already pointed out how the outstanding properties of 4H-SiC make this material an excellent candidate for the fabrication of power MOSFETs.

In particular, an ideal *power switch* should have the following characteristics:

- Able to carry a large current with zero voltage drop in the on-state;
- Blocks high voltage with zero leakage in the off-state;
- Incurs zero energy loss when switching from off-state to on-state and vice versa.

Clearly, it is very difficult to obtain these desirable but opposed characteristics using silicon, especially if the switch must work at high voltage and high current (*power devices*). On the other hand, the smaller drift layer resistance (R_D) allows SiC MOSFETs to fulfil the same tasks as Si-IGBTs, but with lower switching losses and higher frequency and temperature operation.

Until now, the fabrication on SiC of vertical MOSFETs was a major objective for all the SiC players. Its functional similarities with Si-VMOSs and Si-IGBTs make it very easy to substitute them in many applications. For that reason, it is believed that the SiC vertical MOSFET will revolutionize power electronic technology in the next future.

The vertical power MOSFET structure is difficult to produce for various reasons.

The first issue dealt by the manufacturers regards the design of high voltage devices: indeed, the structure, like the VMOS, relies on the vertical equipotential lines through the drift layer during the blocking state. In forward mode, the vertical MOSFET uses a controlled inversion channel linking the source to the JFET and drift area. All these details have been treated in *Chapter 2*. In the *Figure 5.1* reports a schematic vertical MOSFET layout:

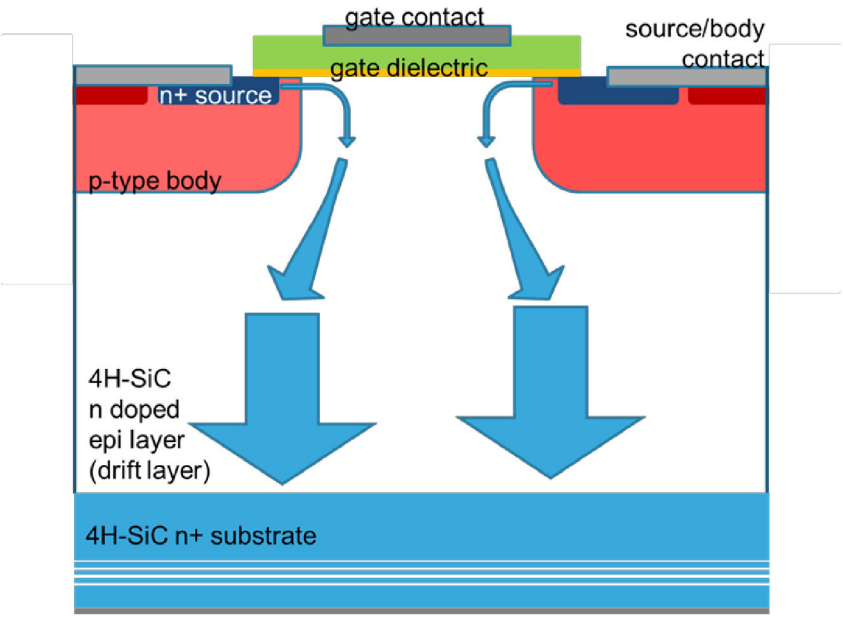


Figure 5. 1: *Schematic view of the vertical cut of a MOSFET*

In an industrial environment, the integration of SiC devices active layers requires the use of dedicated equipment for high temperature activation (>1700 °C) and high temperature implant (>500 °C). Moreover, in the device fabrication flow all dielectric layers are processed at "low temperature" (like in the Si) to prevent that high temperature process can limit operation stability of dielectric layers for gate and contact insulation.

Moreover, since the conventional diffusion technique, used for "Silicon world", cannot be implemented in SiC (due to the extremely low diffusivity of dopants in this material), another important issue comes from the creation of both the selective doped regions and above all of p-well. The simplest solution is the use of ion implantation to selectively dope areas and especially the p-well. This process creates surface crystal defects that

will later deteriorate the channel quality. Special care must be taken with the dose, profile and temperature of the p-well implantation. Moreover, the surface could be degraded using the high temperature annealing to active the dopant. In this work, it has been observed that the quality of the interface has been improved using a protective carbon capping layer, (*Chapter 3* and *Chapter 4*), [1,2].

The major challenge with the MOSFETs integration on SiC is to obtain an inversion channel of good quality. In fact, the very low inversion channel mobility achieved on 4H-SiC have prevented for many years the fabrication of low-resistance MOSFETs that would have proven the SiC potential for power devices. Many years of worldwide investigation have permitted to identify certain sources of the degradation and find solutions. Nowadays, the use of nitridation process of the gate oxides to optimize the channel properties are the commonly adopted solution. This aspect has been discussed in previous chapters, also [3].

Thanks to the progresses in all the SiC fabrication steps, first CREE, then RHOM and finally STMicroelectronics (STM) are today the world industrial players capable to produce and commercialize the 4H-SiC power MOSFETs [4,5,6]. The *Table 5.1* summarizes the properties of the different commercially available vertical power MOSFETs:

Manufacturer	V_{BR}	I_D	$R_{ON}@I_D$	P_{TOT}	T_{Jmax}	Ref.
CREE	1200 V	20 A	80 mΩ	208 W	150 °C	[4]
ROHM	1200 V	20 A	80 mΩ	179 W	150 °C	[5]
STM	1200 V	20 A	80 mΩ	270 W	200 °C	[6]

Table 5. 1: *Properties of commercially available SiC vertical power MOSFETs*

In particular, it is possible to observe the advantages of the STMicroelectronics power device in term of the power losses and the maximum temperature work (T_{Jmax}) at the same breakdown voltage and at the same on-resistance (R_{ON}) at the current of work.

In the following paragraph, the main electrical characteristics of the vertical power MOSFETs fabricated by STM will be shown.

5.2 STM MOSFETs

In *Figure 5.2* the STMicroelectronics MOSFET photos are reported. In this device, the channel perimeter is maximized by using I-line stepper photolithography equipment able to introduce VLSI feature sizes in MOSFET elementary structure.

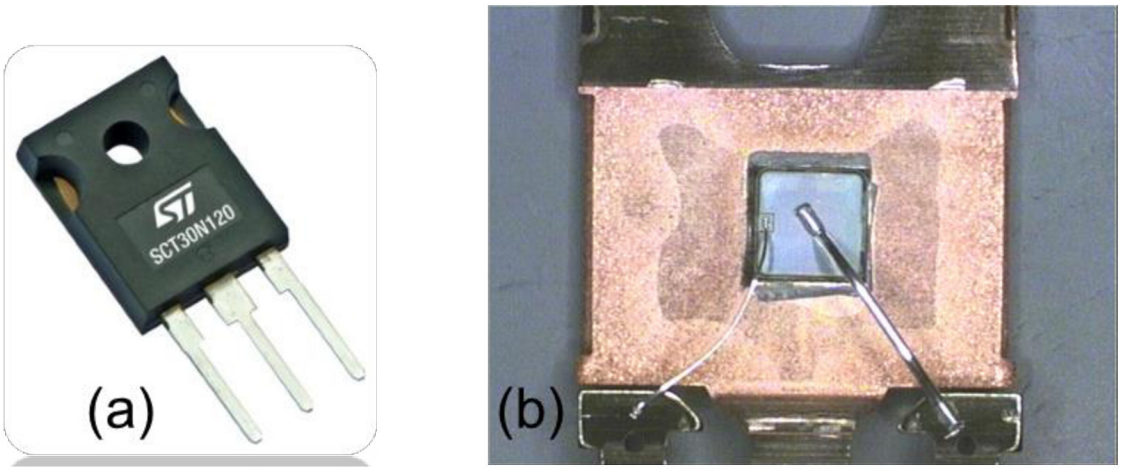


Figure 5. 2: *STM MOSFET device photo, in the package (a) and after decapping (b).*

A self-aligned channel has been realized to maintain a perfect reproducibility of the channel geometry in the whole wafer and from wafer to wafer. With such a design, a good reproducibility of the electrical parameters is also achieved. On-state losses area minimized by adopting many solutions. The electrically active defect density in the channel (i.e., interface states) is strongly reduced by performing N_2O processes as described in *Chapter 4* after gate dielectric formation. The channel dimension together with junction depth is maintained at sub-micrometric level. In particular, in *Figure 5.3* a feedback of the devices processing has been performed using the scanning capacitance microscopy (SCM) technique in the CNR-IMM laboratory. This technique has allowed to point out the body, source regions by the 2D carrier distribution and thus the effective channel length [7].

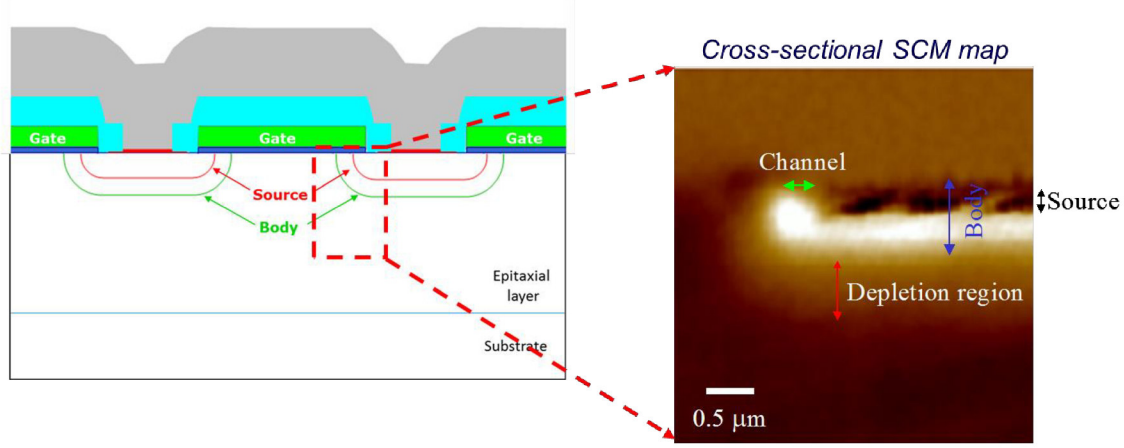


Figure 5. 3: Cross section of power MOSFET active area by SCM map.

The combination of these solutions allowed to obtain very efficient static behaviour, reduced dynamic losses and high ruggedness level in unclamped inductive switching mode.

5.3 Electrical Characteristics of STM 4H-SiC MOSFET

5.3.1 Static Behaviour

Electrical Characterization has been performed on STM 4H-SiC MOSFETs at room temperature and at the maximum temperature rate (T=200°C). All major static characteristics of the device under test (*DUT*), mounted in the commercial TO-247 package, are measured using a Tektronix 371A curve tracer.

Oxide performance has been checked using the gate leakage current. In particular, the gate leakage current may be specified as I_{DGO}, leakage between gate and drain with the source open, or I_{SGO}, leakage between gate and source with the drain open.

In *Figure 5.4(a)* the I_{DGO} curves for the two temperatures are shown. In particular, the red curve is the I_{DGO} behaviour at room temperature (R_T), while the blue curve is the I_{DGO} behaviour at the maximum temperature rate.

In the *Figure 5.4(b)* the I_{SGO} curves for the two different temperatures are shown and compared. Moreover, in this configuration the peaks in the first quadrant indicate the

threshold voltage of the devices and it is possible to observe a decrease of the V_{TH} with increasing the temperature.

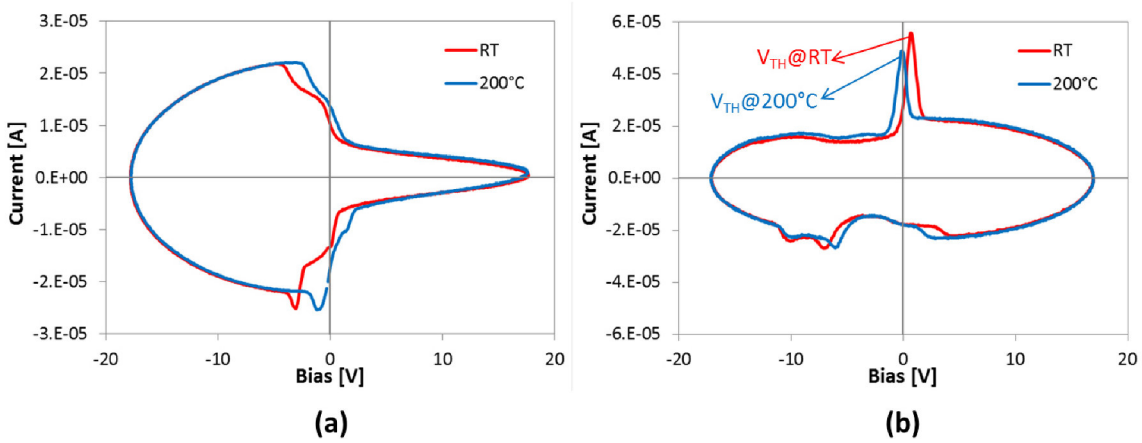


Figure 5. 4: *(a) I_{DGO} curves and (b) I_{SGO} curves at room temperature (red line) and T=200 °C (blue line). In the I_{SGO} configuration the peaks in the first quadrant show the V_{TH} of the device at the two different temperature.*

These leakages result in lower values of leakage current (in the order of some units of nA) and do not represent worst-case conditions.

The threshold voltage is really a turn-off specification. It tells how many milliamps of drain current will flow at the threshold voltage, so the device is basically off but on the verge of turning on. The threshold voltage has a negative temperature coefficient, meaning the threshold voltage decreases with increasing temperature.

Therefore, the threshold voltage behaviour with the temperature has been studied. In particular, the threshold voltage (V_{TH}) for the power device has been measured at a fixed value of current considering the short between gate and drain terminal. In *Figure 5.5 (a)* the V_{TH} trend with the temperature is shown. Considering the V_{TH} value extracted at 1 mA it is possible to observe that V_{TH} decreases with the increasing of the temperature and the slope is around of 6.1mV/°C, *Figure 5.5(b)*.

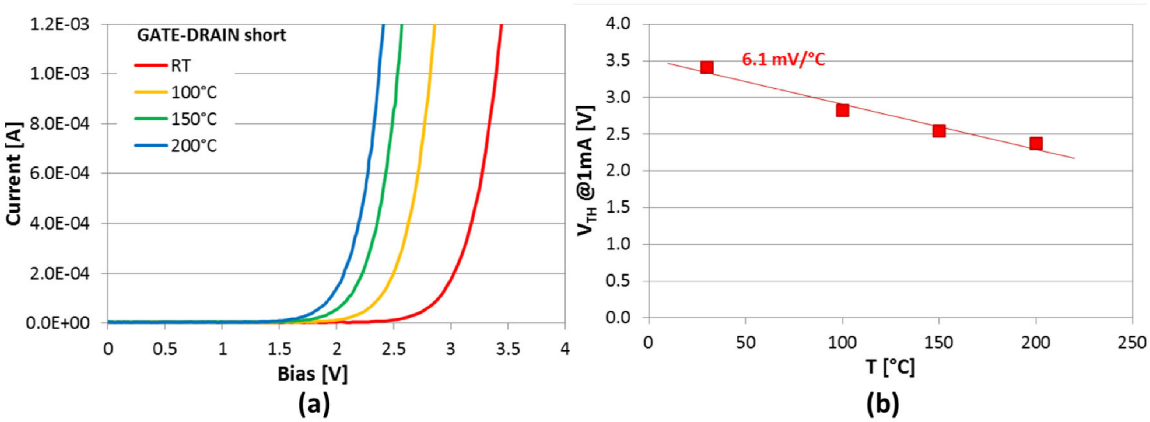


Figure 5. 5: *Threshold Voltage behaviour with the temperature (a) and the V_{TH} value extracted at 1mA for the four different temperatures (b). The V_{TH} decrease with the increasing temperature with a slope of 6.1mV/°C.*

In *Figure 5.6*, the on-state characteristics at room temperature (RT) and at T=200 °C have been reported.

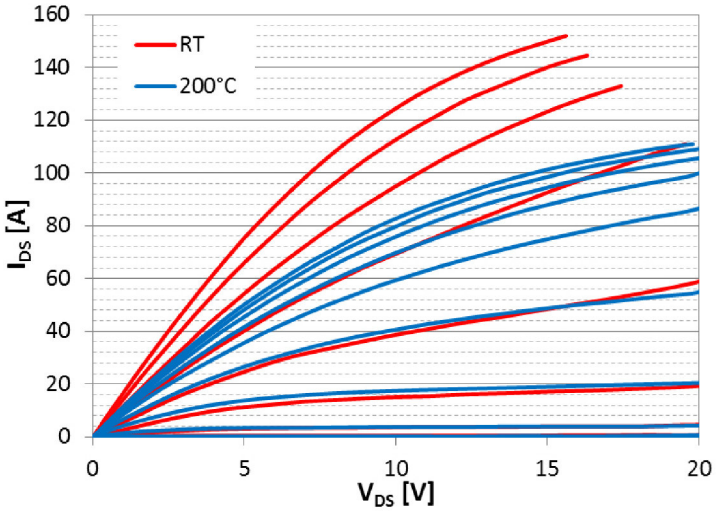


Figure 5. 6: *Typical I-V characteristics of 4H-SiC power MOSFET at room temperature and T=200°C.*

Finally, to complete the electrical characterization of the MOSFET device, the off-state characteristics, with the source and gate terminals shorted, at the two different temperatures are reported in *Figure 5.7*.

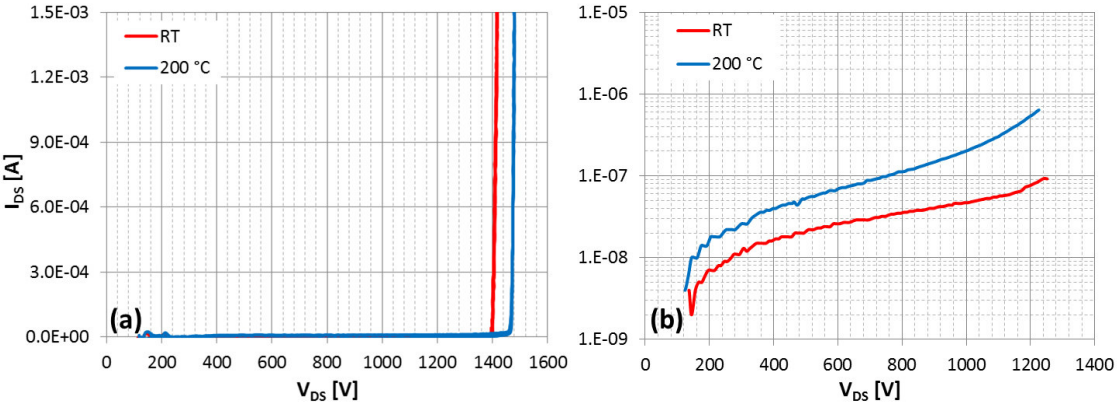


Figure 5. 7: *Off-state characteristics with Breakdown voltage (a) and a zoom on the leakage current in logarithmic scale (b) of the device at the two temperatures.*

The source-drain breakdown voltage, called BV_{DSS}, is the drain-source voltage at which no more than the specified drain current will flow at the specified temperature and with zero gate-source voltage. This tracks the actual avalanche breakdown voltage. The I_{DSS}-zero gate voltage drain current is the drain-source leakage current at a specified drain-source voltage when the gate-source voltage is zero.

In particular, the breakdown voltage for the STM MOSFET, shown in *Figure 5.7(a)*, is higher than 1400V for both the temperatures and it has a positive temperature coefficient. The off-state leakage current, *Figure 5.7(b)*, is lower than 1μA for both temperatures up to 1200V. This indicates a very good blocking capability of the SiC MOSFET over a wide temperature range, especially when compared to the conventional Si switches, whose leakage currents usually increase significantly as the temperature goes above their T_{Jmax} around 150 °C.

Another important characteristic of the STM 4H-SiC MOSFET is associated with the temperature dependence of On-Resistance. Indeed, the R_{ON} remains constant up to 100 ºC and shows a 10% increase at 150 ºC; increase becomes 30% at 200 ºC, *Figure 5.8*.

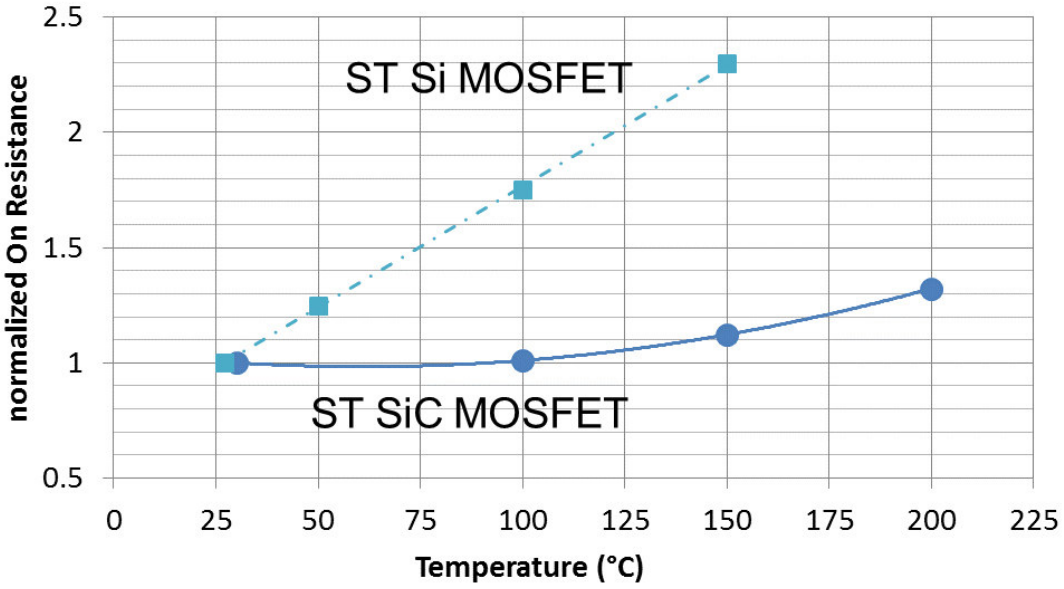


Figure 5. 8: *Temperature dependence of the 4H-SiC and Si MOSFET On-Resistance, in common application temperature range.*

The observed behaviour is not common in conventional Si MOSFETs or superjunction devices. In fact, in *Figure 5.8* the temperature dependence of Si MOSFET is reported for comparison. It is possible to see that in Silicon, the on-resistance variation is constant with temperature with an increase of 130% at 150 ºC. In other supplier's available SiC MOSFETs such value is 90% at 150 ºC. Therefore, the studied SiC MOSFET shows lowest Ron at high temperatures and it is the only supplier to guarantee max Tj as high as 200°C. This is associated mainly to thermal reliability of packages and to the device behaviors. Moreover, when properly packaged, the device could operate at a higher temperature than 200ºC.

5.3.2 Dynamic Behaviour

STM 4H-SiC MOSFETs is an excellent candidate to be used in these applications that require fast, efficient switching thanks to its dynamic behaviour. In fact, the STM 4H-SiC devices can operate at much higher switching frequency with lower switching losses and at higher temperatures.

Being a unipolar device, the SiC MOSFET can be switched much faster than a commercial Si IGBTs, which means higher switching frequency for the same switching loss.

In a real power converter to directly compare the performance of MOSFETs, even one of a different technology such as an IGBT, the inductive switching energy data are performed.

The switching behaviours of the DUT are characterized using the standard double-pulse testing method [8]. Two independent and freely configurable gate pulses turn on the power device for a predetermined time. How fast a device turns on and off basically depends on the gate resistances, the voltage level of the driver, and the characteristics of the device itself. *Figure 5.9* shows the inductive switching test circuit schematic.

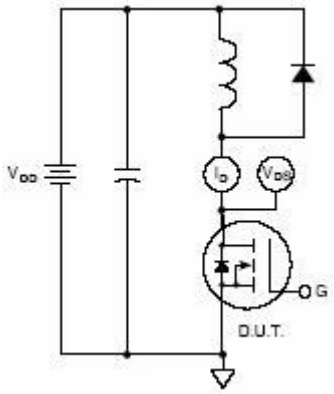


Figure 5. 9: *Inductive switching loss test circuit.*

The switching test is conducted with an inductive load at 800V and 20A.

Figure 5.10 gives the experimental results obtained with a resistance R_G=6.8Ω, V_{GSOFF}=-2V and V_{GSON}=20V. In particular, in *Figure 5.10(a)*, the Turn OFF waveforms and in *Figure 5.10(b)* the Turn ON waveforms are shown.

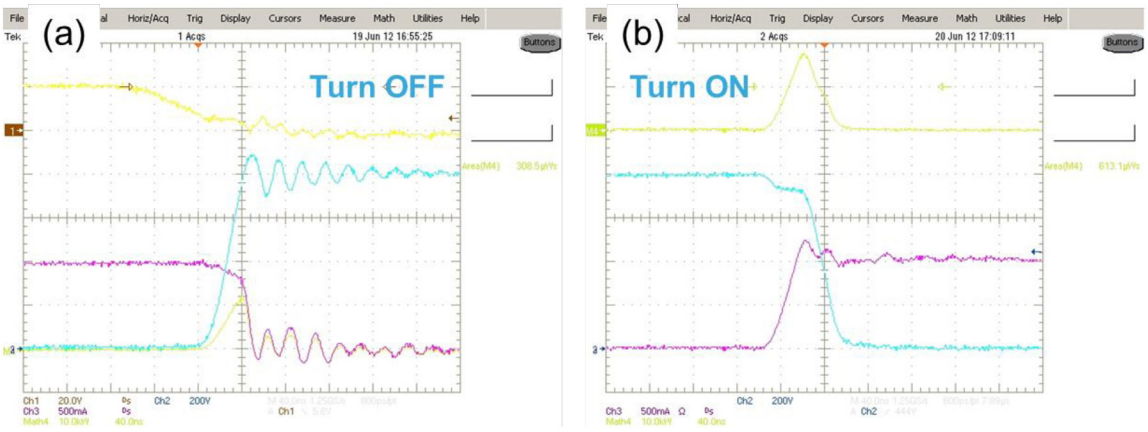


Figure 5. 10: *4H-SiC Power MOSFET switching waveforms for (a) Turn OFF and (b) Turn ON. I=20A, V=800V, Rg=6.8 Ω.*

The switching energies (E_{OFF} and E_{ON}) are calculated from experimental waveforms.

In particular, turn-on switching energy (E_{ON}) is the integral of the product of drain current and drain-source voltage over the interval from when the drain current rises to 5% or 10% of the test current to when the voltage falls below 5% of the test voltage. At last, E_{OFF} is the integral of the product of drain current and drain-source voltage over the interval starting from when the gate-source voltage drops below 90% to when the drain current reaches zero.

Considering the switching energy as a function of the temperatures, it remains almost constant with temperature. In *Table 5.2* the E_{OFF} and E_{ON} at the Room Temperature and T=125 °C are reported.

T_C (°C)	E_{ON} (µJ)	E_{OFF} (µJ)
25	615	315
125	600	370

Table 5. 2: *Switching energy losses at RT and 125 ºC*

Finally, to evaluate the ruggedness of the 4H-SiC MOSFET device the *Unclamped Inductive Switch (UIS)* test on a 10 mH coil is showed in *Figure 5.11*: device withstands 1.2 J.

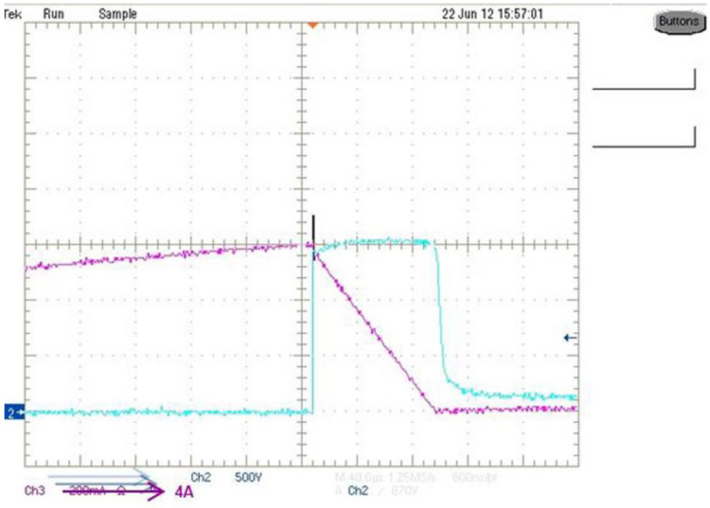


Figure 5. 11: *UIS waveform with 10mH coil.*

Currently, IGBT modules that combine Si-IGBTs and Si-FRDs (*fast-reverse diodes*) are commonly used as power modules to handle high currents and high blocking voltage. SiC power modules are increasingly applied to power supplies for industrial equipment, PV power conditioners and others. Comparing the efficiency of the SiC MOSFETs respect to the best Si-IGBT, the studied 1200V SiC MOSFETs guarantee the same efficiency at 100 kHz compared to a 1200V Si-IGBT at 25 kHz, (*Figure 5.12*).

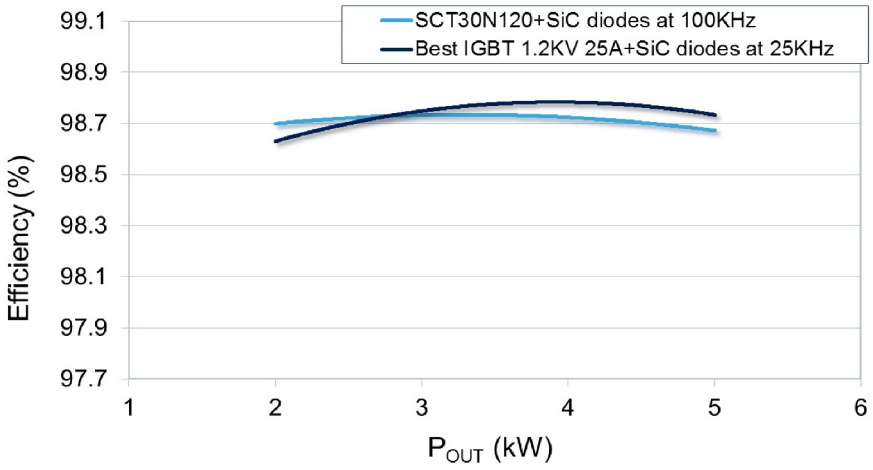


Figure 5. 12: *Comparison of 1200V SiC MOSFET efficiency vs. 1200V Si IGBT. SiC MOSFET device at 100 kHz guarantees the same efficiency of Si IGBT device at 25 kHz.*

Hence, the SiC modules allow substantial reduction in switching losses associated with the tail current and the recovery current of Si-IGBT modules. The fundamental benefits are:

- Improvement of conversion efficiency thanks to lower switching losses;
- Simplification of thermal management, e.g., smaller and less expensive heat sink or cooling system, replacement of water/forced air with natural cooling;
- Downsizing of passive components (inductors, capacitors) thanks to increasing switching frequency.

5.4 Conclusion

The 4H-SiC technology is surely enough mature that MOSFETs devices have already reached the market. This chapter systematically evaluates the characteristics of the commercial 1.2kV, 45A, SiC power MOSFET (SCT30N120) compared the room temperature characteristics with the high temperatures.

It has been observed that this device can operate at T_{jmax}=200°C without a strongly variation of its fundamental static behaviours. In particular, both the off-state (leakage current) and on-state (R_{ON}) is not strongly influenced by the increasing temperature. In fact, the leakage current remains lower than 1µA at 200°C and the R_{ON} remains constant up to 100 ºC and shows a 30% increase at 200 ºC.

Moreover, the dynamic behaviours show a substantial improvement using this device. Indeed, the 1200V SiC MOSFETs guarantee the same efficiency at 100 kHz compared to a 1200V Si-IGBT at 25 kHz.

The static and switching characterizations have shown the great potential of the device also for high-temperature operations.

5.5 References

[1] A. Frazzetto, F. Roccaforte, F. Giannazzo, R. Lo Nigro, C. Bongiorno, S. Di Franco, M.H. Weng, M. Saggio, E. Zanetti, V. Raineri, *Mater. Sci. Forum* ***679-680***, 413-416 (2011).

[2] A Frazzetto, F Giannazzo, R Lo Nigro, V Raineri and F Roccaforte, *J. Phys. D: Appl. Phys*., **44** , 255302 (2011).

[3] A. Frazzetto, F. Giannazzo, P. Fiorenza, V. Raineri, F. Roccaforte, Applied Physics Letters **99**, 072117 (2011).

[4] www.cree.com

[5] www.rohm.com

[6] www.st.com

[7] F. Giannazzo, P. Fiorenza, M. Saggio, F. Roccaforte, *Mater. Sci. Forum* ***778-780***, 407-413 (2014).

[8] G. G. Pollock, A. I. Johnson, *The dynamics of extraction processes: Part II. Comparison of dynamic testing methods and their application to an extraction process.*, Can. J. Chem. Eng., **47**, 565–575 (1969).

Conclusion

In this thesis different aspects, issues and challenges related to the fabrication of 4H-SiC MOSFETs have been tackled.

The transport properties at the interface metal/SiC and SiO_2/SiC were monitored with electrical and structural investigations to study and to understand the main mechanisms limiting devices behaviours during the on-state conduction and hence impacting on the efficiency of the power devices in SiC. In particular, the main efforts have been directed to the formation of good Ohmic contacts on implanted p-type 4H-SiC and to understand the mechanisms limiting transport of the carriers at interface SiO_2/4H-SiC and so the factors influencing channel resistance.

The formation of a good Ohmic contact on the implanted p-type regions is a key technological issue for wide band gap semiconductors in general, due to the large Schottky barrier heights at metal-semiconductor interface and the high ionization energy of the p-type dopants. In this work, Ti/Al contacts on p-type (Al-implanted) doped regions were studied in detail. In particular, it has been observed that after the post-implantation annealing to activate the implanted Al (at 1700°C), significant changes of roughness of the SiC surfaces occurs if the samples are annealed *without* any protection (capping layer). The surface of the implanted layer influences also the properties of alloyed Ti/Al Ohmic contacts formed on it. In fact, the electrical properties of the contacts, evaluated by TLM analysis, showed a reduction of the specific contact resistance in the smoother sample (processed *with* a capping layer) with respect to the rougher sample. However, the average measured values of the ρ_c for both samples are in the order of $10^{-4}\Omega cm^2$. The electrical properties of the implanted layer are independent of the particular process but only depend on the Al-implanted dose. To understand the transport mechanisms and properties at the Ti/Al/4H-SiC interface, the temperature dependence of the specific contact resistance has been studied, indicating that thermionic field emission (TFE) is the dominant transport mechanism through the metal/SiC interface. The reduction of the specific contact resistance, observed in the sample annealed *with* the capping layer, can be associated to a lowering of the Schottky barrier from 0.51 eV (*without* capping layer) to 0.46 eV (*with* capping layer). Finally, the electrical results have been correlated with an inhomogenous microstructural

interface region metal /4H-SiC different in the two cases, when using or not the capping layer, which can justify the different macroscopically measured Schottky barrier heights.

Concerning the channel mobility, the post oxidation annealing (POA) in N_2O ambient of the gate oxide has been chosen to improve the SiO_2/SiC interface quality. Despite the improvement obtained, the effects of the post implantation annealing treatments on the channel mobility remains controversial. In this work, the influence of the surface morphology and mechanism limiting the channel mobility in MOSFETs fabricated in Al-implanted 4H-SiC have been investigated. In particular, similarly to the study performed on Ohmic contacts, also the mobility behavior was investigated for devices fabricated using the two different post-implantation annealing. The field effect channel mobility (μ_{FE}), extracted by lateral MOSFETs as test vehicles, was higher in the device annealed without capping layer. In particular, the value of the peak mobility determined at room temperature were 40 and 24 $cm^2V^{-1}s^{-1}$, for the samples processed *without* and *with* capping layer, respectively. Associated with channel mobility also a higher threshold voltage (V_{TH}) of 7.15 V was extracted for the device annealed with capping layer with respect to that annealed without capping layer of 6.28V. Due to the higher channel mobility in the sample with the largest roughness (RMS = 1.75 nm), it can be inferred that the surface roughness scattering is not the limiting factor to the carrier transport in the channel. This possibility is consistent with recent results demonstrating that the electronics quality of the SiO_2/4H-SiC interfaces is not correlated to the surface roughness, but is rather associated to the presence of carbon –related electronics states. The temperature dependence of the channel mobility allows to determine the limiting mechanisms the channel mobility at the interface SiO_2/4H-SiC, demonstrating that Coulomb scattering by trapped charges is the main limiting mechanism of the mobility, regardless of the interfacial roughness. A direct measure of the density of the interface states (D_{it}) on MOS capacitors showed a lower density of interface states in the sample annealed without cap. The higher trapped charges density found in the smoother interface might related to a different efficiency in the nitrogen incorporation at interface during N_2O process. This issue however needs to be verified by means of chemical analyses.

An alternative method to improve the channel mobility has been also investigated in this work, using a post oxidation annealing in $POCl_3$ ambient. In this

case, a significantly higher drain current was measured in the devices treated in $POCl_3$, corresponding to an increase of the mobility up to 108 $cm^2V^{-1}s^{-1}$. The increase of the channel mobility in the devices processed with $POCl_3$ was accompanied by a reduction of the D_{it} close the conduction band edge. However, an instability of the electrical behaviour of the MOS capacitors has been observed under bias stresses, which has been associated to a degradation of the oxide properties and microstructure as a consequence of a strong P-incorporation during POCl3 annealing. Hence, this technique cannot be easily implemented for the fabrication of the power devices.

Finally, all the progresses previously tackled have been integrated in the power MOSFET device fabricated by STMicroelectronics. The static and dynamic behaviours of the device have been reported. In particular, the static measurements (on-state and off-state) show that the device can operate up to 200°C, without significant variations of its performance, unlike the best silicon devices on the market today. Moreover, the device shows substantial better performances with respect to the Si device (as best IGBT 1200V) when it works in applications that require fast, efficient switching thanks to its dynamic behaviour.

In spite of the significant progresses and maturity obtained from SiC MOSFETs technology, further challenges must be tackled still for the development of next generation devices.

First of all, it is necessary move forward the comprehension of the interface traps. Most of the works has studied the density traps at the interface (D_{it}) considering the n-type MOS capacitors test-structures. The values of D_{it} are measured close to the conduction band edge of 4H-SiC/SiO_2 MOS capacitors. In the literature, interface state density near the valence band edge has not been largely handled but could better explain the trapping mechanisms at the interface SiO_2/SiC in the MOSFETs devices. On the other hand, these mechanisms are in turn indicated as the main responsible for low channel mobility and as a possible reason for V_{TH} instabilities, occurring under prolonged application of a gate bias.

Moreover, the next generation of power MOSFETs requires a further optimization of the on-resistance, best efficiency and switching speed. Compared to conventional planar MOSFETs, which have JFET regions increasing the on-resistance, the new MOSFETs exploit the trench technology. The low on-resistance of the trench devices is associated with the absence of the JFET region and with the possibility to take advantage of

different lattice planes to improve the channel mobility. The low on-resistance of the trench SiC MOSFETs is ideal for improving inverter power density and performance.

As a further point, a higher-quality gate oxide is needed. Gate oxide serves as an insulating layer in order to sustain a high transverse electric field. If the oxide quality and integrity are poor, current may leak through the oxide. This leakage current could have a detrimental effect on the device performance. The current-conduction mechanisms through the gate oxide, which contribute to the hard or soft dielectric breakdown, are the more critical issues for these devices.

Presently, SiO_2, subjected to thermal post-oxidation annealing in nitric ambient with an ultra-low leakage current, is commonly employed as the material to form the gate oxide in the MOSFETs. Because of its relatively low dielectric constant (k), if compared with the SiC substrate, the gate oxide would electrically break down before than the breakdown field of SiC is achieved. In order to reduce the electric field strength imposed to the oxide, a replacement of this oxide with a relatively *high-k* oxide could be made in the next future. The reliability of the gate oxide became more critical in the trench structures, hence the interplay between *high-k* oxide and trench has to be investigated and deeply understood.

All the aforementioned open issues are presently object of the research activity carried out by the scientific academic and industrial community working on SiC.

Publications

1. A. Frazzetto, F. Giannazzo, R. Lo Nigro, S. Di Franco, C. Bongiorno, M. Saggio, E. Zanetti, V. Raineri, **F.** Roccaforte, *Nanoscale electro-structural characterization of Ohmic contacts formed on p-type implanted 4H-SiC,* Nanoscale Research Letters **6**, (2011) 158.

2. A. Frazzetto, F. Roccaforte, F. Giannazzo, R. Lo Nigro, C. Bongiorno, S. Di Franco, M.H. Weng, M. Saggio, E. Zanetti, V. Raineri, *Impact of surface morphology on the electrical properties of Al/Ti Ohmic contacts on Al-implanted 4H-SiC*, Mater. Sci. Forum **679-680**, (2011) 413-416.

3. A. Frazzetto, F. Giannazzo, R. Lo Nigro, V. Raineri, F. Roccaforte, *Structural and transport properties in alloyed Ti/Al Ohmic contacts formed on p-type Al-implanted 4H-SiC annealed at high temperature,* J. Phys. D: Appl. Phys., **44**, (2011) 255302.

4. A. Frazzetto, F. Giannazzo, P. Fiorenza, V. Raineri, F. Roccaforte, *Limiting mechanism of inversion channel mobility in Al-implanted lateral 4H-SiC metal-oxide semiconductor field-effect transistors*, Appl. Phys. Lett. **99,** (2011) 072117.

5. F. Roccaforte, A. Frazzetto, G. Greco, R. Lo Nigro, F. Giannazzo, M. Leszczyński, P. Pristawko, E. Zanetti, M. Saggio, V. Raineri , *Microstructure and transport properties in alloyed Ohmic contacts to p-type SiC and GaN for power devices applications,* Mat. Sci. Forum **711,** (2012) pp. 203-207.

6. A. Frazzetto, F. Roccaforte, F. Giannazzo, R. Lo Nigro, M. Saggio, E. Zanetti, V. Raineri, *Effects of different post-implantation annealing conditions on the electrical properties of interfaces to p-type implanted 4H-SiC,* Mat. Sci. Forum, **717-720**, (2012) pp. 825-828.

7. F. Roccaforte, A. Frazzetto , G. Greco, F. Giannazzo, P. Fiorenza, R. Lo Nigro, M. Saggio, M. Leszczyński, P. Pristawko,V. Raineri, *Critical issues for interfaces to p-type SiC and GaN in power devices***,** Appl. Surf. Sci. **258 (12)**, (2012) 8324-8333.

8. P. Fiorenza, F. Giannazzo, A. Frazzetto, F. Roccaforte, *Influence of the surface morphology on the channel mobility of lateral implanted 4H-SiC(0001) metal-oxide-semiconductor field-effect transistors*, J. Appl. Phys. **112**, (2012) art. N° 084501.

9. L.K. Swanson, P. Fiorenza, F. Giannazzo, A. Frazzetto, F. Roccaforte, *Correlating macroscopic and nanoscale electrical modifications of SiO2/4H-SiC interfaces upon post-oxidation-annealing in N_2O and $POCl_3$*, Appl. Phys. Lett. **101**, (2012) art. N°. 193501.

10. P. Fiorenza, F. Giannazzo, L. K. Swanson, A. Frazzetto, S. Lorenti, M. S. Alessandrino, F. Roccaforte, *A look underneath the SiO_2/4H-SiC interface after N_2O thermal treatments,* Beilstein Journal of Nanotechnology **4**, (2013), 249-254.

11. P. Fiorenza, A. Frazzetto, L.K. Swanson, F. Giannazzo, F. Roccaforte, *A nanoscale look in the channel of 4H-SiC lateral MOSFETs* , Mat. Sci. Forum **740-742**, (2013) pp. 699-702.

12. P. Fiorenza, L.K. Swanson, M. Vivona, F. Giannazzo, C. Bongiorno, A. Frazzetto, F. Roccaforte, *Comparative study of gate oxide in 4H-SiC lateral MOSFETs subjected to post-deposition-annealing in N_2O and $POCl_3$*, Appl. Phys. A. **115,** (2014) 333–339.

13. P. Fiorenza, L. K. Swanson, M. Vivona, F. Giannazzo, C. Bongiorno, S. Lorenti, A. Frazzetto, F. Roccaforte, *Characterization of SiO_2/SiC interfaces annealed in N_2O or $POCl_3$,* Mat. Sci. Forum **778-780** (2014), 623-626.

14. M. Vivona, G. Greco, S. Di Franco, F. Giannazzo, F. Roccaforte, A. Frazzetto, S. Rascunà, E. Zanetti, A. Guarnera, M. Saggio, *Comparative study of the current transport mechanisms in Ni2Si Ohmic contacts on n- and p-type implanted 4H-SiC 4H-SiC,* Mat. Sci. Forum **778-780** (2014), 665-668.

15. P. Fiorenza, A. Frazzetto, A. Guarnera, M. Saggio, F. Roccaforte, *Fowler-Nordheim tunneling at SiO_2/4H-SiC interfaces in metal-oxide-semiconductor field effect transistors,* Appl. Phys. Lett. **105** (2014), 142108.