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REDUCTION OF SWITCHING LOSSES IN IGBT POWER MODULES

Tesi di Dottorato di Ricerca Internazionale in Energetica

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INTRODUCTION

Power modules are electronic components that are formed by semiconductor devices. These power devices have appeared on the market for the first time in 1975 and immediately have obtained a large success in the world of Power electronics.

Their applicability must be considered under the following aspects: "optimized" complexity of a module, heat dissipation capability, isolation voltage and partial discharge stability, static and dynamic symmetry of the structure, electromagnetic stability, defined and safe failure behavior, simple assembly and connection technology, low-polluting production and recyclability.

The purpose of this work is to study in deep the transition phenomena of IGBTs in order to evaluate different optimization strategies for losses reduction and propose a novel technique.

The IGBT devices are increasingly used in electronic circuits both for their ease of driving that for their ability to handle high currents and voltages at high switching frequencies.

Increasing devices switching speed is possible to reduce the power dissipation with the disadvantage of an increase of electromagnetic interference (EMI) and overcurrents. In fact, with increasing di/dt during switching transients EMI are increased, so it is necessary to specify the design of any power converter, the right tradeoff between switching speed, energy losses, EMI, overvoltages and overcurrents.

In electronic systems for power conversion, the driver circuit is the interface between the control circuit and power devices. The main function of the driver consists in amplifying the control signals, in order to supply the energy requested by the power devices to change their state from interdiction to saturation and vice-versa.

In power applications a particular attention must be taken to such phenomena as commutation losses, overcurrents during the turn-ON and overvoltage at the turn-OFF of the devices.

These phenomena are connected to non ideal behavior of real devices and stray circuit parameters. Steep profiles of current lead to large ElectroMagnetic Interference (EMI) and overvoltages, while rapid variations of the voltage can produce phenomena of "latch-up" in single IGBT or unwanted commutations. On the other hand, slow commutations are characterized by low values of dv/dt and di/dt, causing excessive losses in those power application during commutations.

One of the main goals in design the driver stages of power converters is the reduction of the commutation losses, obtaining remarkable benefits in terms of reduction of the dissipation and, consequently, the chance to increase the switching frequency. In order to reduce the commutation losses, the simplest way consists in shorting the time of commutation by rising the gate current lowering gate resistance value. These benefits are paid with the increasing complexity of the driving circuits, the greater difficulties in their design and higher final costs.

Therefore, it is essential to face the issue with opposite requirements at the design stage obtaining optimal tradeoff.

FIRST PART - THEORETICAL ASPECTS

CHAPTER 1 - IGBT

The **insulated-gate bipolar transistor** (**IGBT**) is a three-terminal power semiconductor device primarily used as an electronic switch and in newer devices is noted for combining high efficiency and fast switching. It is used in many modern applications: variable—frequency drives (VFDs), electric cars, trains, variable speed refrigerators, air-conditioners and even stereo systems with switching amplifiers. Since it is designed to turn ON and OFF rapidly, amplifiers that use it often synthesize complex waveforms with pulse width modulation and low-pass filters.

1.1. Controllable Switches

IGBTs are controlled switches, in which the "ON and OFF states" are fixed by a control signal. Ideally when the switch is open no current flows and when it is closed the current can flows in only one direction.

The most commonly used devices as switches in today's industrial applications are power BJT, MOSFET and IGBT.

The BJT and MOSFET Transistors are complementary in many aspects regarding their behavior.

In BJT the effect of base conductivity modulation means that the voltage drop between drain and source is small and independent of the collector current. This is due to the high number of minority carriers in the depletion region when the device operates in saturation, unless achieved particularly high injection levels. This means that the BJT have low conduction losses.

In MOSFET Transistors, larger values of output resistance ON-State and the absence of a conductivity modulation effect give rise the voltage drops between drain and source much more than BJTs. Consequently the conduction losses will be greater.

If in the BJT the output resistance and voltage drop, in saturation region, are independent of the size of the device that has tied the value of breakdown voltage, in the MOSFET these values depend on the technological characteristics of the device, such as doping and thickness of different layers. So the BJT although characterized by low values of resistance in conduction and high voltage blocking capabilities, have numerous limitations among which include the low switching speed and high current driving. The MOSFET overcome these problems in that they are driven in voltage with high switching speed, at the expense of conduction losses.

Then the MOSFET Transistors are better than BJTs.

The advantages of MOSFET Transistors are switching speed and the possibility of driving voltage devices. The benefit is a reduction in overall switching losses during power transients. The voltage control allows simple drivers because you can avoid to provide high current device.

IGBTs take the best part of these two types of transistor, the high input impedance and high switching speeds of a MOSFET with the low saturation voltage of a BJT and combines them together to produce another type of switching power device that is capable of handling large collector-emitter currents with virtually zero gate current drive.

The IGBT is a fairly recent invention. The first-generation devices of the 1980s and early 1990s were prone to failure through such modes as latchup (in which the device will not turn OFF as long as current is flowing) and secondary breakdown (in which a localized hotspot in the device goes into thermal runaway and burns the device out at high currents). Second-generation devices were much improved, and the current third-generation ones are even better, with speed rivaling MOSFETs, and excellent ruggedness and tolerance of overloads.

The IGBT combines the simple gate-drive characteristics of MOSFETs with the high-current and low-saturation-voltage capability of bipolar transistors. It combines an isolated gate FET for the control input, and a

bipolar power transistor as a switch, in a single device. The IGBT is used in medium mode power supplies, traction motor control and induction heating. Large IGBT modules typically consist of many devices in parallel and can have very high current handling capabilities in the order of hundreds of amperes with blocking voltages of 6000 V, equating to hundreds of kilowatts.

IGBT, for its structural and functional characteristics, is presented as a compromise solution between MOSFET and BJT combining the major qualities of both.
In the table 1 are shown the main advantages and disadvantages of the controlled devices.

	ADVANTAGES	DISADVANTAGES
BJT	Low conduction losses	Current driving Slow switching
MOSFET	Voltage driving Fast switching	High conduction losses
IGBT	Voltage driving Fast switching Low conduction losses High breakdown voltage	Latchup Current tail

Tab. 1 - Advantages and Disadvantages of controlled devices.

1.2. Architectural and Physical characteristics

The Insulated Gate Bipolar Transistor (IGBT) uses the insulated gate, hence the first part of its name, technology of the MOSFET with the output performance characteristics of a conventional bipolar transistor, hence the second part of its name. The result of this hybrid combination is that the "IGBT Transistor" has the output switching and conduction characteristics of a bipolar transistor but is voltage-controlled like a MOSFET.
IGBTs are mainly used in power electronics applications, such as inverters, converters and power supplies, were the demands of the solid state switching device are not fully met by power bipolars and power

MOSFETs. High-current and high-voltage bipolars are available, but their switching speeds are slow, while power MOSFETs may have high switching speeds, but high-voltage and high-current devices are expensive and hard to achieve.

The advantage gained by the insulated gate bipolar transistor device over a BJT or MOSFET is that it offers greater power gain than the bipolar type together with the higher voltage operation and lower input losses of the MOSFET. In effect it is an FET integrated with a bipolar transistor in a form of Darlington configuration as shown in Figure 1.

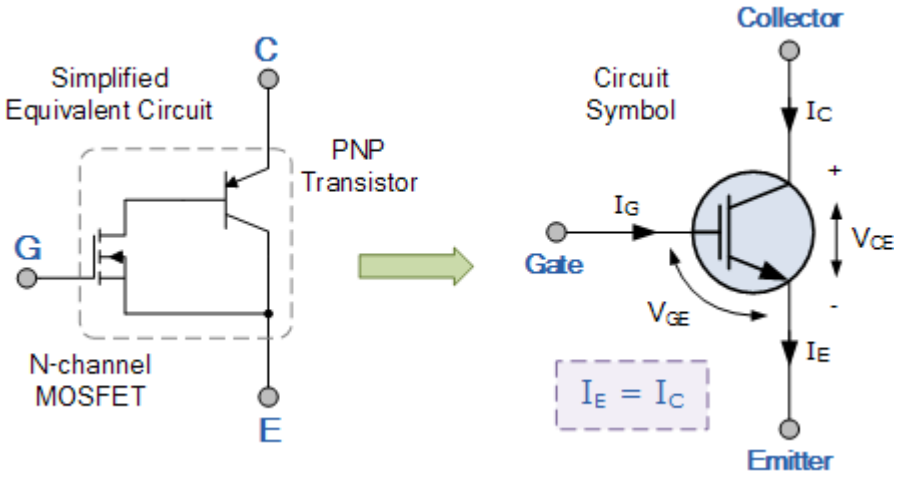

Fig. 1 - Circuit symbol of IGBT device.

It is possible to see that the insulated gate bipolar transistor is a three terminal, transconductance device that combines an insulated gate *n*-channel MOSFET input with a PNP bipolar transistor output connected in a type of Darlington configuration. As a result the terminals are labeled as: **Collector**, **Emitter** and **Gate**. Two of its terminals (C-E) are associated with a conductance path and the third terminal (G) associated with its control.

The Insulated Gate Bipolar Transistor can be used in small signal amplifier circuits in much the same way as the BJT or MOSFET type transistors. But as the IGBT combines the low conduction loss of a BJT with the high switching speed of a power MOSFET an optimal solid state switch exists which is ideal for use in power electronics applications.

When used as static controlled switch, the insulated gate bipolar transistor has voltage and current ratings similar to that of the bipolar transistor. However, the presence of an isolated gate in an IGBT makes it a lot simpler to drive than the BJT as much less drive power is needed.
An insulated gate bipolar transistor is simply turned "ON" or "OFF" by activating and deactivating its Gate terminal. A constant positive voltage input signal across the Gate and the Emitter will keep the device in its "ON" state, while removal of the input signal will cause it to turn "OFF" in much the same way as a bipolar transistor or MOSFET.

1.2.1. Basic structure

The IGBT is a semiconductor device with four alternating layers (P-N-P-N) that are controlled by a metal - oxide - semiconductor (MOS) gate structure without regenerative action.

Semiconductors are solids characterized by a band structure with a full valence band and a empty conduction band separated by a gap with an energy of the order of one or a few electron volts. At room temperature only a few electrons have sufficient energy to enter the empty band, so as to be able to conduct.
An important characteristic of semiconductors is also to have, in addition to electrons, a second type of charge carriers, able to generate a current: excited electrons into the conduction band leave the free states in the valence band, which allow for some mobility to other electrons left. This motion is described as the motion of a positive hole.
The main reason for which the semiconductors are so useful is that the conductivity of semiconductors can be modified with the addition of impurities (doping), with the action of an electric field, with exposure to light, or by other means.

With reference to the vertical section of a generic n-channel IGBT shown in the Figure 2(a) you can see the analogy with the typical structure of a vertical MOSFET in Figure 2(b). [3]

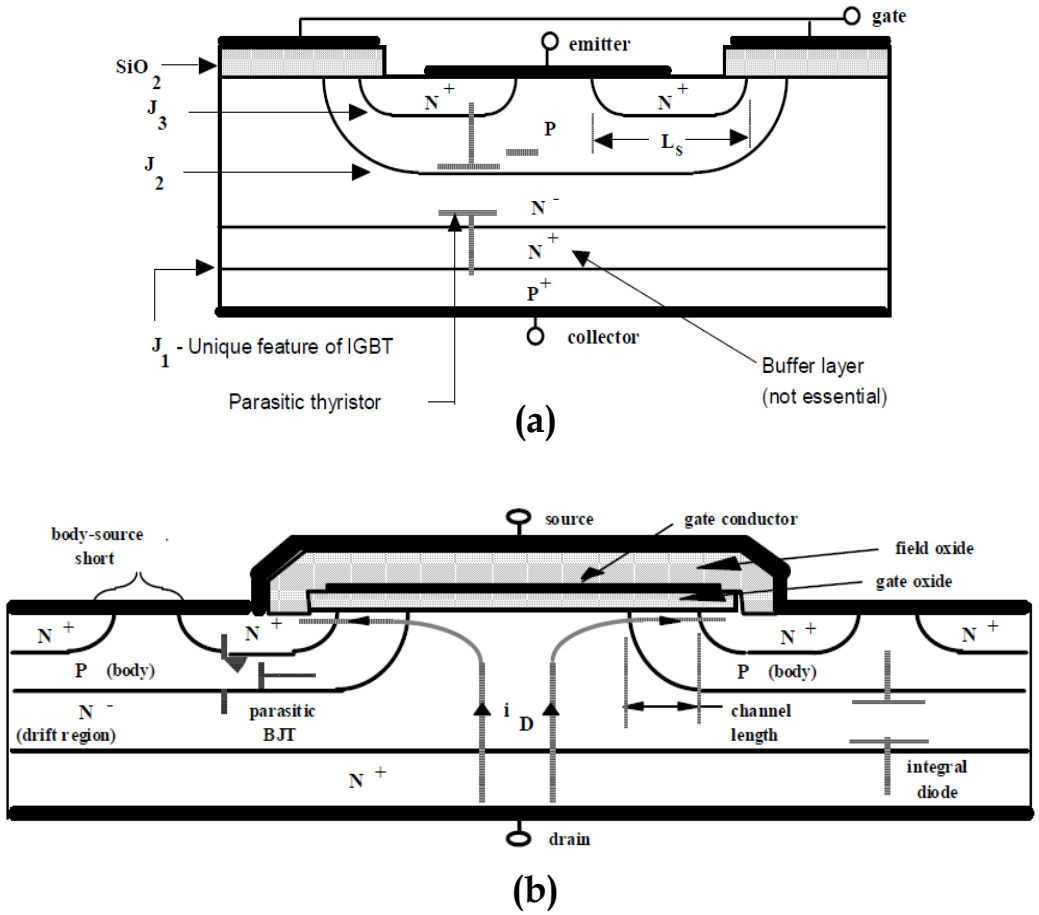

Fig. 2 - (a) Vertical section of an n-channel IGBT; **(b)** Vertical section of an n-channel MOSFET.

The main difference is the addition of a p^+ type layer which is the collector of the device. This layer forms with that above a *pn* junction and it is responsible for injecting minority carriers in n^+ and n^- layers which are in fact the drain region of a MOS structure with vertical development. The wide n^- region, known as the drift region or LDB (Low Doped Base), along with the body (*p*) and substrate (p^+) form a pn^-p^+ which can be considered as a *pnp* BJT.

The drift region (n^-) allows to the IGBT to withstand high voltages because lightly doped, while the n+ region has the dual function of controlling the gain of the transistor and to limit the emptying of the gate-collector

junction avoiding this reaches the emitter. Similar considerations apply for *p*-channel IGBT.

It is important to note that due to its intrinsic constitution, the structure of IGBTs contains a thyristor parasite whose activation is potentially destructive to the device. A constructive precaution aimed at reducing the probability of accidental ignition of the parasitic thyristor is to extend the emitter metallization above the body region.

The presence or absence of the layer n+ inside the structure of the device, classifies the IGBTs in two different types: [21]

- NPT IGBTs (Non Punch Through) without layer n^+;
- PT IGBTs (Punch Through) with layer n^+.

	NPT	PT
Switching Loss	MEDIUM Long tail current Moderate increase in E_{OFF} with temperature	LOW Short tail current Significant increase in E_{OFF} with temperature
Conduction Loss	MEDIUM Increases with temperature	LOW Flat to slight decrease with temperature

Tab. 2 - Characteristics Comparison of NPT and PT IGBTs.

So the IGBT can be seen how the connection of a Power MOS and a BJT *pnp* type whose base is connected to the drain of the PMOS. Therefore the IGBT presents the Power MOS characteristics in the input and the BJT characteristics in the output.

A general comparison between BJT's, MOSFET's and IGBT's is given in the following table 3.

	BJT	MOSFET	IGBT
Voltage Rating	High < 1kV	High < 1kV	Very High > 1kV
Current Rating	High < 500A	Low < 200A	High > 500A
Input Drive	Current 20-200 h_{FE}	Voltage V_{GS} 3-10V	Voltage V_{GE} 4-8V
Input Impedance	Low	High	High
Output Impedance	Low	Medium	Low
Switching Speed	Slow (µs)	Fast (ns)	Medium
Cost	Low	Medium	High

Tab. 3 - Comparison between IGBT, MOSFET and BJT devices.

We have seen that the Insulated Gate Bipolar Transistor is semiconductor switching device that has the output characteristics of a bipolar junction transistor, BJT, but is controlled like a metal oxide field effect transistor, MOSFET.

One of the main advantages of the IGBT transistor is the simplicity by which it can be driven ON or OFF or in its linear active region as a power amplifier. With its lower ON-state conduction losses and its ability to switch high voltages without damage makes this transistor ideal for driving inductive loads such as coil windings, electromagnets and DC motors.

1.2.2. IGBT characteristics

As shown in Figure 3, the current-voltage characteristics of an n-channel IGBT device appear similar to those of a BJT (the region of direct polarization), except for the control parameter that is the voltage between gate and emitter (V_{GE}) instead of the gate current.

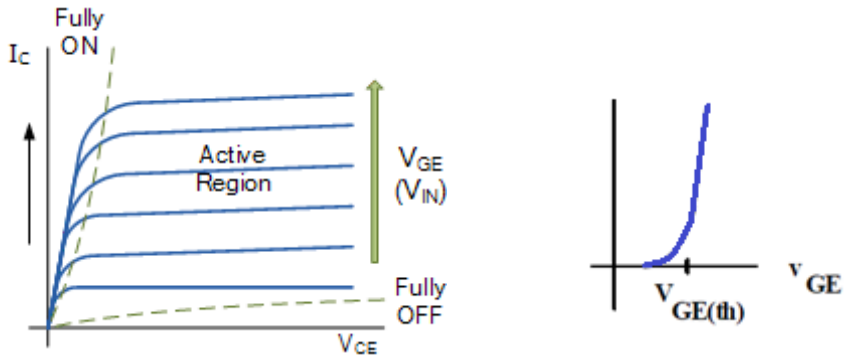

Fig. 3 - Current- Voltage characteristics of IGBT devices.

The curve is linear in the range of allowed values of the V_{GE} above the threshold voltage $V_{GE(th)}$. After the curve is not linear. The $V_{GE(th)}$ represents the value of voltage applied between the collector and emitter that separates the ON state ($V_{GE} > V_{GE(th)}$) from the OFF state ($V_{GE} < V_{GE(th)}$).

Because the IGBT is a voltage-controlled device, it only requires a small current on the Gate to maintain conduction through the device unlike BJT's which require that the gate current is continuously supplied in a sufficient enough quantity to maintain saturation.

Also the IGBT is a unidirectional device, meaning it can only carries the current in the "forward direction", that is from Collector to Emitter unlike MOSFET's which have bi-directional current switching capabilities (controlled in the forward direction and uncontrolled in the reverse direction).

The principal of operation and Gate drive circuits for the Insulated Gate Bipolar Transistor are very similar to that of the *n*-channel power MOSFET. The basic difference is that the resistance offered by the main conducting channel when current flows through the device in its "ON" state is very much smaller in the IGBT. Because of this, the current ratings are much higher when compared with an equivalent power MOSFET.

The main advantages of using the Insulated Gate Bipolar Transistor over other types of transistor devices are its high voltage capability, low ON-resistance, ease of drive, relatively fast switching speeds and combined with zero gate drive current makes it a good choice for moderate speed, high voltage applications such as in pulse-width modulated (PWM),

variable speed control, switch-mode power supplies or solar powered DC-AC inverter and frequency converter applications operating in the hundreds of kilohertz range.

1.2.3. Comparison with Power MOSFET

An IGBT features a significantly lower forward voltage drop compared to a conventional MOSFET in higher breaking down voltage rated devices. As the blocking voltage rating of both MOSFET and IGBT devices increases, the depth of the n^- drift region must increase and the doping must decrease, resulting in roughly square relationship decrease in forward conduction versus breaking down voltage capability of the device. By injecting minority carriers (holes) from the collector p^+ region into the n^- drift region during forward conduction, the resistance of the n^- drift region is considerably reduced. However, this resultant reduction in ON-state forward voltage comes with several penalties:

- The additional *pn* junction blocks reverse current flow. This means that unlike a MOSFET, IGBTs cannot conduct in the reverse direction. In bridge circuits, where reverse current flow is needed, an additional diode (freewheeling diode) is placed in parallel with the IGBT to conduct current in the opposite direction. The penalty isn't overly severe because at higher voltages, where IGBT usage dominates, discrete diodes are of significantly higher performance than the body diode of a MOSFET.
- The reverse bias rating of the n^- drift region to collector p^+ diode is usually only of tens of volts, so if the circuit application applies a reverse voltage to the IGBT, an additional series diode must be used.
- The minority carriers injected into the n^- drift region take time to enter and exit or recombine at turn ON and turn OFF. This results

in longer switching times, and hence higher switching loss compared to a power MOSFET.

- The ON-state forward voltage drop in IGBTs behaves very differently from power MOSFETs. The MOSFET voltage drop can be modeled as a resistance, with the voltage drop proportional to current. By contrast, the IGBT has a diode-like voltage drop (typically of the order of 2V) increasing only with the log of the current. Additionally, MOSFET resistance is typically lower for smaller blocking voltages, so the choice between IGBTs and power MOSFETs will depend on both the blocking voltage and current involved in a particular application.

In general, high voltage, high current and low switching frequencies favor IGBTs while low voltage, low current and high switching frequencies are the domain of the MOSFET.

1.3. Operating mode

From an operational point of view, the IGBT can be regarded as constituted by an *n*-channel MOS in input and by a *pnp* BJT in output. The two devices are connected in Darlington configuration (Fig. 1), act as a primary device (BJT) and driver (MOS) respectively.

The MOS section determines the state of IGBT's operation, while the BJT section determines the blocking voltage between Collector and Emitter or the transport of charge between them, according to the mode in which the device is to operate (OFF/ON).

1.3.1. Block mode operation (OFF state)

In the OFF state, the behavior of an IGBT is equal to that of a MOSFET.

The voltage applied between the Gate and Emitter determines the status of the device. For values of $V_{GE}<V_{GE(th)}$ there isn't formation of the inversion layer in the section of the MOSFET in input. In these conditions, the IGBT is turned OFF, the voltage between Collector and Emitter of the *pnp* bipolar transistor of the output section is supported by the p^+n^- junction, in Figure 2(a) is J_2 junction. The doping level of the p^+ and n^- regions is fixed so as to extend the depletion region of the junction J_2 inside the drift region.

You can see that the maximum voltage applied between Collector and Emitter of the IGBT depends on the thickness of the drift region, which must contain the depletion region J_2. If the layer of n^+ type was absent, so for a NPT IGBT, the capacity to block reverse depends on the depth of the drift region, and can be made equal to that direct.

The ability to direct sealing of the device depends on the characteristics of the drift region: greater is its thickness, the higher is the value of the voltage that the device can support in the output. Unfortunately, the same parameter is also linked to the resistance value of the collector-emitter path in the ON state, increasing with it. In NPT devices an increased ability to block direct the device produces an increase in the output resistance in the ON state and therefore an increase of conduction losses. In PT devices you exceed this problem by introducing a thin n^+ layer in the p^+ region of the collector when the value of the output voltage exceeds the limit value of the thickness of the n^- layer. In this way, in the PT devices is possible to realize a drift region thinner than that of a NPT IGBT, maintaining the same output voltage.

The advantage is in the reduction of conduction losses, the disadvantage is a reduced of blocking reverse ability.

1.3.2. Conduction mode operation (ON state)

In the ON state, there are the working mechanisms of the MOS and BJT. In Figure 4 is described the operation of the ON state of an IGBT. [3, 10]

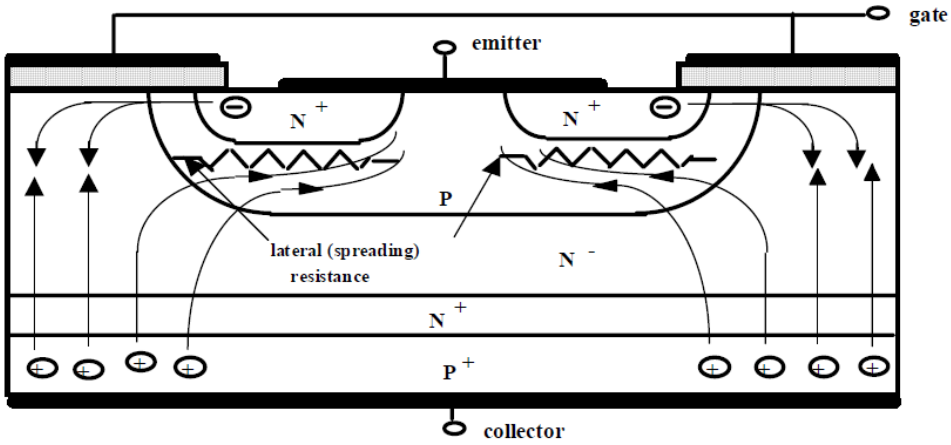

Fig. 4 - Conduction mode operation of the IGBT.

When the $V_{GE}>V_{GE(th)}$ you can see the formation of an inversion layer charge in the body region under the Gate contact. For high values of V_{GE} the *n*-channel puts into short-circuits the drift region (n^-) and the Emitter region (n^+). The result is an electron current flowing from one region to another through the *n*-channel, like a MOSFET. But the IGBT has another layer of p^+ type. This layer produces an injection of positive charges that can make up for the electron flow generated in the upper layers. The holes move through the drift region is to diffusion that derives in various directions. So you can see how the structure formed by the body, the drift region and the drain behaves as a bipolar transistor *pnp* type.

It is thus justified the Darlington configuration used to represent the IGBT shown in Figure 1, while in Figure 5 are shown, with the respective symbols, the MOS and BJT sections present in the device.

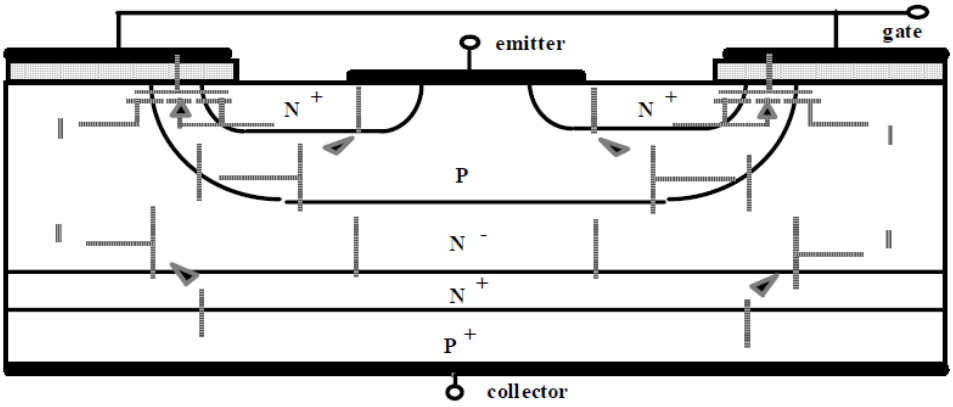

Fig. 5 - MOS and BJT section into IGBT.

In the IGBT, the voltage drop which has in conduction state is smaller than that of a PowerMOS of equal characteristics.

To understand the reason, should be considered the intrinsic voltage drops that occur between the Collector and Emitter. Applying Kirchoff's law is obtained by the following relationship:

$$V_{CE(ON)} = V_{p^+n} + V_{drift} + V_{ch}$$

The V_{p+n} is a typical bias voltage of the *pn* junction and its value is approximately in the range 0.7 - 1.0 V. The V_{drift} is much smaller than that of the Power MOS due to an effect of conductivity modulation of the drift region due to the injection of minority carriers from the p^+ region, as happens in the BJT. The V_{ch} depends on the ohmic resistance of the channel and it is the same like a MOSFET. The effect is to reduce the voltage drop at the output of the IGBT device compared to Power MOS.

1.4. Operating faults: the Latch-up

The IGBT contains a parasitic *pnpn* thyristor structure between the Collector and the Emitter.

A latch-up means the turning ON of the thyristor. When there is action by a thyristor, the IGBT current is no longer controlled by the MOS gate. The IGBT would be destroyed because of excessive power dissipation

produced by the amount of current over the rated value between the Collector and the Emitter.

During ON-state, paths for current flow in an IGBT are shown in Figure 4. The holes are injected into the n^- drift region from the p^+ collector form two paths. Part of the holes disappear by recombination with electrons came from MOSFET channel. Other part of holes are attracted to the vicinity of the inversion layer by the negative charge of electrons, travel laterally through the *p*-body layer and develops a voltage drop in the ohmic resistance of the body. This voltage tends to forward bias the n^+p junction and if it is large enough, substantial injection of electrons from the emitter into the body region will occur and the parasitic NPN transistor will be turned-ON. If this happens, both NPN and PNP parasitic transistors will be turned-ON and hence the thyristor composed of these two transistors will latch on and the latchup condition of IGBT will have occurred. Once in latchup, the gate has no control on the collector current and the only way to turn-OFF the IGBT is by forced commutation of the current, exactly the same as for a conventional thyristor.
If latchup is not terminated quickly, the IGBT will be destroyed by the excessive power dissipation. IGBT has a maximum allowable peak drain current (I_{CM}) that can flow without latchup. Device manufacturers specify this current level in the datasheet. If this current level is exceeded in static conditions, with the device in the permanent ON state, a large enough lateral voltage drop will activate thyristor and the latchup of IGBT.

In Figure 6 is shown a circuit model of the IGBT which concerns the phenomenon of latchup and the parasitic thyristor which generates it.
In dynamic conditions (Figure 7), during switching, the value of the collector current in which occurs the latchup is lower than that recorded in static conditions. During turn OFF, in fact, the rapid switching OFF of the MOS part of the device and resetting of the current through this part produce a sudden increase of the voltage on the collector supported by the

pn-junction formed by the drift region and body region, inversely polarized. [3, 21]

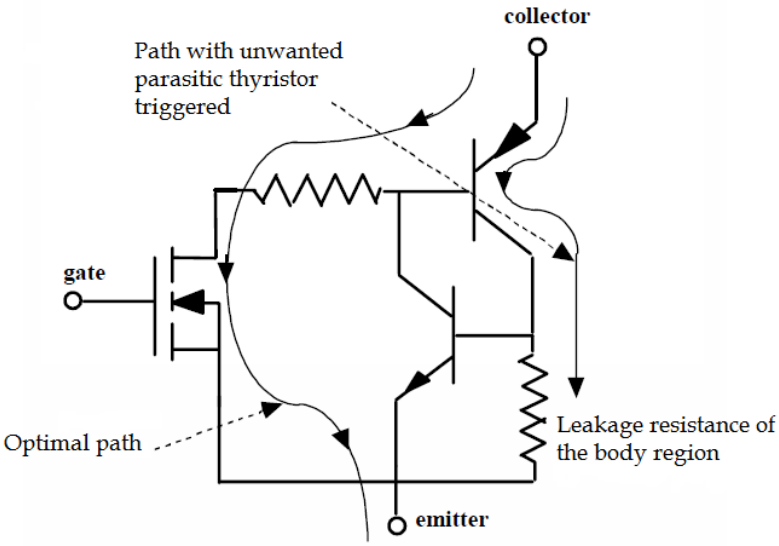

Fig. 6 - Equivalent circuit with parasitic thyristor.

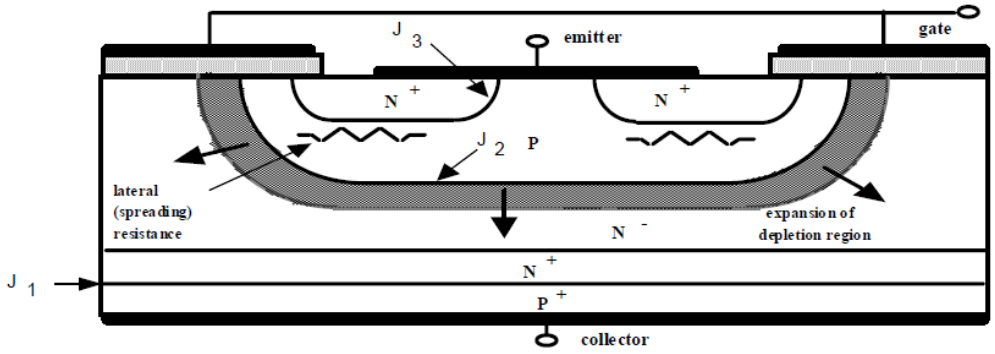

Fig. 7 - Expansion of the depletion region in the drift region, which can cause latchup dynamic.

There are two approaches to reduce the probability of initiation of the parasitic thyristor and the consequent destruction of the device latchup. The first one, the technology, is to adopt a series of constructive measures designed to reduce the value of the leakage resistance of the body which is associated with the potential drop which triggers the phenomenon.

The second one, that user, involves the design of mechanisms that on the one hand prevent the occurrence of static and dynamic overcurrent, on the other hand slow turn OFF of the device so as to reduce the expansion speed of the depletion region in the drift region so that the holes can recombine before you get to body. But excessive slowing of the switching of the device results in an excessive increase of the switching losses.

An increase in the gate resistance due to a slowing down of switching, from the ON state to the OFF state or vice versa. Since the dynamic latchup only affects the process of switching off, it is useful to decouple the resistive check on the gate by introducing two different resistors, one for power ON and one for power OFF. This allows it to act directly on the speed of the IGBT switching OFF without interfering with the switching ON.

These solutions may be insufficient to find a good compromise between the many conflicting requirements related to the switching of the devices and of which latchup and switching losses represent only one part.

The aim of this work is to find the right tradeoff by designing a good driving circuit for IGBT.

1.5. Switching characteristics

The switching characteristics of an IGBT are very much similar to that of a Power MOSFET. The major difference from MOSFET is that it has a tailing collector current due to the stored charge in the n^- drift region. The current tail increases the turn OFF loss and requires an increase in the dead time between the conduction periods of two devices in a half-bridge circuit.

Consider the vertical section of an *n*-channel IGBT shown in Figure 8.

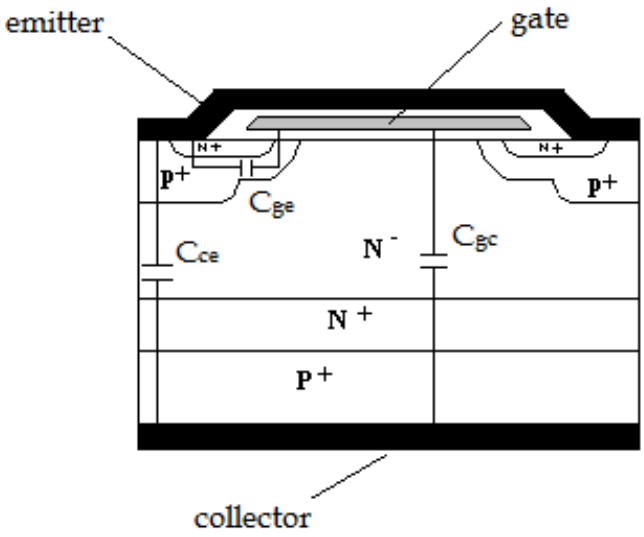

Fig. 8 - Parasitic capacitances in the IGBT.

There are many parasitic capacitive phenomena that influence the switching transients. They may, however, be traced back to three fundamental capabilities: C_{ce}, C_{ge} and C_{gc}.

The first one concerns all parasitic capacitive effects between Collector and Emitter of the device, the second one relates the parasitic capacitive effects between Gate and Emitter of the device and the third one concerns the parasitic capacitive effects between Gate and Collector of the device.

The C_{ce} can be ignored because it doesn't affect the switching characteristics. Instead, the capacity C_{ge} and C_{gc} aren't constant during turn ON and turn OFF, but changes with the voltage applied to them. The most significant changes affecting the C_{gc} as the voltage jump which it is subject during a switching is far higher than the C_{ge}. So the variations of C_{gc} are the only ones which are taken into account in the analysis of transient. They are continuous and non-linear as is shown in Figure 9.

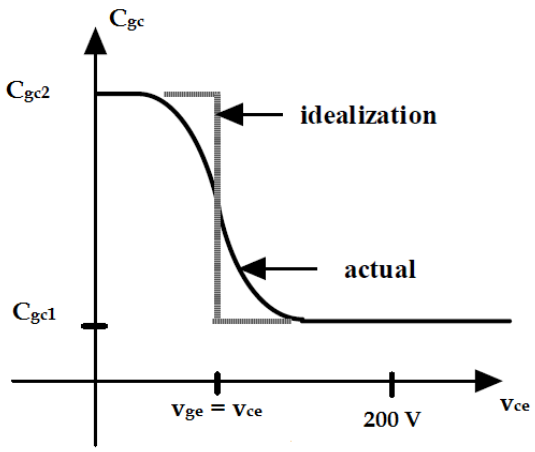

Fig. 9 - Variation of C_{gc} depending on the voltage between collector and emitter.

For simplicity, in order to calculate the waveforms of switching, it was considered appropriate to identify the C_{gc} with two discrete values: C_{gc1} and C_{gc2}, one of starting and the other of arrival. The transition from one value to another occurs the instant that the v_{ce} and the v_{ge} are equal. This is the moment of entry or exit of the device from the ohmic region.

In Figure 10 is shown the circuit commonly used to study the switching behavior of a generic power IGBT and reproduces the working conditions of a device inserted in a DC-DC converter or an inverter. This circuit allows us to measure the electrical quantities during the switching transient, as well as the energy losses.

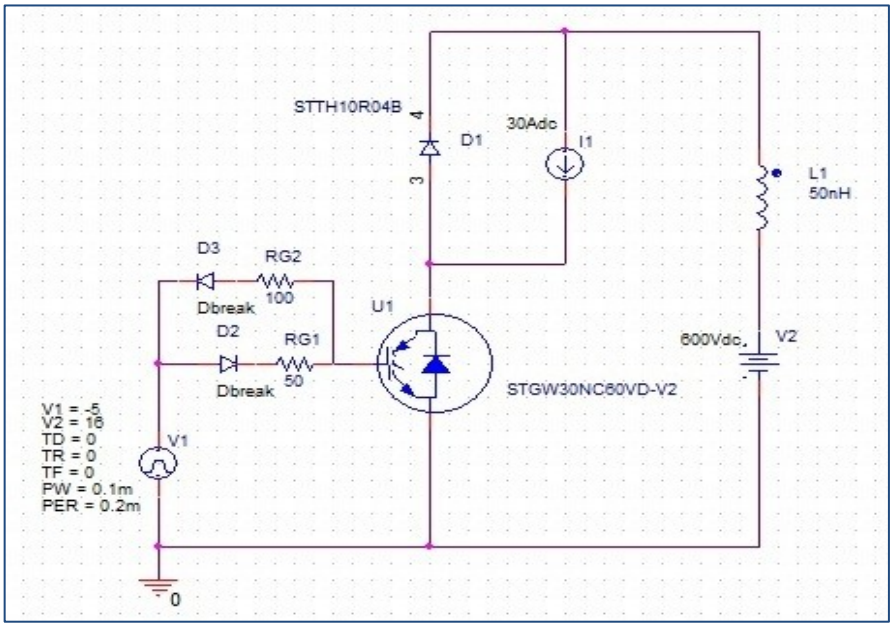

Fig. 10 - Generic circuit to study the switching behavior of IGBTs.

The current generator I_1 ideally represents an inductive load as, for example, an electric motor. It can be assumed, approximately, that the current through the load during a switching cycle is constant. This current is imposed on the circuit due to the highly inductive nature of the load and the energy stored in it. Hence the use of the ideal current generator to model the inductive load.

The recirculation diode D_1 is connected in antiparallel to the load in order not to pass current when the load is powered.

The gate resistors R_{G1} and R_{G2} work by controlling parameter on the speed of transition between ON and OFF states and their value strongly influences the output gradient of the voltage and the current (*dv/dt* and *di/dt*) in the process of switching.

The ideal voltage generator V_1 provides pulses of appropriate amplitude acts to force the switching. It represents the real driving circuit of the device (*driver*).

The generator V_2, however, provides blocking voltage of the device during turn OFF transition.

The device U_1 is the IGBT under test.

1.5.1. Turn ON

The following figure shows the waveforms of the voltage and current that characterize the transition from the OFF to the ON states of the IGBT operating in an inverter. [1, 11, 16, 17, 18]

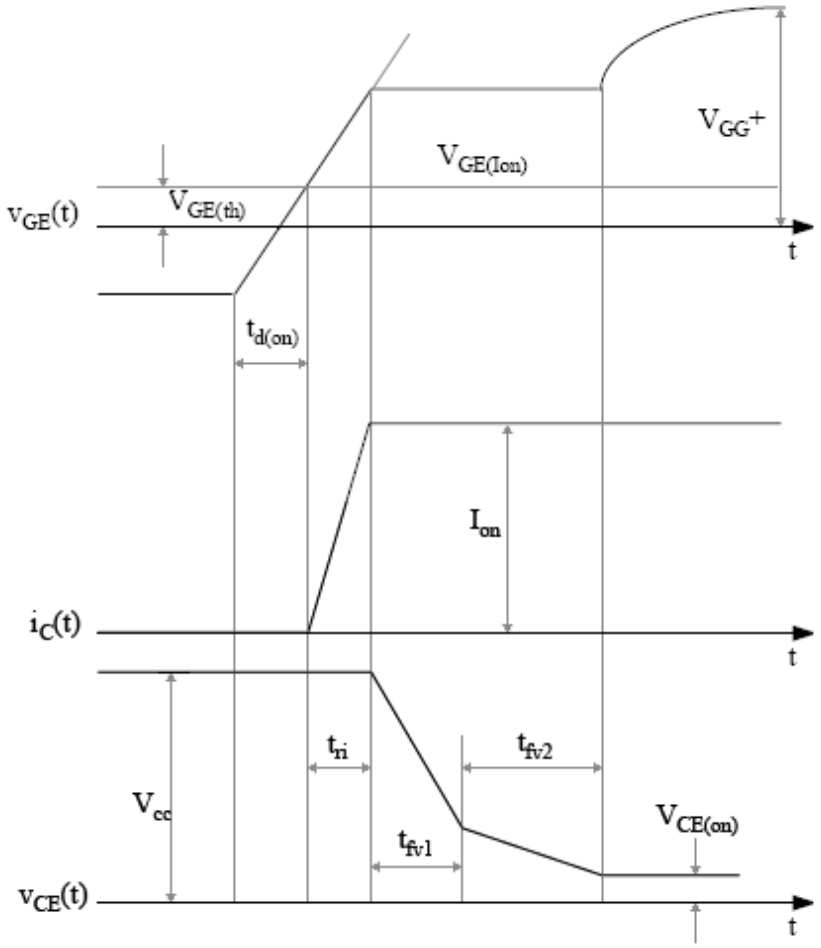

Fig. 11 - Turn ON characteristics of an ideal IGBT.

Assuming at first $V_{GE} = 0$ and assuming that at time t = 0 the generator V_1 (V_{GG}) imposes a positive voltage step of amplitude greater than the threshold voltage $V_{GE(th)}$ will see the evolution of the electrical quantities of the input and output shown in the Figure 11.

During the delay time $t_{d(on)}$ the voltage $V_{GE(t)}$ increases from zero to $V_{GE(th)}$ due to the currents that flow in the capacity C_{ge} and C_{gc}.

The pattern in which the $V_{GE(t)}$ grows can be considered approximately linear, although it is to be understood as the initial part of an exponential with a slope given by the time constant

$$\tau_1 = R_G(C_{ge} + C_{gc1}).$$

In this first phase the $V_{GE(t)}$ changes, while collector voltage and current do not change. When the gate voltage reaches the threshold begins a second phase of the turn ON indicated by the time lag t_{ri}. The instant in which the

gate voltage equals the threshold value, the collector current starts to grow.

In the ideal case, the effects of overcurrents related to secondary phenomena are ignored (reverse recovery current of a not ideal diode), for which the collector voltage is constant until the current is not equal to its static value in the ON mode (I_{on}). In the real case, however, these effects are evident and consequently also the collector voltage has the same problems. The following figure shows interference of the real case.

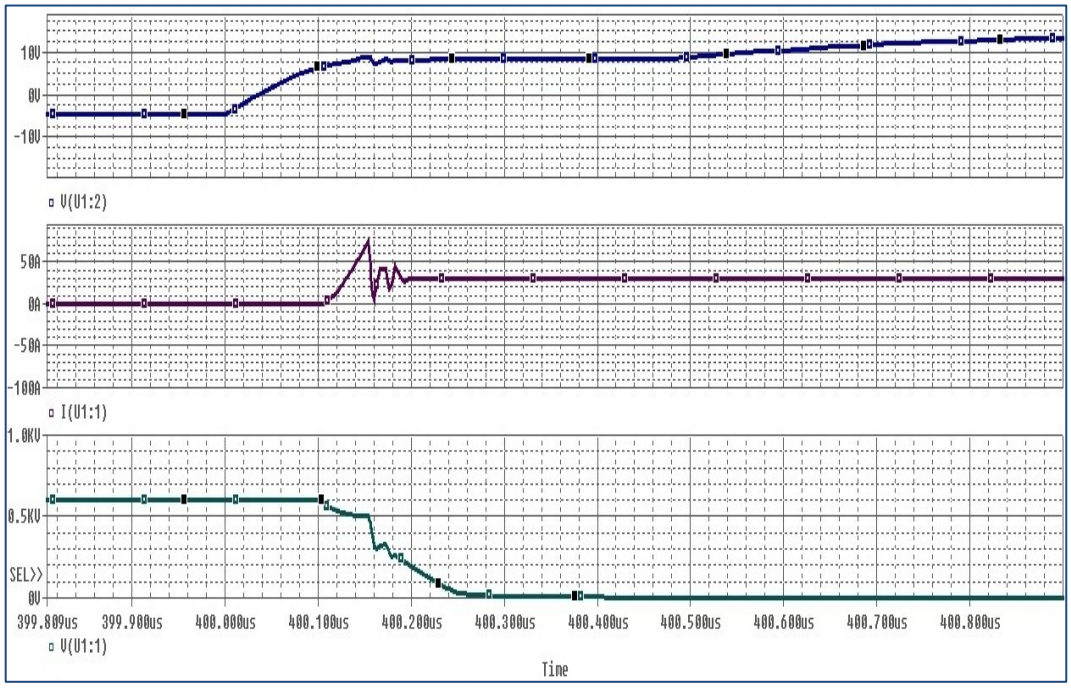

Fig. 12 - Turn ON characteristics of an real IGBT. The blue waveform represents the gate voltage, the violet waveform the collector current and the green waveform represents the collector voltage.

Just finishing the transient current, start a third phase of switching in which the gate voltage stands at a constant value. This value is necessary to sustain the collector current I_{on}.

The time interval during which the gate voltage is constant is called *Region of Miller*. This assumes a very important role in the development of optimization techniques for the control of IGBT devices. The duration of this interval is equal to $t_{fv1} + t_{fv2}$.

As mentioned previously, the gate voltage is constant in Miller region. In t_{fv1} happens a rapid decrease of the output voltage. In t_{fv2} the $V_{CE(t)}$

continues to decrease but with different slope. In fact, at this stage, it is assumed that the device is entered in the ohmic region, and, as mentioned previously, the final value of the C_{gc} is equal to C_{gc2}. The decrease in the slope of the $V_{CE(t)}$ must be attributed to the increase of C_{gc}.

The C_{gc} changes continuously and not linear between the minimum and the maximum value identified by C_{gc1} and C_{gc2}. This phenomenon is called *Miller Effect*. Outside the Region of Miller the voltage between gate and emitter to grow back to move to the value imposed by the generator input.

The time constant with which the VGE evolves exponentially towards its final value is

$$\tau_2 = R_G(C_{ge} + C_{gc2}).$$

While the voltage between Collector and Emitter is equal to $V_{CE(on)}$.

In power applications, where the devices are used in switching mode, at the end of turn ON is always $V_{GE} >> V_{GE(th)}$.

From all this it is clear that the voltage and current gradients are dependent on the gate resistance R_G. A reduction of R_G involves an increase of the speed of switching and vice versa.

The R_G as the only control parameter represents a limit. In fact, an increase in the *dv/dt* by a reduction of the R_G, at turn OFF, contributes to the reduction of the switching losses. But the reduction of R_G increases the *di/dt* that can generate overvoltages and electromagnetic interference (EMI) unwanted. Similar words apply to the turn ON. So a need to develop techniques capable of influencing separately control the profiles of voltage and current. The aim of this work is to explore these possibilities.

1.5.2. Turn OFF

For the study of the switching OFF of an IGBT is possible to follow a similar approach to turn ON. In this phase, the device presents a

phenomenon known as current tail which determines a significant slowdown with a consequent increase of the switching losses. [1, 11, 16, 18] The test circuit used is the same (Figure 10).

The following figures show the waveforms of the voltage and current that characterize the transition from the ON to the OFF states of the IGBT operating in an inverter. In Figure 13 the ideal behavior and in Figure 14 the real behavior of an IGBT.

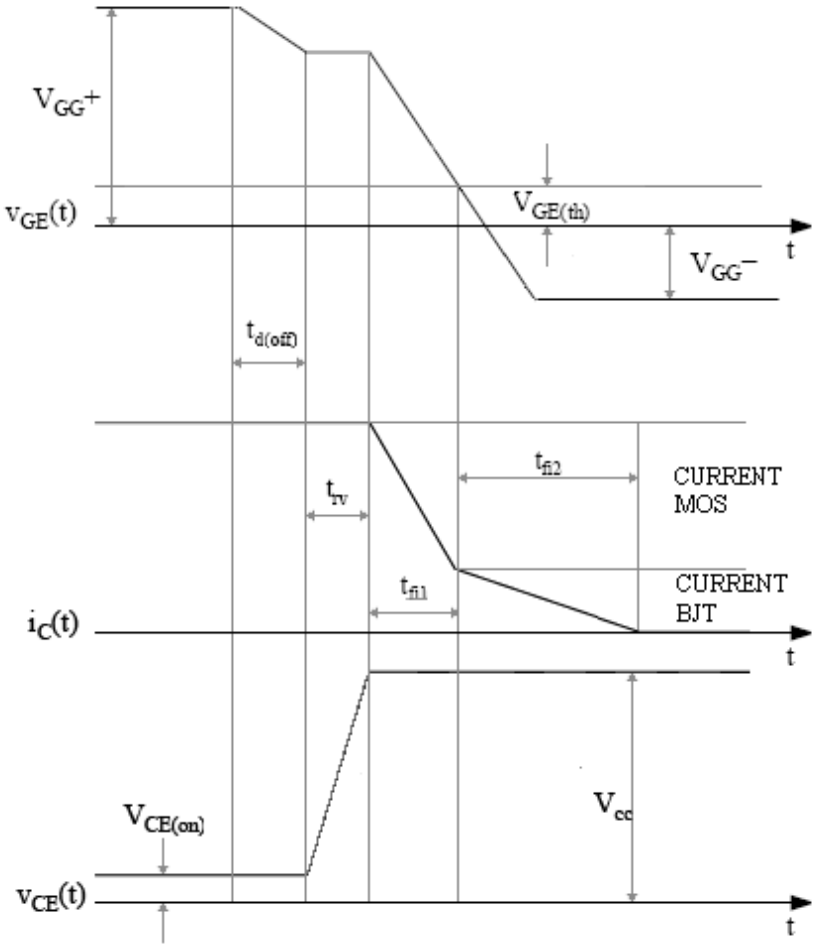

Fig. 13 - Turn OFF characteristics of an ideal IGBT.

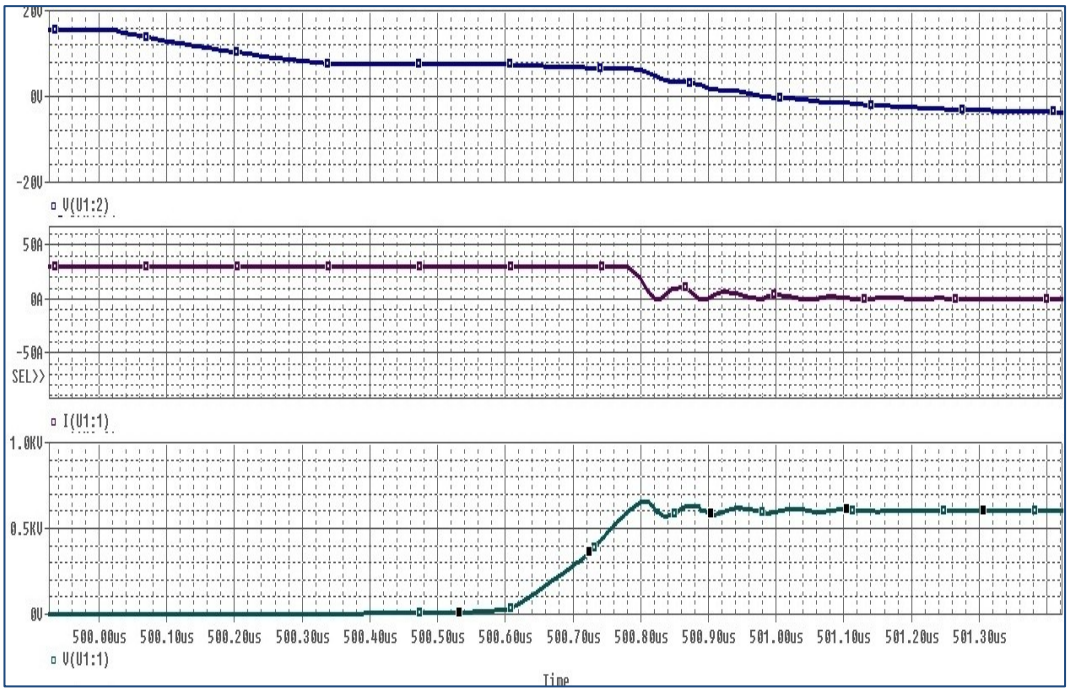

Fig. 14 - Turn ON characteristics of an real IGBT. The blue waveform represents the gate voltage, the violet waveform the collector current and the green waveform represents the collector voltage.

From a qualitative assessment has perfect symmetry between ON and OFF states in relation to the sequence of events and the evolution of the variables, except for the final stretch (interval t_{fi2}). In a totally specular to turn ON, the instant witch the driver force a negative step on the gate, the voltage V_{GE} starts to decrease at an exponential rate and the time constant related to the parasitic capacitances C_{gc} and C_{ge}.

During the interval $t_{d(off)}$, the collector voltage and the current remain unchanged and the only electrical quantity that changes is the V_{GE}. After reaching the threshold $V_{GE(th)}$, the V_{GE} stands at V_{Miller} constant value as in power ON. In the range of Miller (t_{rv}) the collector current is constant while the collector voltage V_{CE} changes.

In the ideal case being absent overvoltages tied to parasitic inductances present in the power side of the circuit, the collector voltage reaches its final value in correspondence of the Miller region. At the same time the extinction of the voltage transient begins the current transient. This starts to decrease in two phases: t_{fi1} and t_{fi2}.

In the interval t_{fi2} the current has a sharp reduction in slope that causes a slowdown in switching. This phenomenon is caused by the bipolar section

of the IGBT. That is, the positive charges trapped in the drift region in the second phase of the power OFF. In fact, the MOS section of the device, very fast, is the first to turn OFF. At the end of t_{fi1} can be closed switching of the input section of the IGBT.

This happens before the charges present in the drift region have had time to drain away. The timing and effectiveness are related to the life time of the excessive charges. The life time is linked to the value of $R_{CE(on)}$. The higher the life time of the charges and the lower the $R_{CE(on)}$, and the smaller the conduction losses. It is therefore necessary to find a compromise between:

- contain the conduction losses through a reduction in $R_{CE(on)}$;
- contain the switching losses by reducing the lifetime of excess carriers.

It is also noted that the phenomenon of the current tail is characterized by a positive temperature coefficient. The duration of the phenomenon increases with increasing temperature, which in turn depends on the power dissipated. This increases with the current tail. So it triggers a dangerous process that leads to the destruction of the IGBT. It is appropriate to find a compromise position between two features. The solutions to the problem of the current tail can be found exclusively in technology.

1.5.3. High temperature characteristics

The minority carrier lifetime in the drift region increases as the temperature increases. This not only delays recombination process (current tail) of the minority carrier, but it also increases the PNP transistor gain. So the portion of the initial abrupt fall in the overall collector current reduces. As such, t_f (fall time) of the spec is lengthened, and turn-OFF time increases with an increase in temperature.

1.5.4. Real or Ideal behavior of the IGBT

Ideally the power devices must be able to tolerate high voltages in the OFF state, conduct high currents with low voltage drops in the ON state and be able to quickly switch between ON and OFF states.
An ideal switch must have the following characteristics:

- Blocking direct and reverse voltages of any magnitude without conducting current in the OFF state;
- Conducting any current with no voltage drop across its terminals in the ON state;
- Switch from ON to OFF and vice versa quickly;
- Request small quantity of power for driving.

All real devices show a behavior that is very different from the ideal one. In particular, commutations not instantaneous, a voltage drop different from zero in the ON state and small leakage current in the OFF state produce a power dissipation due to joule effect, which in extreme cases can lead to destruction of the device to excessive overheating.

1.6. Operation Losses

An ideal totally controlled device has the following features:

- It is able to withstand direct and reverse voltages of any amplitude with zero current in OFF state;
- It conducts currents of any amplitude with insignificant voltage drop;
- It is able to instantly switch from ON to OFF states and vice versa;
- It absorbs powers negligible for the trigger.

The real devices haven't these characteristics and, therefore, during operation they have losses that can irreversibly destroy itself. [1, 3, 11, 16, 17, 18]

In Figure 15 is shown a complete switching cycle for a generic switch.

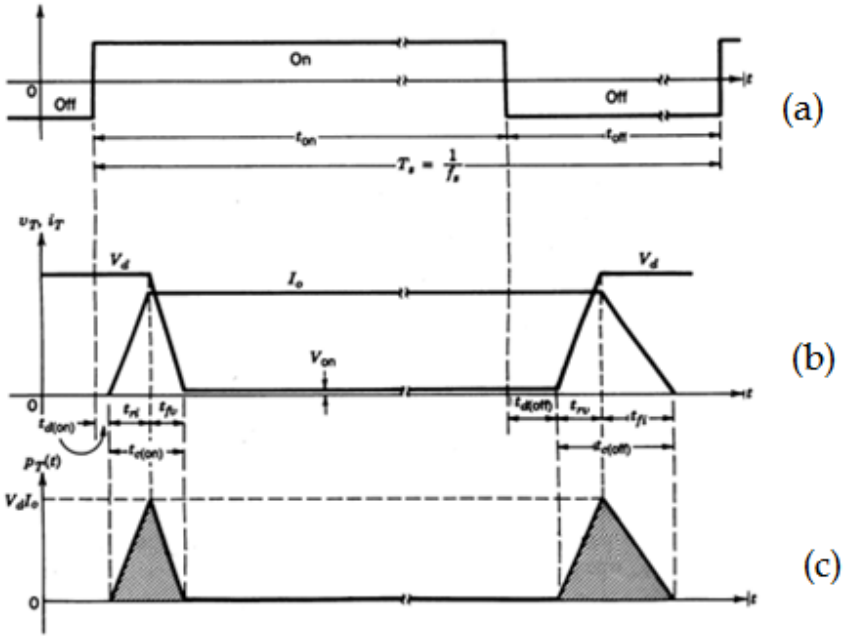

Fig. 15 - Switching characteristics and relative loss in a controlled device.

For simplicity, we consider ideal devices so that the waveforms are linearized and neglect secondary phenomena which can be overcurrents during turn ON and overvoltages during turn OFF.

In Figure 15 are shown: (a) the signal input of the switching, (b) the electrical characteristics, (c) the power and the energy losses.

During power up, after a delay time $t_{d(on)}$ with respect to the application of the step voltage on the gate, begins the current transient to reach the steady-state value I_0. For the duration of the current transient t_{ri}, the output voltage is unchanged. Once the current transient has ended the output voltage reaches the steady-state value $V_{CE(on)}$ during the time period t_{fv}. It is evident that for a time equal to $t_{c(on)} = t_{ri} + t_{fv}$ the device is having to support a current and a voltage simultaneously different from zero.

Under the hypothesis of linear waveform characteristics, this involves a dissipation of energy that can be quantified by the following relation:

$$W_{c(on)} = \frac{1}{2} V_d I_0 t_{c(on)}$$

The same happens to turn OFF and the dissipated energy is described by the following equation:

$$W_{c(off)} = \frac{1}{2} V_d I_0 t_{c(off)}$$

During the conduction phase the current is equal to I_0. This generates a small voltage drop $V_{CE(on)}$ which depends on the output resistance of the device in the ON state.

The energy dissipated during the conduction mode is given by:

$$W_{on} = V_{on} I_0 t_{on}$$

The sum of the three energies gives us the value of the total energy lost during a switching cycle.

Figure 15(c) shows the waveform of the instantaneous power lost during a complete switching cycle, obtained as the product of current and voltage. The average value of the lost power is obtained by multiplying the energy expenditure in a switching cycle for the working frequency of the switch f_s. The average power dissipated is approximately given by:

$$P_S = \frac{1}{2} V_d I_0 f_S (t_{on} + t_{off})$$

The power lost due to non-ideal switching devices depends linearly on the frequency. So, to reduce switching losses involves a dual advantage. In fact, if the frequency f_s remains constant efficiency of the device increases, because it will be subject to less thermal stress. Conversely, for the same maximum power lost, it is possible to increase the working frequency as required by modern control techniques.

In conduction mode, the average power dissipated is given by:

$$P_{on} = V_{on} I_0 f_S t_{on}$$

It can be considered negligible the contribution of the leakage current in the OFF state. So, the total average power dissipated by a switch is equal to:

$$P_T = P_S + P_{on}$$

From the expressions derived for the switching and conduction losses, can be easily deduce the desirable features for a switch:

- low values of the reverse current;
- low values of the voltage drop to reduce the conduction losses;
- switching times $t_{c(on)}$ and $t_{c(off)}$ very small in order to use the device at high values of f_s;
- ability to conduct high current values and to support high values of reverse voltage;
- low values of power to switch the device;
- ability to withstand the rated voltage and current at the same time to avoid the use of external protection circuits ("snubber" circuits);
- ability to withstand high values of *di/dt* and *dv/dt* to avoid the use of external circuits for their limitation.

1.6.1. Operation losses of an IGBT

Now we can calculate the losses in an IGBT. To make a realistic estimation some not-ideal characteristics should be taken into account. For this reason, the test circuit to which reference should be made now, shown in Figure 16, takes into account the parasitic inductances in the current paths causing overvoltage shutdown. It will not also neglected the reverse recovery current of the freewheeling diode, due to overcurrent at turn ON. [4]

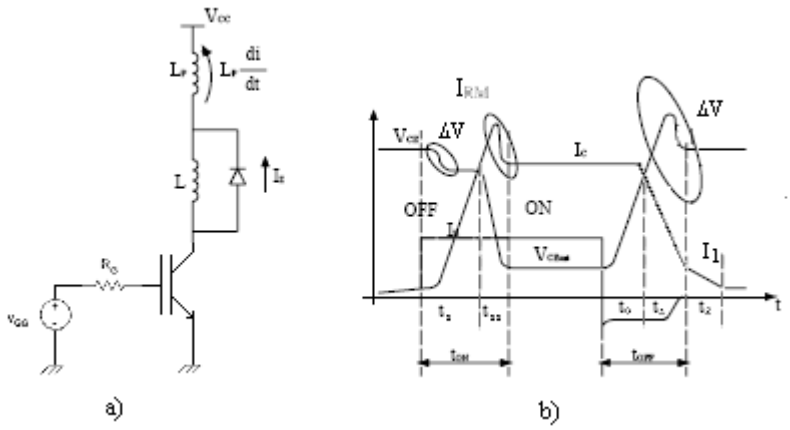

Fig. 16 - a) Test circuit with parasitic inductance; b) Output current and voltage during switching.

The energy lost in power ON is given by:

$$W_{c(on)} = \frac{1}{2}(V_{CE} - \Delta V)(I_C + I_{RM})(t_r + t_{rr})$$

I_{RM} introduces the contribution given by the not ideal recirculation diode. In fact, the I_C has an overshoot with respect to the steady-state value due to the reverse recovery current of the diode. This overcurrent is linked to the *di/dt*. The V_{CE} has a small negative step ΔV before dropping the final saturation value. The ΔV, takes into account the voltage drop across parasitic inductance L_p. So the voltage across the device becomes:

$$V_{CE} = V_{CC} - L_p \frac{di}{dt}$$

The average power dissipation is obtained by multiplying $W_{c(on)}$ for f_s, thus obtaining:

$$P_{c(on)} = \frac{1}{2}(V_{CE} - \Delta V)(I_C + I_{RM})(t_r + t_{rr})f_S$$

At turn OFF the energy lost is given by the sum of the contributions for the three time intervals t_0, t_1 and t_2. t_0 and t_1 characterize the switching OFF of the MOS section of the IGBT, while t_2 is related to the effect of the current tail in the drift region. The total energy lost in power down is:

$$W_{c(off)} = W_{c(t_0)} + W_{c(t_1)} + W_{c(t_2)}$$

$$W_{c(off)} = \frac{1}{2}[I_C V_{CE} t_0 + (I_C + I_1)(V_{CE} + \Delta V)t_1 + I_1 V_{CE} t_2]$$

The average power dissipation is obtained by multiplying $W_{c(off)}$ for f_s, thus obtaining:

$$P_{c(off)} = \frac{1}{2}[I_C V_{CE} t_0 + (I_C + I_1)(V_{CE} + \Delta V)t_1 + I_1 V_{CE} t_2] f_S$$

1.6.2. Reduction of Overcurrent at Turn-ON

The gate resistor (R_G) controls the IGBT collector current slope. The choice of this resistor is based on a compromise between reduced power consumption (which requires a low value of R_G) and a tolerable *dv/dt* or *di/dt* in order to limit the peak current due to the recovery diode and the electromagnetic interference (EMI) generation requiring a high value of R_G. The latching current depends upon the gate resistance value. The manufacturers suggest a minimum gate resistance value to avoid the latching phenomenon. IGBT drivers are generally implemented using two resistors: one resistor is employed at turn-ON and the other one for turn-OFF. Advanced methods are proposed to limit *di/dt* and *dv/dt* based on the feedback control of the IGBT collector current or the collector voltage slope. However, it is not easy to achieve these complex methods, which require considerable silicon area.

In order to protect the IGBT from over-current, risk of latch-up and to limit the EMI, without incurring any increase in the values of gate resistance and the power consumption, the gate voltage must be increased in two separate stages. By increasing the gate to an intermediate stage for a short time before the final turn-ON, the IGBT collector current and its slope *di/dt* are limited. Hence, the peak current due to the diode reverse recovery is reduced.

1.6.3. Reduction of Overvoltage at Turn-OFF

If there is a short-circuit or over-current in the load, a large voltage overshoot can occur across the IGBT at turn-OFF and can exceed the IGBT breakdown voltage. It is proposed to drive the IGBT by applying a signal on the gate with two different stages. By reducing the gate voltage to an intermediate level for a short time before the final turn-OFF, the IGBT collector current is limited and hence the potential overshoot is reduced.

1.6.4. Conduction losses and Switching losses

At any given time, the energy dissipated in the IGBT can be obtained with the following expression:

$$E = \int_0^t V_{CE}(i) i(t) dt$$

where t is the length of the pulse. Power is obtained by multiplying energy by frequency, if applicable. When the transistor is OFF $i(t)$=0 and losses are negligible. Unfortunately, no simple expression can be found for the voltage and current functions when the IGBT is conducting. Hence, for analytical expediency, we resort to the distinction between conduction and switching losses.

Defining conduction losses the losses that occur between the end of the turn-ON interval and the beginning of the turn-OFF interval, as defined for the switching losses characterization. Since the turn-ON energy is measured from 5% of the test current to 5% of the test voltage and the turn-OFF energy is measured starting from 5% of the test voltage, conduction losses occur when the voltage across the IGBT is less than 5% of the test or supply voltage. The function $V_{CE(i)}$ in the formula above characterizes the conduction behavior of the IGBT.

Losses in hard switching have been broken down into two components: turn-ON and turn-OFF losses, as described in paragraph 1.5.

1.7. Problems related to *dv/dt*

The operation of an IGBT can meet a series of issues related to high values of *dv/dt*. You can have two cases.

- ***dv/dt* in static conditions**

We talk about *dv/dt* in static conditions when an IGBT that is in OFF state suffers a transient variation of its collector voltage. This change of voltage is reflected in input through the capacity C_{gc} and C_{ge}, generating a voltage change on the gate able to turn ON the device. Another effect is due to the possible activation of the parasitic thyristor which can destroy the device.

- ***dv/dt* in dynamic conditions**

The *dv/dt* belongs to the operation of any switch. During turn OFF of an IGBT can be seen a rapid expansion of the depletion region which causes an unwanted peak current. This creates the conditions for the occurrence of latch-up.

1.8. Safe Operating Area (SOA)

The safe Operating Area (SOA) is defined as the current-voltage boundary within which a power switching device can be operated without destructive failure. For IGBT, the area is defined by the maximum Collector-Emitter voltage V_{CE} and collector current I_C within which the IGBT operation must be confined to protect it from damage. The IGBT has the following types of SOA operations: Forward-Biased Safe Operating Area (FBSOA), Reverse-Biased Safe Operating Area (RBSOA) and Short-Circuit Safe Operating Area (SCSOA). [3, 21]

The IGBT has robust SOA both during turn ON and turn OFF. Figure 17 (a) shows the FBSOA. On the left side it is restricted by the forward voltage drop characteristics. Up to maximum continuous collector current this voltage remains reasonably constant at a low value. However, at I_{CM} this

voltage starts increasing as the IGBT starts entering active region. On the top the FBSOA is restricted by I_{CM}.

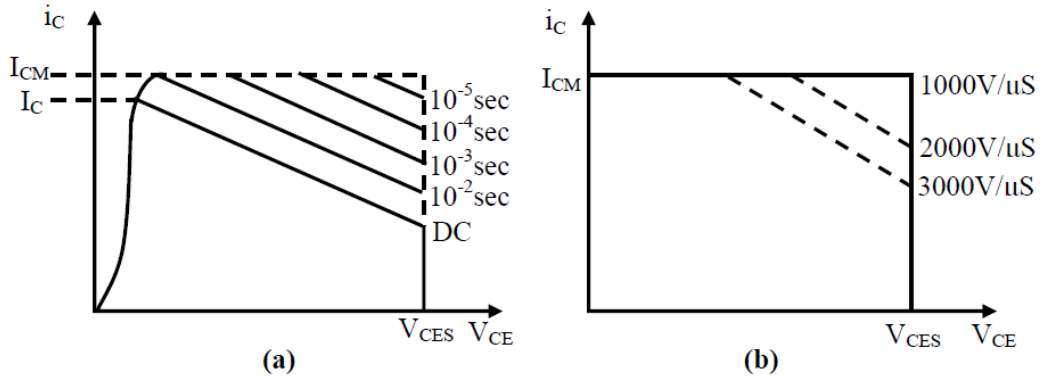

Fig. 17 - Safe operating area of an IGBT. (a) FBSOA; (b) RBSOA.

The other two limits are formed by the maximum power dissipation limit and the maximum forward voltage limit. Like other devices the maximum power dissipation limit increases with reduction in the on pulse width.

The RBSOA for low values of *dv/dt* is rectangular. However, for increased *dv/dt* the upper-right hand corner is progressively cut out. The reason for this restriction on the RBSOA is to avoid dynamic latch-up. The device user can easily control *dv/dt* by proper choice of V_{gg} and the gate drive resistance.

A very important requirement imposed on the power switching device, when used in motor control applications is that be able to turn-OFF safely due to a load or equipment short circuit. When a current overload occurs, collector current rises rapidly until it exceeds that which the device can sustain with the applied gate voltage. The key to survivability for the power device is to limit the current amplitude to a safe level for a period of time that is sufficiently long to allow the control circuit to detect the fault and turn the device OFF.

1.9. Application Area of IGBT

In a social background where it is indispensable to take action concerning the environment, power devices have the main role of efficiently using resources and energy in power electronics, and are thus growing increasingly more important.

Based on offering power devices designed for "low power loss" and "miniaturization," the companies dealing to produce intelligent power modules, which are at the forefront of the inverter products market.

The main criteria in choosing either IGBT or MOSFET are voltage rating, power losses (efficiency of the whole system) and of course the cost of the whole system. Choosing one over other may impact not only losses in the transistors but also the weight and cost of cooling, size of the complete product and also reliability so sometimes e.g. a weight constrain may force you to use MOSFET instead of IGBT. [1]

Looking at the graph below, you will see different areas, where each type of switch are typically used:

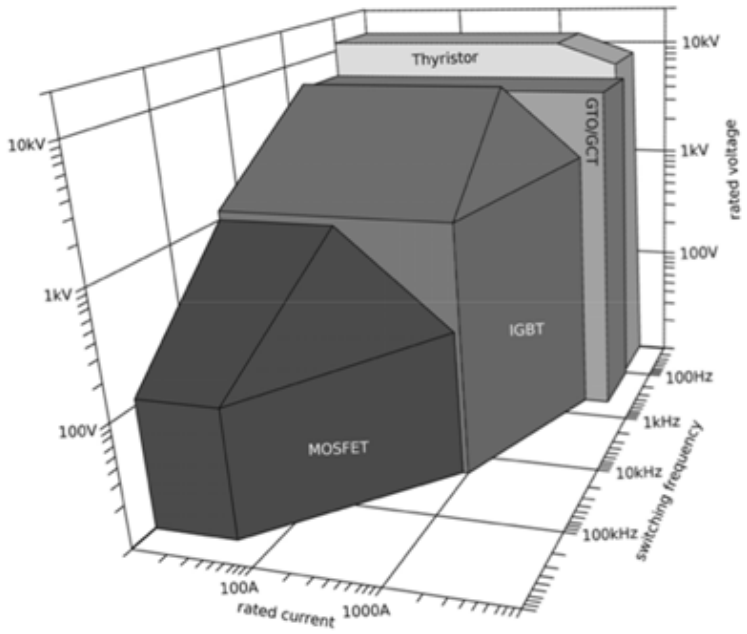

Fig. 18 - Current/Voltage/switching frequency domains of the main power electronics switches.

Choosing a particular device type depends on specific application and its requirements.

MOSFETs dominate in high frequency and low current applications because they can switch extremely fast and act as resistance when ON. Fast switching means they are used when the device has to be small as when you increase switching frequency you can reduce the size of passive filters.

The conduction losses are proportional to the square of drain current and therefore you cannot pass huge current through the structure.

So the power MOSFET has the advantages of a majority carrier device, so it can achieve a very high operating frequency, but it cannot be used with high voltages; as it is a physical limit, no improvement is expected in the design of a silicon MOSFET concerning its maximum voltage ratings. However, its excellent performance in low voltage applications make it the device of choice for applications with voltages below 200 V. By placing several devices in parallel, it is possible to increase the current rating of a switch. The MOSFET is particularly suited to this configuration, because its positive thermal coefficient of resistance tends to result in a balance of current between the individual devices.

IGBTs have higher breakdown voltage and conduction losses are approximately equal to V_f*I_c therefore you can use them in high current applications. They have limited switching speed therefore they are typically used in industrial applications where low switching frequency is not a problem (acoustical noise).

The IGBT is a relative recent component, so its performance improves regularly as technology evolves. It has already completely replaced the bipolar transistor in power applications; a power module is available in which several IGBT devices are connected in parallel, making it attractive for power levels up to several megawatts, which pushes further the limit at which thyristors and GTOs become the only option. Basically, an IGBT is a bipolar transistor driven by a power MOSFET; it has the advantages of being a minority carrier device (good performance in the ON-state, even

for high voltage devices), with the high input impedance of a MOSFET (it can be driven ON or OFF with a very low amount of power).

The major limitation of the IGBT for low voltage applications is the high voltage drop it exhibits in the ON-state. Compared to the MOSFET, the operating frequency of the IGBT is relatively low (usually not higher than 50 kHz), mainly because of a problem during turn-OFF known as current tail. The slow decay of the conduction current during turn-OFF results from a slow recombination of a large number of carriers that flood the thick 'drift' region of the IGBT during conduction. The net result is that the turn-OFF switching loss of an IGBT is considerably higher than its turn-ON loss. Generally, in datasheets, turn-OFF energy is mentioned as a measured parameter; that number has to be multiplied with the switching frequency of the intended application in order to estimate the turn-OFF loss.

CHAPTER 2 - THE DRIVER

In Power Electronics, a **driver** is an electrical circuit or other electronic component used to control another circuit or other component, such as a high-power transistor.

They are usually used to regulate current flowing through a circuit or is used to control the other factors such as other components, some devices in the circuit. The term is often used, for example, for a specialized integrated circuit that controls high-power switches in switched-mode power converters. An amplifier can also be considered a driver for loudspeakers, or a constant voltage circuit that keeps an attached component operating within a broad range of input voltages.

Typically the driver stage of a circuit requires different characteristics to other circuit stages. For example in a transistor power amplifier, typically the driver circuit requires current gain, often the ability to discharge the following transistor bases rapidly, and low output impedance to avoid or minimize distortion.

A generic power system can be represented by the following block diagram.

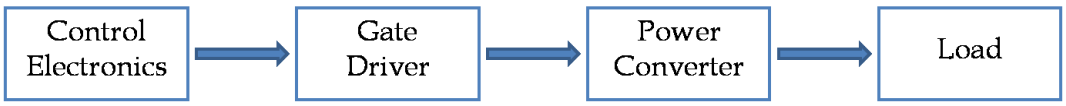

Fig. 19 - Block diagram of a generic electronic power system.

The first block represents the control of the system, where they are generated logic signals to the Gate Driver. The second block consists to the Gate Driver. The third block is a converter. Finally, the last block, represents the load that is placed downstream of the power converter.

In electronic systems for power conversion, the driver circuit is the interface between the control circuit and the switching devices. Its main function is to amplify a control signal, suitably generated, in order to provide the necessary energy to the devices to force the switching ON and OFF. A driver must also ensure the electrical insulation between the

power section of the converter and the section containing the processing circuits of the logic signals.

A good driving circuit must possess certain essential requirements such as:

- Possibility of supplying to the gate of the switch sufficiently high current to ensure fast switching times.
- Minimization of switching losses.
- Protection devices from overcurrent and overvoltage.
- Negative voltage for a rapid and stable power OFF devices reducing the probability of spurious triggering due to *dv/dt*.
- Control of Electromagnetic Interference (EMI) related to the *di/dt*.
- Protection from latchup phenomenon for driving IGBT.
- In systems based on isolated gate devices, ability to deliver high peak currents during the initial phase of the switching and maintain high voltage drop between the gate and emitter at low current.
- Electrical isolation between input and output.

Depending on the type of application, some of the above requirements become more critical compared to other.

In high power applications must be given special attention to the switching losses, overcurrents at turn ON and overvoltages at turn OFF.

These phenomena are connected to the waveforms of the voltage and current transient. Steep profiles of current can cause ElectroMagnetic Interference (EMI) and overvoltages, while rapid variations of the voltage can produce phenomena of "latch-up" in single IGBT or unwanted commutations. On the other hand, slow commutations are characterized by low values of *dv/dt* and *di/dt*, causing excessive losses in those power application during commutations.

One of the main goals in the design of the driver stages of power converters is the reduction of the commutation losses, obtaining remarkable benefits in terms of reduction of the dissipation and,

consequently, the chance to increase the switching frequency. In order to reduce the commutation losses, the simplest way consists in shorting the time of commutation by rising the gate current lowering gate resistance. These benefits are paid with the increasing complexity of the driving circuits, the greatest difficulties in their design and the final costs higher. Therefore, it is essential to face the issue at the design stage with opposite requirements obtaining optimal tradeoff.

2.1. IGBT driver design considerations

When designing and building driver circuits for an IGBT, the following will need to be taken in to consideration to prevent unwanted voltage spikes, oscillation or ringing, and false turn-ON.

a. Layout
b. Power supply by-passing
c. Mismatch of driver to the driven IGBT/MOSFET

To ensure a robust and problem free IGBT driver, designers are advised to pay close attention to what is recommended in the next few paragraphs.

Layout

A very crucial point is proper grounding. A very low-impedance path for current return to ground avoiding loops is a good design practice. The three paths for returning current to ground are between:

1. Driver and the logic driving it;
2. Driver and its own power supply;
3. Driver and the source/emitter of the IGBT being driven.

All these paths should be very short in length to reduce inductance. Also, these paths should be as wide as possible to reduce resistance. In addition, these ground paths need to be kept separate to avoid returning ground current from the load to affect the logic line. It is very important to note

that all ground points in the circuit should return to the same physical point to avoid generating differential ground potentials.

Power Supply By-Passing

Since turning an IGBT ON and OFF amounts to charging and discharging large capacitive loads, the peak charge current need to be within the capability of drive circuit. At the same time the driver will have to draw this current from its power supply in a short period of time. This means that using of proper by-pass capacitors for the power supply becomes very important. A pair of by-pass capacitors of at least 10 times the load capacitance with complementary impedance, used in parallel and very close to the V_{CC} pin, can take care of this issue. These by-pass capacitors should have the lowest possible equivalent series resistance (ESR) and equivalent series inductance (ESL) and the capacitor lead lengths should be as short as possible.

Mismatch of Driver to the Driven IGBT

Since all IGBT driver I_{Cs} have some losses, it is necessary to calculate the power dissipated in the driver for a worst-case condition. The total power dissipated in the IGBT driver I_C is:

$$P_{gate-driver(tot)} = P_{Output} + P_{Emitter} + P_{Internal}$$

Since ambient temperature in the vicinity of the IGBT driver will have an effect on the actual power dissipation capability of the driver, the maximum allowable power dissipation at this temperature will need to be derated accordingly (in comparison to room temperature).

2.2. Structural features

Driver circuits are most commonly used to amplify signals from controllers or microcontrollers in order to control power switches in

semiconductor devices. Driver circuits often take on additional functions which include isolating the control circuit and the power circuit, detecting malfunctions, storing and reporting failures to the control system, serving as a precaution against failure, analyzing sensor signals, and creating auxiliary voltages.

2.2.1. Primary side of driver circuit

On the primary side of the IGBT driver circuit, input signals are received and error signals are sent back to the controller.
Signal processing that takes place on the primary side of the driver circuit enables short pulse suppression in order to minimize glitches, prevention of IGBTs turning on simultaneously so to avoid short circuits and monitoring of temperature and undervoltages.

2.2.2. Isolation between primary and secondary sides

Isolation of primary and secondary sides of the driver circuit is generally accomplished by use of transformers or optocouplers (LEDs and phototransistors). Typical driver circuits can withstand voltages of 2500 V between the primary and secondary side.
Some simple driver circuits forego the isolation between the primary and secondary sides, leaving this task in the hands of the user.

2.2.3. Secondary side of driver circuit

On the secondary side of the driver circuit, input signals are amplified and used to control the switching of the IGBTs. Overcurrents are monitored to detect shorts in the power circuit. This is done by either comparing the Collector-Emitter voltage V_{CE} to a preset threshold or by monitoring the signal of a current sensor.

If overcurrent occurs, the secondary side of the driver switches all the IGBTs OFF and sends an error signal to the primary side.

2.2.4. Isolation of the triggering signal using an optocoupler

Optocouplers are often used in place of transformers to isolate signals. An optocoupler is made up of an LED (Light Emitting Diode) and a light sensitive transistor (phototransistor) all in one package.

In general, optocouplers are inferior to transformers since they display higher susceptibility than transformers, less durability, limited performance, and limited isolation voltage.

SECOND PART - EXPERIMENTAL ASPECTS

CHAPTER 3 - DRIVING TECHNIQUES

In order to introduce advanced driving techniques a standard hardswitching circuit has been considered as a reference to measure the electrical quantities during the switching transients, as well as to evaluate the energy losses, with different values of the gate resistance.
The considered gate resistance values are: 33Ω, 47Ω, 68Ω and 100Ω.

The IGBT under test is STGW40V60DF - V3, provided by ST Microelectronics.

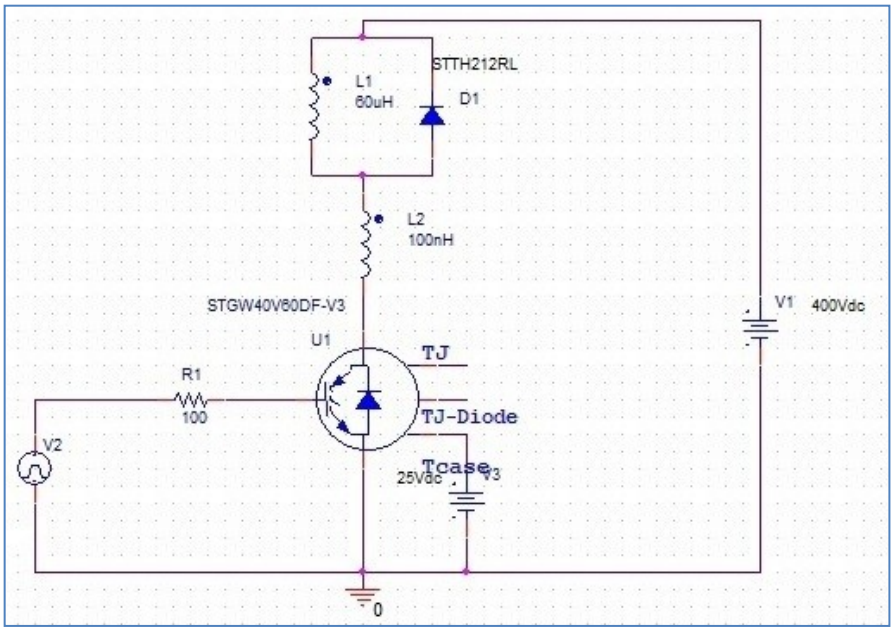

Fig. 20 - Basic circuit with Rg= 100Ω.

3.1. Driving open loop - Hardswitching

The simplest way to force the switching of a power device is to apply a voltage step on the gate without bothering to dynamically control the evolution of the output variables in the transient. The method provides as a single control parameter the value of the gate resistance R_G.
A first step towards the optimization of the driving circuit is to use two different values of gate resistance for Turn-ON and Turn-OFF. The purpose is to keep within acceptable limits the *dv/dt* during Turn-OFF in

order to avoid phenomena of "latching" or spurious switching of the device.

For these reasons must be $R_{G(OFF)} > R_{G(ON)}$.

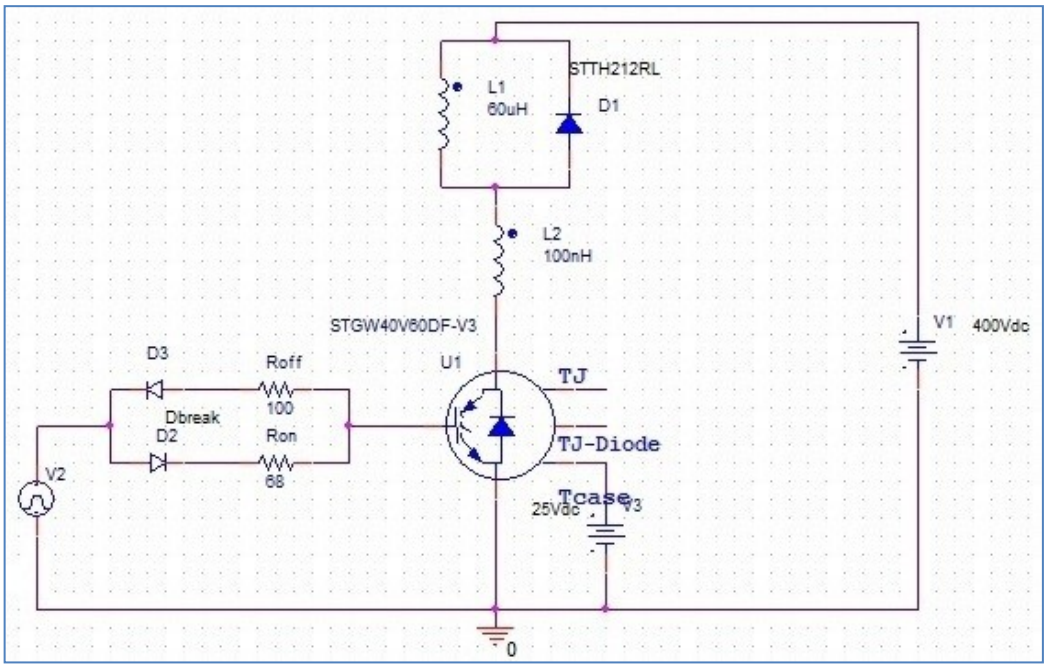

Fig. 21 - Circuit with driver in Hardswitching with $R_{G(ON)}$=68Ω and $R_{G(OFF)}$=100Ω.

The generator input V_2 strength a power ON and a power OFF through a rectangular pulse voltage of -15V/+15 V and the duration of 6μs. Two different values of the gate resistance have been chosen for the switching ON and OFF. The inductor L_1 is an inductive load; the diode D_1 represents the recirculation diode of the upper device in half-bridge configuration; the inductor L_2 is parasitic effects of the line; the generator V_1 provides the blocking voltage to the device.

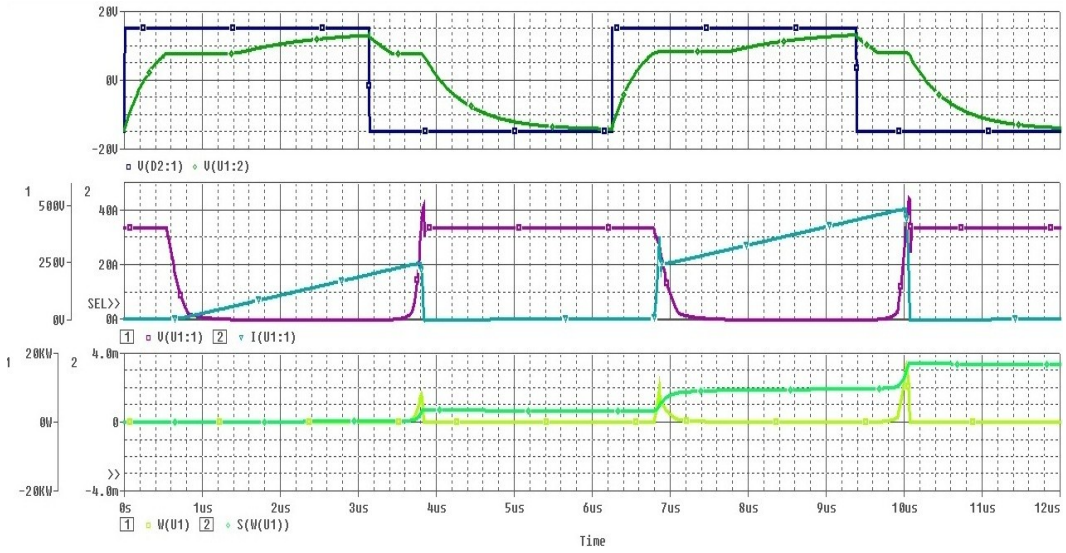

Fig. 22 - Simulation which shows the voltage signal input (in dark blue), the gate voltage (in dark green), the collector voltage (in purple), the collector current (in light blue), the power (in light green) and the energy dissipation (in green).

The values of energy dissipated during the switching transient evaluated in simulation correspondence of different gate resistance values are shown below.

Gate Resistances		**Energy Losses**	
R_G ON [Ω]	**R_G OFF [Ω]**	**E ON [µJ]**	**E OFF [µJ]**
33	100	536,96	640,34
47	100	763,01	644,36
68	100	1175	616,12
33	100	536,96	640,34
33	68	527,98	480,38
33	47	539,02	359,66

Tab. 4 - Energy dissipated changing the gate resistance ensuring $R_{G(OFF)} > R_{G(ON)}$.

The circuit simplicity and low cost are the strengths of this method.
On the other hand the impossibility to perform a dynamic control of the gradients of voltage and current and R_G as the only effective control parameter of these magnitudes make the margins of optimization very restricted. By adjusting the value of R_G action is taken at the same time and in equal measure on both gradients. Therefore only one of the two quantities can be set adjusted independently.

Another problem is to ensure that during switching there is a uniform current distribution between multiple devices connected to each other

because when the power involved is high these problems can cause malfunction or destruction of devices.
To solve these problems it is necessary to carry out the independent control of the gradients of voltage and current. This can be achieved only with feedback techniques.

3.2. Driving closed loop - Feedback Techniques

The following techniques, based on the feedback control of the output, allow to overcome the limits of the traditional method in order to optimize operation. These techniques allow you to control the waveform of current and voltage at the collector of each device, in order to be able to act in a targeted and independent on *di/dt* and *dv/dt* with the aim of finding a tradeoff between switching losses, EMI and stress due to overvoltage and overcurrent. [9, 13, 15, 20]

3.2.1. Independent control of *dv/dt* and *di/dt* through feedback on the gate voltage

In driving open loop, the switching speed is set appropriately dimensioning the gate resistance. This approach doesn't allow either a dynamic control or an independent control of the current and voltage profiles, hindering the optimization process.
Decouple control of *di/dt* from the *dv/dt* means giving the designer an additional degree of freedom in finding the best tradeoff between switching losses, EMI and stress on the device. Figure 23 shows a principle diagram of a driving system that realizes such decoupling. [17]

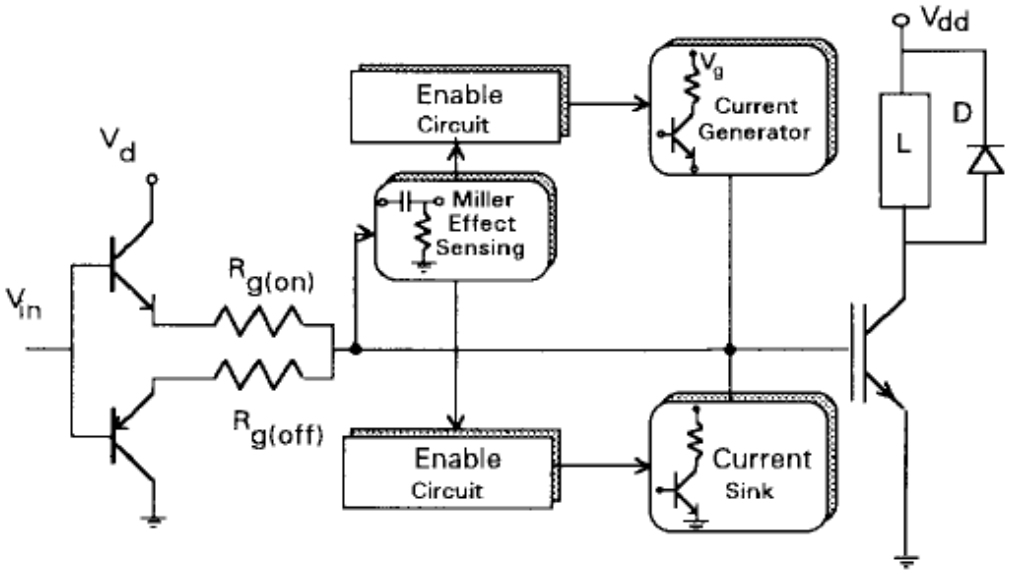

Fig. 23 - Basic diagram of a driving system optimized.

Starting from a basic open loop configuration, here is added a feedback loop on the gate voltage that allows to detect start and stop the source of the Miller zone on V_{GE} and activate at a current pulse generator to inject on the gate of the device an additional charge, for the entire duration of the Miller interval.

Turn ON

At Turn - ON a pulse from the sensing circuit on the gate terminal active temporarily, in the zone of Miller, a current pulse generator that injects an additional charge on the gate. Its duration is lower than the region of Miller. The sudden increase of the charge injected on the input capacitance due to a significant increase in the *dv/dt* leaving unaltered the *di/dt*, since, in the initial instant of the Miller region, the transient on the collector current has already ended. The additional charge also produces a significant reduction in the amplitude of the Miller zone as charging of the capacitance between gate and collector increases. For the method to be effective it isn't necessary to inject charge to the whole interval of Miller, but rather accurately synchronize the injection of the charge in the gate with the beginning of the Miller effect. In this way it is possible to speed

up the voltage transient leaving almost unaltered the current transient with a reduction up to 50% of the switching losses in the best case. With this technique it is possible to realize the decoupling control of the output.
In fact, to act on *di/dt* is possible to dimension the R_G increasing its value in order to contain the EMI caused by abrupt variations of current. If you have a slowdown at Turn-ON of the device it is possible to compensate for the decrease in the *di/dt* and the consequent increase of the losses by increasing the *dv/dt* independently.

Turn OFF

At Turn - OFF, a similar mechanism to that used for the Turn-ON allows to reduce the delay time of switch-OFF and accelerating the fall of the current leaving unaltered the voltage profile. An auxiliary circuit of discharge done near the area of Miller a route of low impedance that temporarily increases the amount of charge to the gate. It should however be noted that the dynamic control of *di/dt* affects only the initial region of the decreasing current, due to the section of the MOS device still active. The current tail in shutdown, due to the BJT section of the device, can't be modified in any way through an external circuit, but only by acting on the parameters of the device fabrication. Generally, the value of the gate resistance on the turn OFF is set so as to keep the device in its Reverse Bias Safe Operating Area (RBSOA). This involves two types of problems:

- Spurious switching in a bridge configurations;
- High delay time to turn OFF.

The *di/dt* is related with electromagnetic interference. To reduce EMI and recover the lost power, due to higher *dv/dt* in the area of Miller, it is necessary to size the gate resistance.
In this case, activating the current sink both in the region of Miller and in the stretch that precedes it, we would obtain a double benefit:

- Reducing the delay time to turn OFF;

- Reduction of losses through an increase in the *dv/dt* without affecting the current transient.

An idealized model simulations

With Pspice simulator has been verified the effectiveness of the method by testing it on an ideal circuit and compared the electrical quantities during switching obtained with both methods: open and closed loop.
Starting from a basic open loop configuration, here is added a feedback loop on the gate voltage that allows to detect start and stop the source of the Miller zone on V_{GE} and activate at a current pulse generator to inject on the gate of the device an additional charge, for the entire duration of the Miller interval.
Gate charge is the total amount of charge to turn ON a power device.

At Turn-ON, the increase of the amount of charge injected on the input capacitance due to a significant increase in *dv/dt* leaving unaltered the *di/dt*, since, at the instant of origin of the region of Miller, the transitional on the collector current has already sold out. During turn-OFF, a similar mechanism can reduce the delay time switch-OFF and accelerate the power fails while leaving the voltage profile. Here a "current sink" increases in the area of Miller the amount of charge removed from the gate capacitance of the IGBT.
It is known that any power device that works generates losses. Power device losses can be categorized into three elements: driving loss that is generated when driving the power device; switching loss that is generated when the device is turned ON or OFF; conduction loss that is generated while the device is turned ON. Driving loss can be calculated from gate charge. Switching loss can be calculated from gate resistance and device parasitic capacitances. Conduction loss can be calculated from ON-resistance. Since the device under test works at high frequencies (about

500 kHz) driving loss and switching loss are dominant. Power loss is then calculated as product of gate charge, gate voltage and frequency. [5]

$$P = f * I_G * V_{GE}$$

In figure 24 is represented the same circuit of Figure 21 to which is added an impulsive ideal current generator. This produces a rectangular pulse of current of appropriate amplitude synchronized with the instant of origin of the Miller region and duration equal to that interval of Miller.

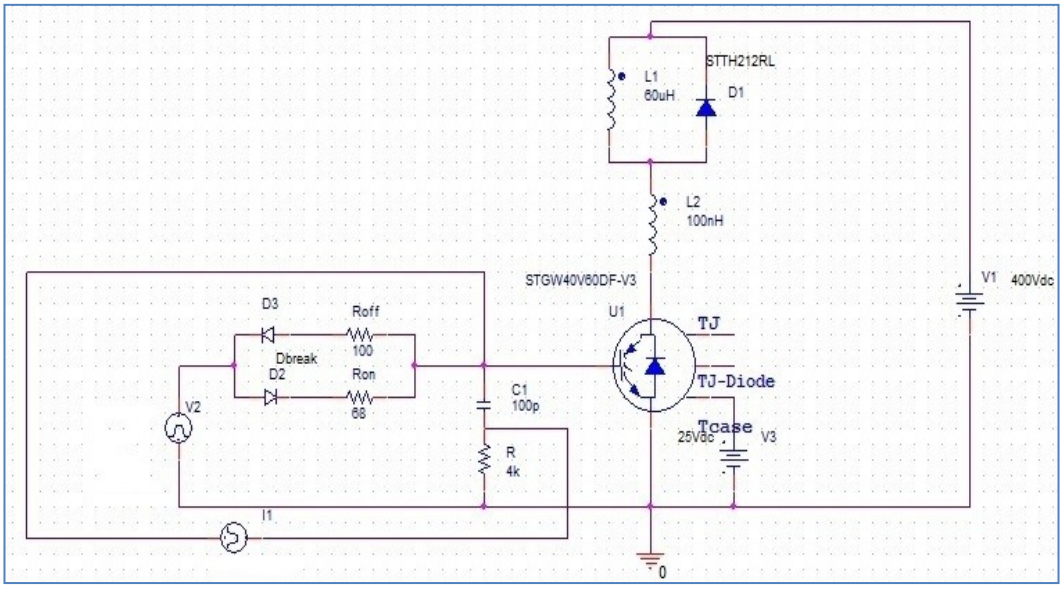

Fig. 24 - Driving circuit with feedback on the gate with $R_{G(ON)}$=68Ω and $R_{G(OFF)}$=100Ω.

Figures 25-26 show the performance of the voltage and current on the collector of the device for switching ON and OFF in relation to the impulse of additional current applied to the gate at the instant of the initial of the Miller zone.

The displayed sequence shows a Turn-ON followed by a Turn-OFF.

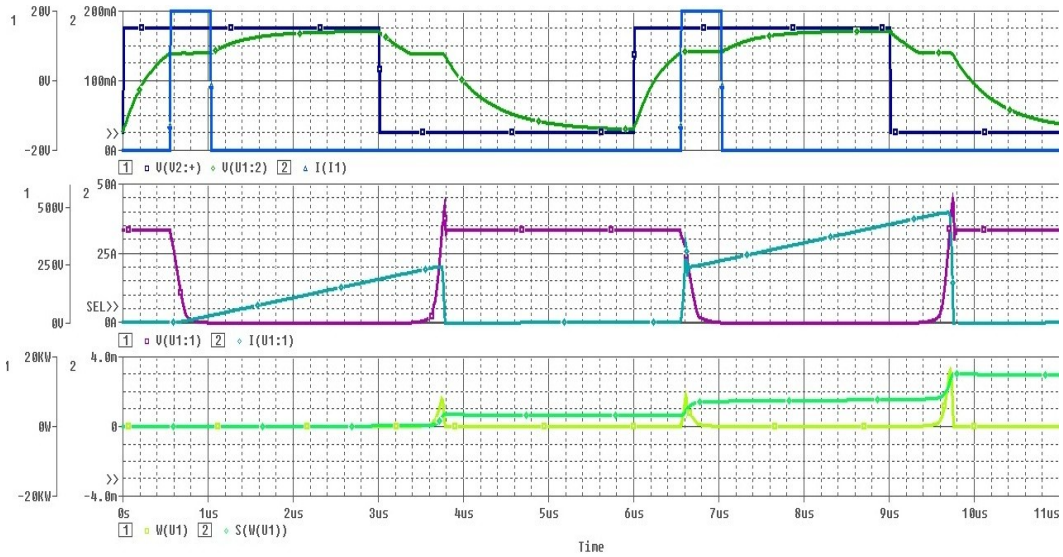

Fig. 25 - Simulation phase of Turn - ON which shows the voltage signal input (in dark blue), the gate voltage (in dark green), the current pulse (in blue), the collector voltage (in purple), the collector current (in light blue), the power (in light green) and the energy dissipation (in green).

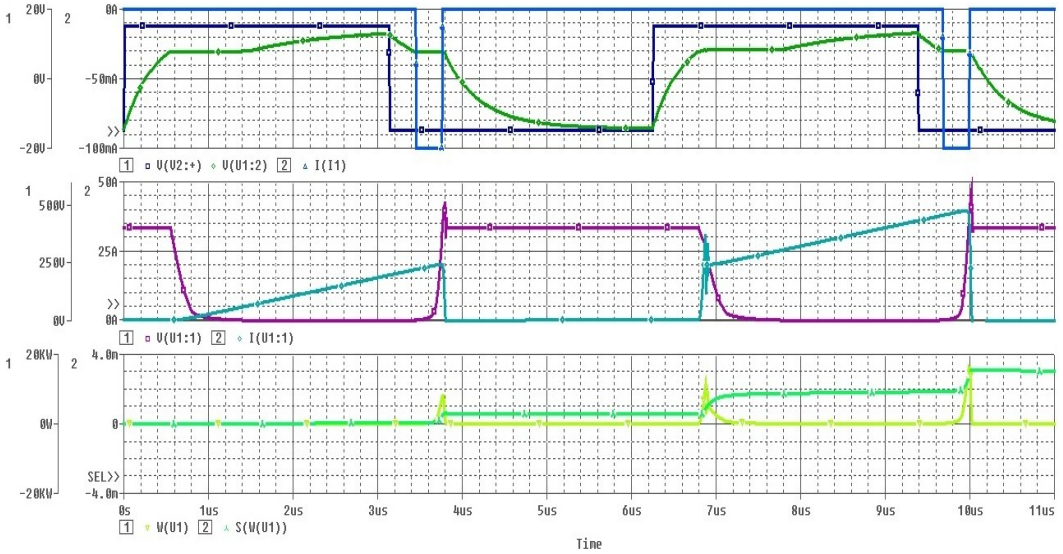

Fig. 26 - Simulation phase of Turn - OFF which shows the voltage signal input (in dark blue), the gate voltage (in dark green), the current pulse (in blue), the collector voltage (in purple), the collector current (in light blue), the power (in light green) and the energy dissipation (in green).

Figures 27-29 show the trend of the voltage and current on the collector of the device for turn ON in correspondence of different values of the gate resistor. Figures 28-30 show the trend of the power and energy lost for turn ON in correspondence of different values of the gate resistor, in the same condition.

Figures 27-28 show the waveforms by changing the $R_{G(ON)}$ for the value 33Ω, 47Ω and 68Ω while the $R_{G(OFF)}$ is constant to the value of 100Ω. It can be observed that the increase of the gate resistance $R_{G(ON)}$ causes a progressive reduction of *dv/dt* with small variations of the *di/dt*. The

advantage is the reduction of overcurrent, while the disadvantage consists in the increase of energy loss during switching.

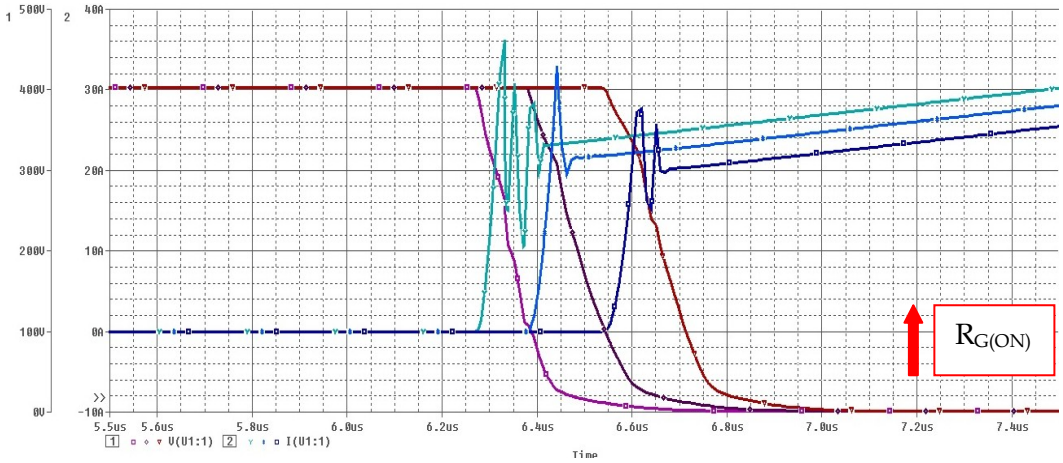

Fig. 27 - Simulation phase of Turn - ON which shows the collector voltage (in purple) and the collector current (in blue) changing the $R_{G(ON)}$.

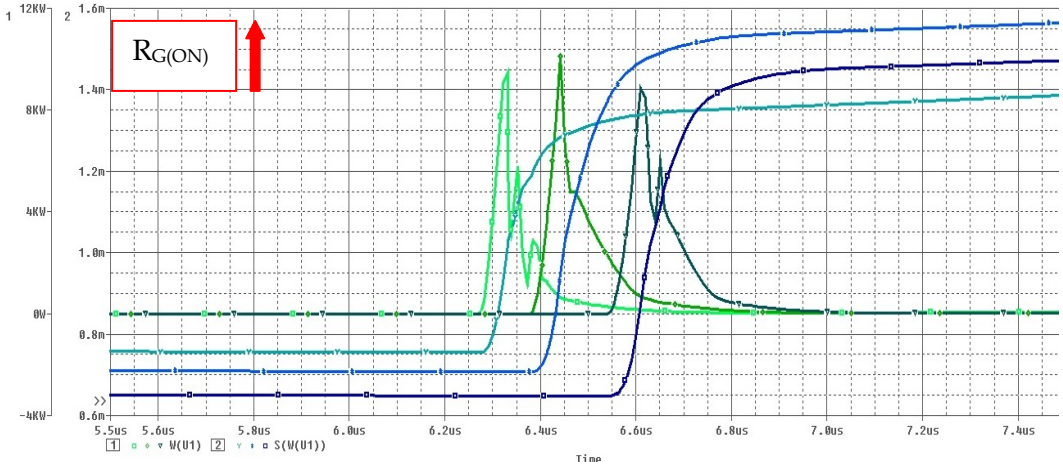

Fig. 28 - Simulation phase of Turn - ON which shows the power (in green) and the energy losses (in blue) changing the $R_{G(ON)}$.

Figures 29-30 show the waveforms by changing the $R_{G(OFF)}$ for the value 47Ω, 68Ω and 100Ω while the $R_{G(ON)}$ is constant to the value of 33Ω. It can be observed that increasing the gate resistance $R_{G(OFF)}$ a progressive reduction of *dv/dt* is caused with small increase of the *di/dt*. A drawback consists in the progressive increasing of energy losses during the commutation.

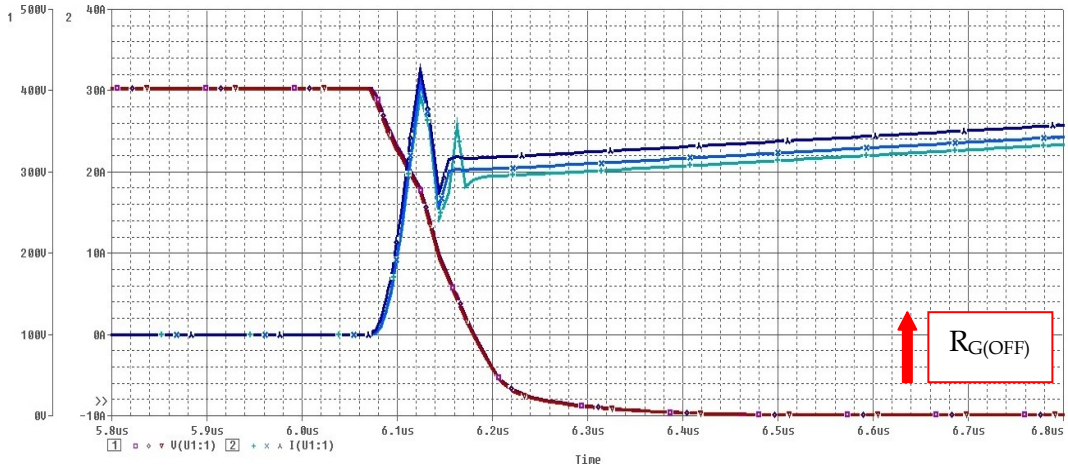

Fig. 29 - Simulation phase of Turn - ON which shows the collector voltage (in purple) and the collector current (in blue) changing the $R_{G(OFF)}$.

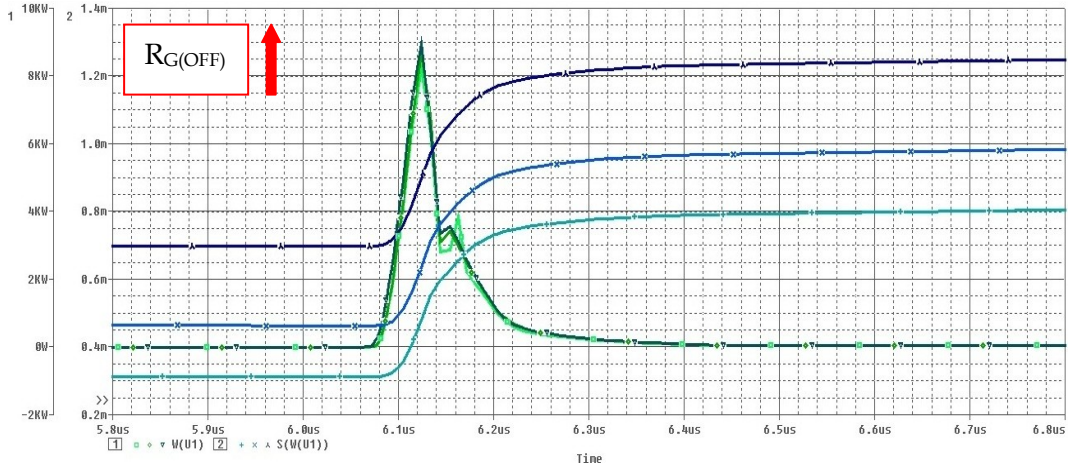

Fig. 30 - Simulation phase of Turn - ON which shows the power (in green) and the energy losses (in blue) changing the $R_{G(OFF)}$.

Figures 31-33 show the trend of the voltage and current on the collector of the device for turn OFF in correspondence of different values of the gate resistor. Figures 32-34 show the trend of the power and energy lost for turn OFF in correspondence of different values of the gate resistor, in the same condition.

Figures 31-32 show the waveforms by changing the $R_{G(ON)}$ for the value 33Ω, 47Ω and 68Ω while the $R_{G(OFF)}$ is constant to the value of 100Ω. It can be observed that the increase of the gate resistance $R_{G(ON)}$ cause an increase in the *dv/dt* and a reduction of the *di/dt*. This leads to a smaller region of Miller, then a quick shutdown of the device and a reduction of energy losses during Turn OFF.

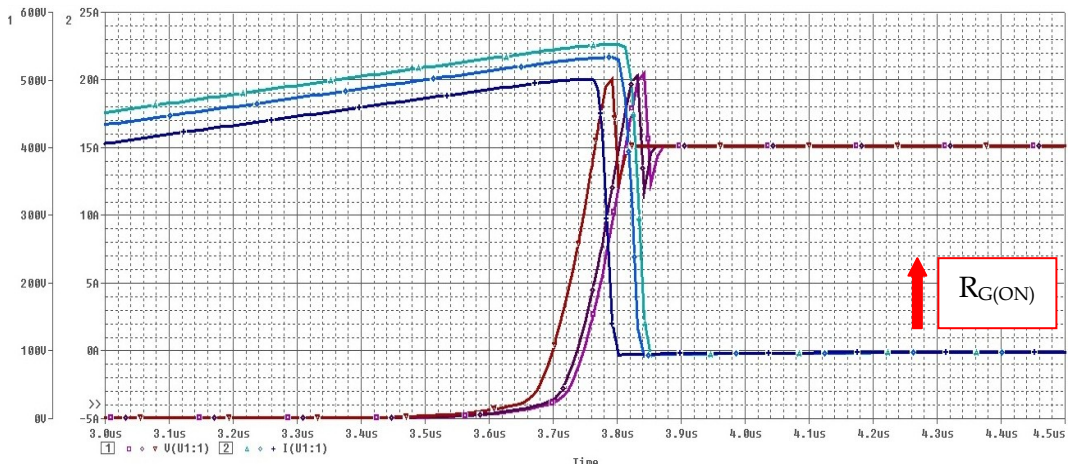

Fig. 31 - Simulation phase of Turn - OFF which shows the collector voltage (in purple) and the collector current (in blue) changing the $R_{G(ON)}$.

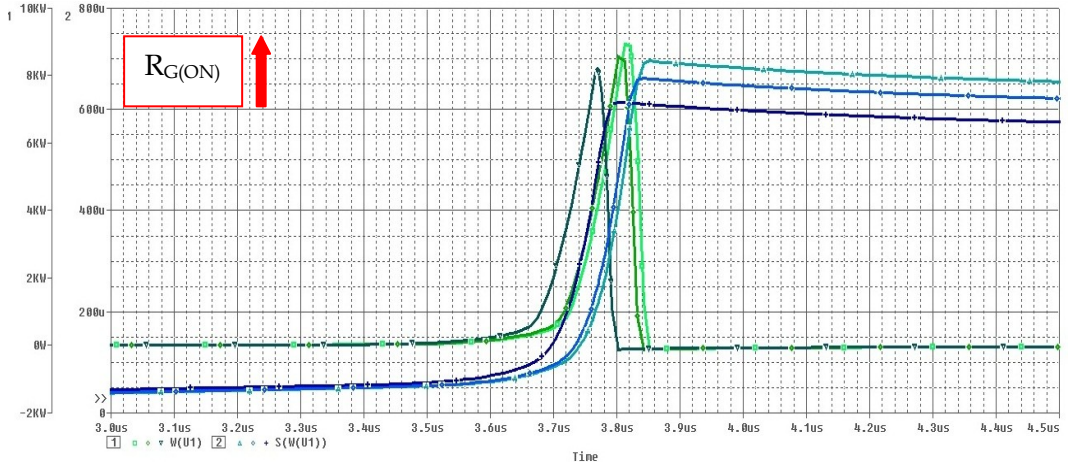

Fig. 32 - Simulation phase of Turn - OFF which shows the power (in green) and the energy losses (in blue) changing the $R_{G(ON)}$.

Figures 33-34 show the waveforms by changing the $R_{G(OFF)}$ for the value 47Ω, 68Ω and 100Ω while the $R_{G(ON)}$ is constant to the value of 33Ω. It can be observed that increasing the gate resistance $R_{G(OFF)}$ causes a progressive reduction of *dv/dt* and *di/dt*. A drawback consists in the progressive increase of energy loss during switching and the increase of overvoltages.

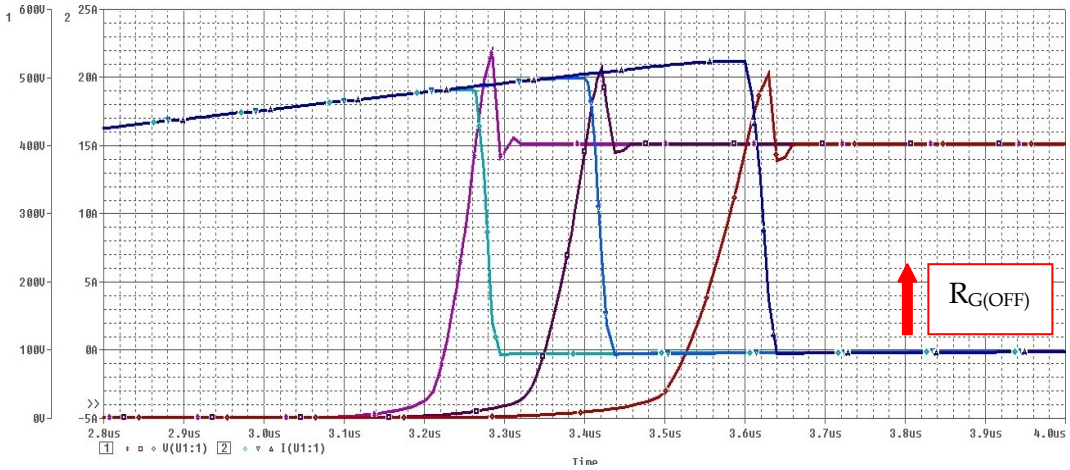

Fig. 33 - Simulation phase of Turn - OFF which shows the collector voltage (in purple) and the collector current (in blue) changing the $R_{G(OFF)}$.

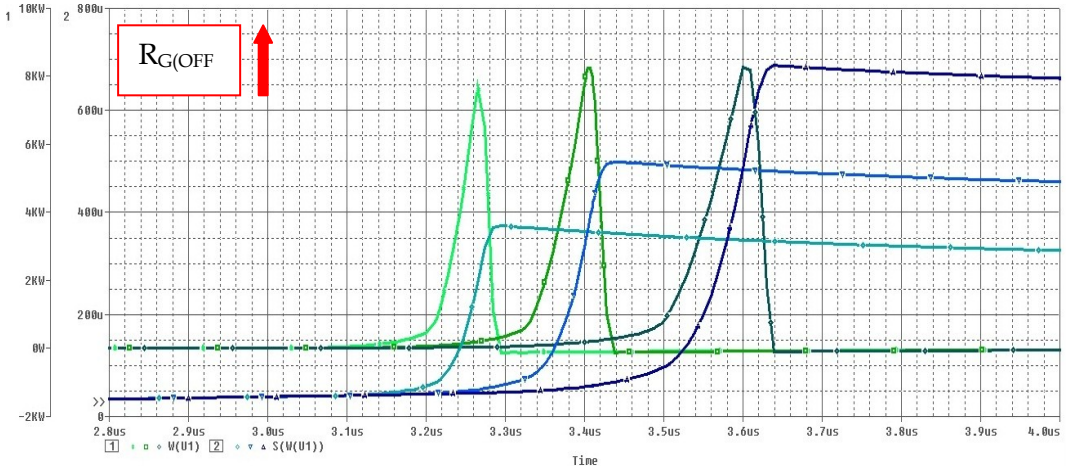

Fig. 34 - Simulation phase of Turn - OFF which shows the power (in green) and the energy losses (in blue) changing the $R_{G(OFF)}$.

The values of energy dissipated during the switching transients for different gate resistance values are shown below.

Gate Resistances		Energy Losses	
R_G ON [Ω]	**R_G OFF [Ω]**	**E ON [µJ]**	**E OFF [µJ]**
33	100	497,37	589,18
47	100	627,10	547,49
68	100	785,05	539,52
33	100	497,37	589,18
33	68	471,63	440,49
33	47	449,67	335,64

Tab. 5 - Energy dissipated changing the gate resistance ensuring $R_{G(OFF)}>R_{G(ON)}$.

In addition to the increase of overcurrents at Turn-ON and overvoltages at Turn-OFF a greater circuit complexity is added in comparison to open

loop method, associated with the presence of circuits of the detection zone of the Miller and a pulsed current generator.

3.2.2. Dynamic control of *dv/dt* with active clamping

This technique realizes an active control of the *dv/dt* through a feedback on the collector voltage in order to dynamically set a proper value. This technique allows also to limit overvoltage during shutdown.

A clamper is an electronic circuit that fixes either the positive or the negative peak excursions of a signal to a fixed value. The clamper doesn't restrict the peak-to-peak excursion of the signal, it moves the whole signal up or down so as to place the peaks at the reference level. A diode clamp circuit consists of a diode, which conducts electric current in only one direction and prevents the signal exceeding the reference value and a capacitor which provides a DC offset from the stored charge. The capacitor forms a time constant with the resistor load which determines the range of frequencies over which the clamper will be effective.

A clamping circuit will bind the upper or lower extreme of a waveform to a fixed DC voltage level. These circuits are also known as DC voltage restorers. Clampers can be constructed in both positive and negative polarities. When unbiased, clamping circuits will fix the voltage lower limit (or upper limit, in the case of negative clampers) to 0 Volts. These circuits clamp a peak of a waveform to a specific DC level compared with a capacitively coupled signal which swings about its average DC level.

Clamp circuits are categorised by their operation; negative or positive, and biased or unbiased. A positive clamp circuit outputs a purely positive waveform from an input signal; it offsets the input signal so that all of the waveform is greater than 0 V. A negative clamp is the opposite of this that outputs a purely negative waveform from an input signal.

A bias voltage between the diode and ground offsets the output voltage by that amount.

Shown below are the main clamp circuits used in applications.

Positive unbiased

In the negative cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak positive value of V_{IN}. During the positive cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage, so $V_{OUT} = 2V_{IN}$.

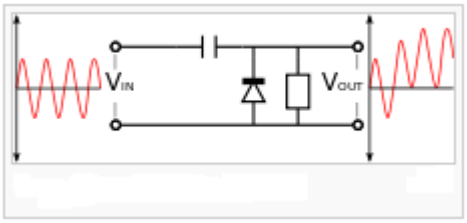

Fig. 35 - A positive unbiased clamp.

Negative unbiased

A negative unbiased clamp is the opposite of the equivalent positive clamp. In the positive cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak value of V_{IN}. During the negative cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage again, so $V_{OUT} = -2V_{IN}$.

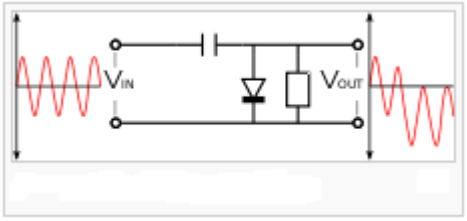

Fig. 36 - A negative unbiased clamp.

Positive biased

A positive biased voltage clamp is identical to an equivalent unbiased clamp but with the output voltage offset by the bias amount V_{BIAS}. Thus, $V_{OUT} = 2V_{IN} + V_{BIAS}$.

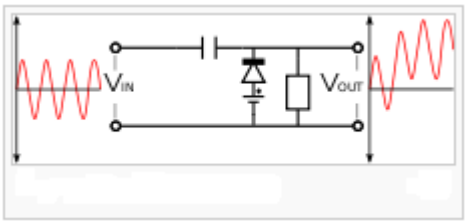

Fig. 37 - A positive biased clamp.

Negative biased

A negative biased voltage clamp is likewise identical to an equivalent unbiased clamp but with the output voltage offset in the negative direction by the bias amount V_{BIAS}. Thus, $V_{OUT} = -2V_{IN} - V_{BIAS}$.

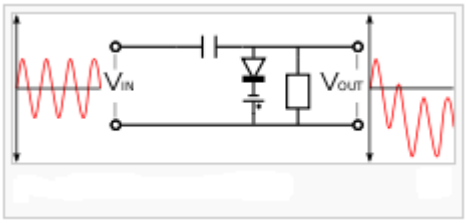

Fig. 38 - A negative biased clamp.

Operational - Amplifier circuit

The figure shows a clamp circuit with a non-zero reference clamping voltage realized using an operational - amplifier device. The advantage here is that the clamping level is at precisely the reference voltage. There is no need to take into account the forward voltage drop of the diode. The effect of the diode voltage drop on the circuit output will be reduced by the gain of the amplifier, resulting in an insignificant error. The circuit also has a great improvement in linearity at small input signals in comparison to the simple diode circuit.

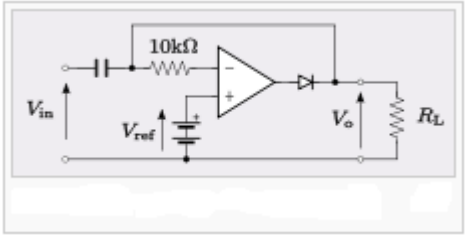

Fig. 39 - Op-amp clamp circuit.

Principles of operation

Clamping can be used to adapt an input signal to a device that cannot make use of or may be damaged by the signal range of the original input.

The schematic of a clamper includes a capacitor, followed by a diode in parallel with the load. The clamper circuit relies on a change in the capacitor's time constant; this is the result of the diode changing current path with the changing input voltage. The magnitude of R and C are chosen so that the time constant RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the diode's non-conducting interval. On the other hand the capacitor is chosen small enough to allow it to charge quickly during the diode's conducting interval.

During the first negative phase of the AC input voltage, the capacitor in the positive clamper charges rapidly. As V_{IN} becomes positive, the capacitor serves as a voltage doubler; since it has stored the equivalent of V_{IN} during the negative cycle, it provides nearly that voltage during the positive cycle; this essentially doubles the voltage seen by the load. As V_{IN} becomes negative, the capacitor acts as a battery of the same voltage of V_{IN}. The voltage source and the capacitor counteract each other, resulting in a net voltage of zero as seen by the load.

This technique therefore allows to ensure, at the same *dv/dt* at turn-OFF, a faster switching compared to the driving open loop where the *di/dt* would be higher.

3.2.3. Active control of the collector voltage by feedback with preconditioning Bias voltage

Also this technique is based on the introduction of a feedback between collector and gate of the device. The collector voltage is compared with a

reference signal through a low-gain operational amplifier. The figure 40 shows a diagram of the driving system.

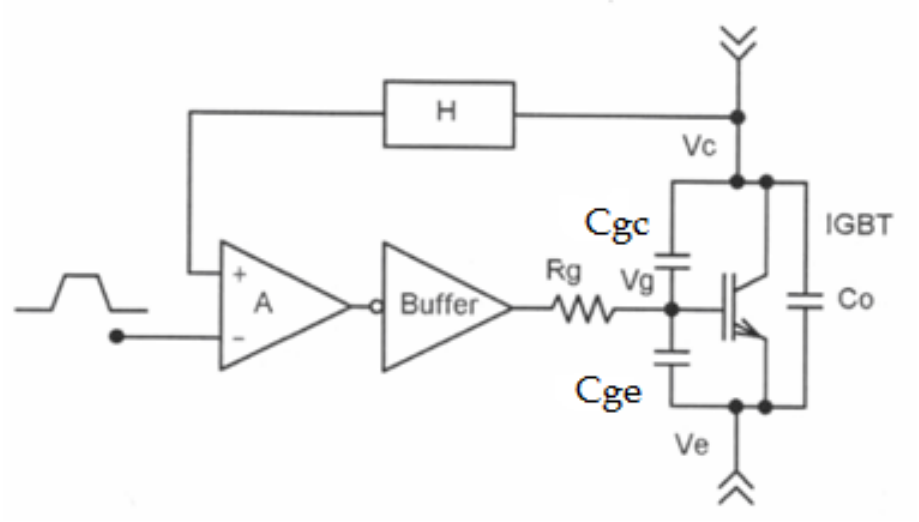

Fig. 40 - Principle diagram.

The H block in the feedback loop must ensure that the relationship of feedback and a bandwidth determined in the project. A current buffer is inserted to provide the IGBT gate all the necessary current. The gate resistance is used to ensure the stability of the circuit and its value is similar to that used in hardswitching. Using this circuit, during switching, the collector voltage of the IGBT follows the waveform profile given by the reference signal.

The parameters *Cgc*, *Cge* and *Co* represent the capacitive parasitic phenomena intrinsic to the device. The values of these capacities vary in function of the voltage V_{CE} and collector current. At turn ON, the value of *Cgc* is maximum and the intrinsic bandwidth of the device reduced to its minimum value; while to turn OFF the *Cgc* is minimal and its velocity with respect to the gate signal is maximum. During shutdown the value of *Cgc* is reduced in comparison to the condition of the system and the response speed of the device is increased. To achieve an accurate control is appropriate that the response speed of the device is high. The worst case occurs in the turn-OFF when the initial value of *Cgc* is maximum. To improve the performance of the control circuit the technique involves the

application of a small bias voltage, said preconditioning, before the beginning of turn-OFF.

The aim is to improve the response of the device by reducing the value of *Cgc*, strongly correlated to the V_{CE}.

CHAPTER 4 - A NOVEL TECHNIQUE

4.1. Independent control of *dv/dt* and *di/dt* through feedback on the gate voltage using a monostable circuit

In order to overcome the drawbacks of hardswitching driving, mainly the high switching losses and EMI, has pursued the goal of selecting a technique of driving advanced that proves appropriate in this case.

The technique of independent control of the *dv/dt* and *di/dt* through feedback on the gate voltage allows to reduce switching losses and the occurrence of EMI through an appropriate dimensioning of the gate resistance R_G and of an auxiliary generator in the area of Miller that charging the device at Turn ON and discharge it at Turn OFF.
Switching charge is the total charge in the period for which the collector voltage and the collector current are crossed. So the idea of this new method consists in detecting the Miller area using the shunts circuits (RC) and a monostable circuit coupled to two operational amplifiers, such as to allow the activation of a "sink", like the circuit totem pole, in such a way you can inject or subtract current during switching.

The proposed method realizes the decoupled control of *dv/dt* and *di/dt*, both turn ON and turn OFF.

4.1.1. Operating principle

With the simulator Pspice has been verified the effectiveness of the method by performing tests on the circuit under evaluation, both in power ON and OFF of the device.

Turn ON

The circuit devoted to the improvement of the turn-ON dynamic, shown in Fig. 41, is used to inject an additional charge into the gate. The aim is to accelerate the commutation of the device only acting on the *dv/dt*, leaving the profile of the current unchanged.

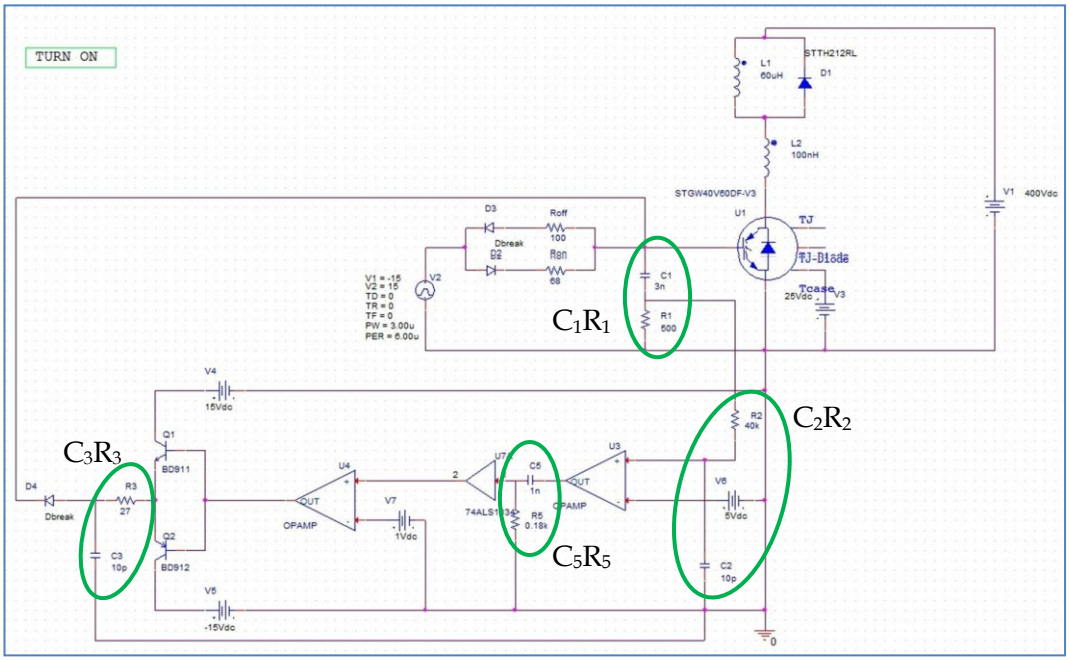

Fig. 41 - Driving circuit with feedback on the gate with $R_{G(ON)}$=68Ω and $R_{G(OFF)}$=100Ω at Turn - ON.

Since the current is stabilized to its steady state value of the 'ON' state in correspondence of the Miller zone, a special circuit (C_1R_1 + R_2C_2) receives the impulse voltage and current from the gate and synchronizes them with the start of the Miller region.

The comparator U_3 is used in inverting configuration. It is the circuit that amplifies the pulse from the RC shunt, turning it into a rectangular pulse of amplitude 5 V going to drive the next monostable circuit.

The C_5R_5 circuit receives the pulses of voltage and current and synchronizes them with the end of the Miller region.

The comparator U_4 amplifies the voltage pulse from the monostable up to 15 V such as to drive the current generator realized with two complementary BJTs connected in totem pole configuration.

The R_3C_3 circuit is placed at the output and sets the amplitude of the current pulse.

Figure 42 shows the voltage and current on the collector of the device for switching ON together with the impulse of the additional current injected into the gate at the instant of the initial of the Miller zone.

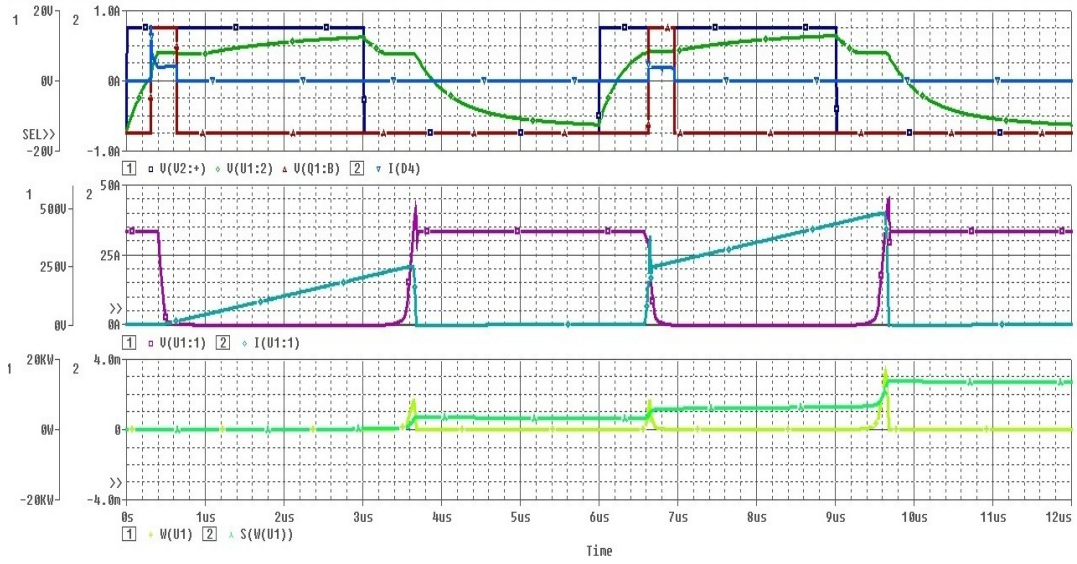

Fig. 42 - Simulation phase of Turn - ON which shows the voltage signal input (in dark blue), the gate voltage (in dark green), the current pulse (in blue), the voltage pulse that regulates the current (in dark red), the collector voltage (in purple), the collector current (in light blue), the power (in light green) and the energy dissipation (in green).

Minimizing power loss is essential to the overall design of an efficient power electronics circuit. As it was said in Chapter 3 switching losses depend on the value of the gate resistance. So in order to determine the losses have made different simulations by changing the value of the gate resistance.

Figures 43 and 45 show the waveform of collector voltage and current changing the value of R_G. Figures 44 and 46 show the waveform of power and energy losses at the same condition.

Therefore, figures 43 and 44 show the waveforms by changing the $R_{G(ON)}$ for the value 33Ω, 47Ω and 68Ω while the $R_{G(OFF)}$ is constant to the value of 100Ω. It can be observed that increasing the value of the gate resistance $R_{G(ON)}$ a progressive reduction of *dv/dt* and *di/dt* is caused. The

disadvantage consists in the increase of overcurrent and energy losses during switching.

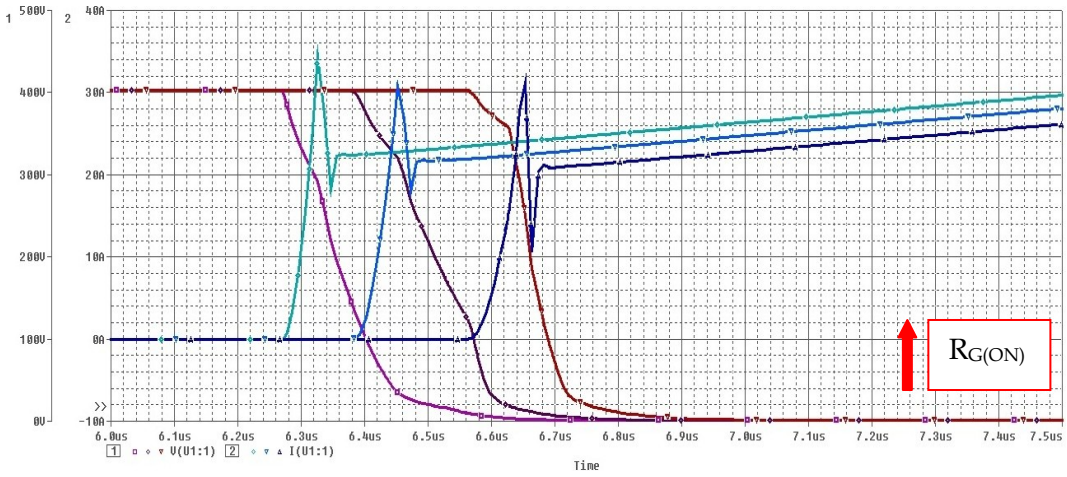

Fig. 43 - Simulation phase of Turn - ON which shows the collector voltage (in purple) and the collector current (in blue) changing the $R_{G(ON)}$.

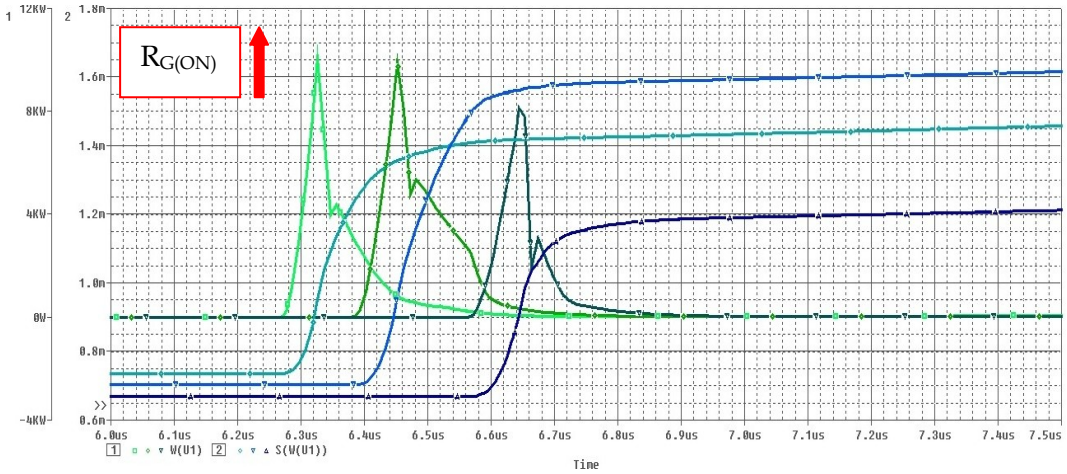

Fig. 44 - Simulation phase of Turn - ON which shows the power (in green) and the energy losses (in blue) changing the $R_{G(ON)}$.

Figures 45 and 46 show the waveforms by changing the $R_{G(OFF)}$ for the value 47Ω, 68Ω and 100Ω while the $R_{G(ON)}$ is constant to the value of 33Ω. It can be observed that the increase of the gate resistance $R_{G(OFF)}$ causes a reduction of *dv/dt* and *di/dt*, of overcurrent and losses during the commutation.

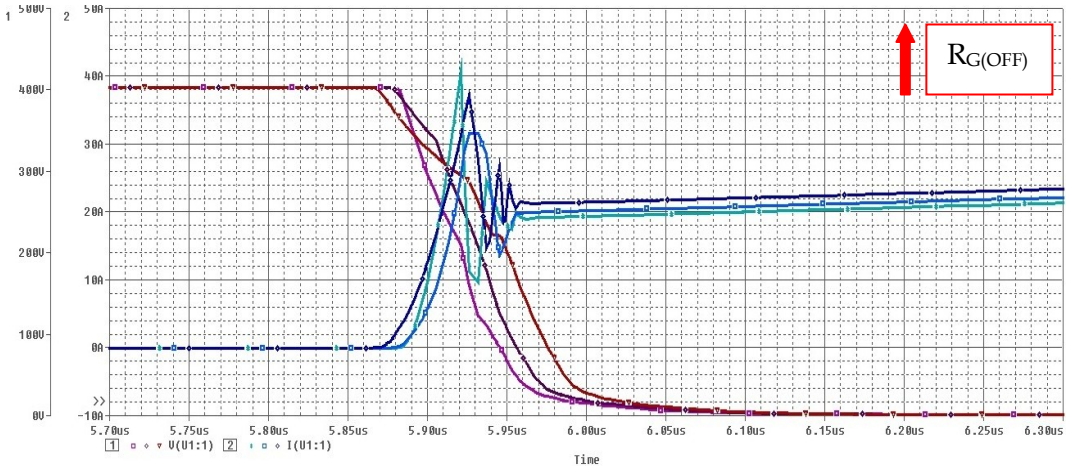

Fig. 45 - Simulation phase of Turn - ON which shows the collector voltage (in purple) and the collector current (in blue) changing the $R_{G(OFF)}$.

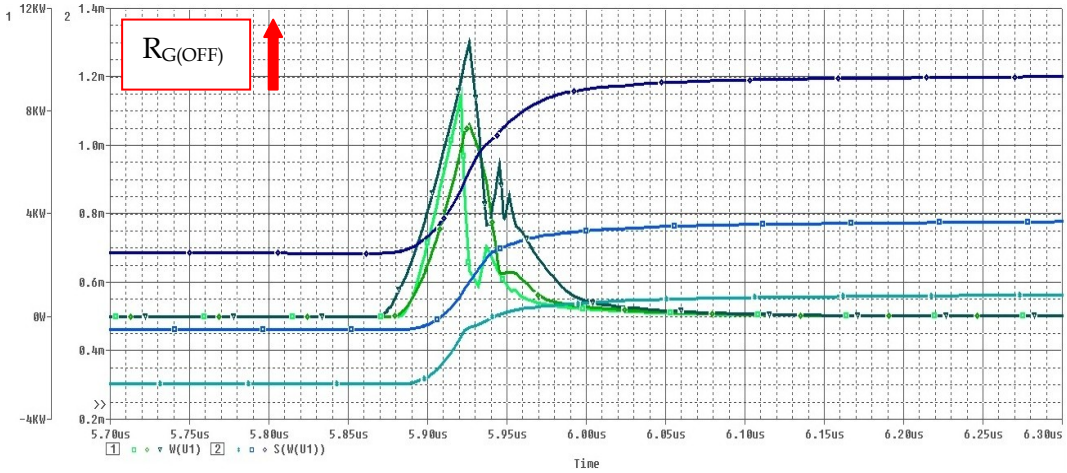

Fig. 46 - Simulation phase of Turn - ON which shows the power (in green) and the energy losses (in blue) changing the $R_{G(OFF)}$.

Turn OFF

The circuit used for Turn OFF the device is similar that of Turn ON with the only difference of using the two operational amplifiers U_3 and U_4 in no inverting configuration and diode D_4 inversely polarized. This allows to extract the current from the gate while still decoupling of *dv/dt* and *di/dt*.

Figure 47 shows the corresponding circuit at turn OFF.

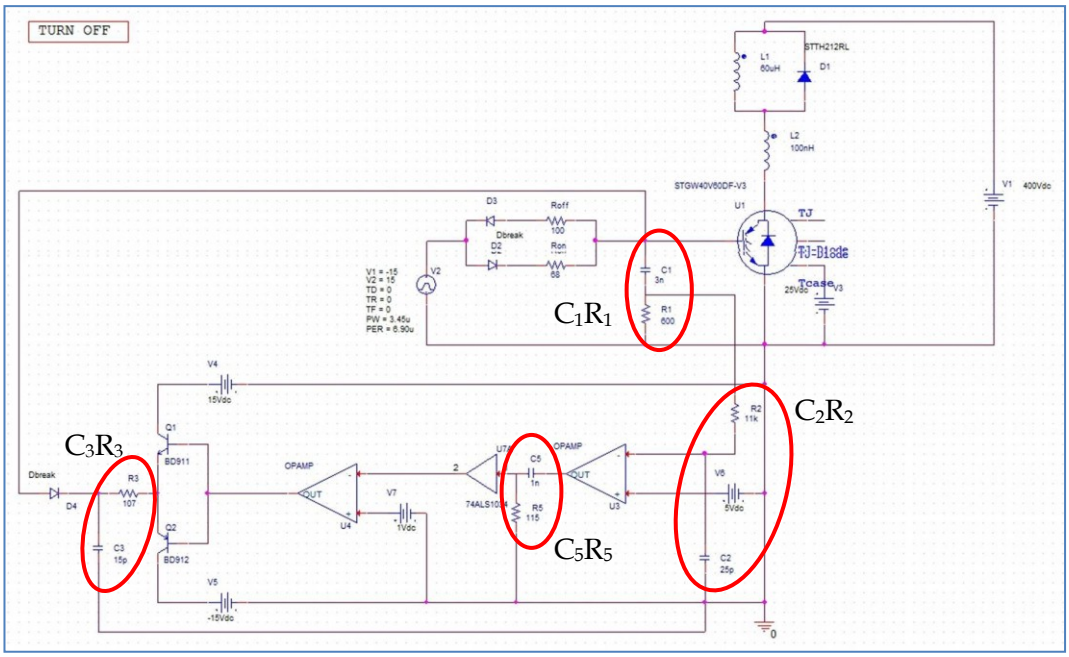

Fig. 47 - Driving circuit with feedback on the gate with $R_{G(ON)}$=68Ω e $R_{G(OFF)}$=100Ω at Turn - OFF.

Figure 48 shows the collector voltage and current of the device for switching OFF together with the quantity of charge subtracted from the gate at the instant of the initial of the Miller zone.

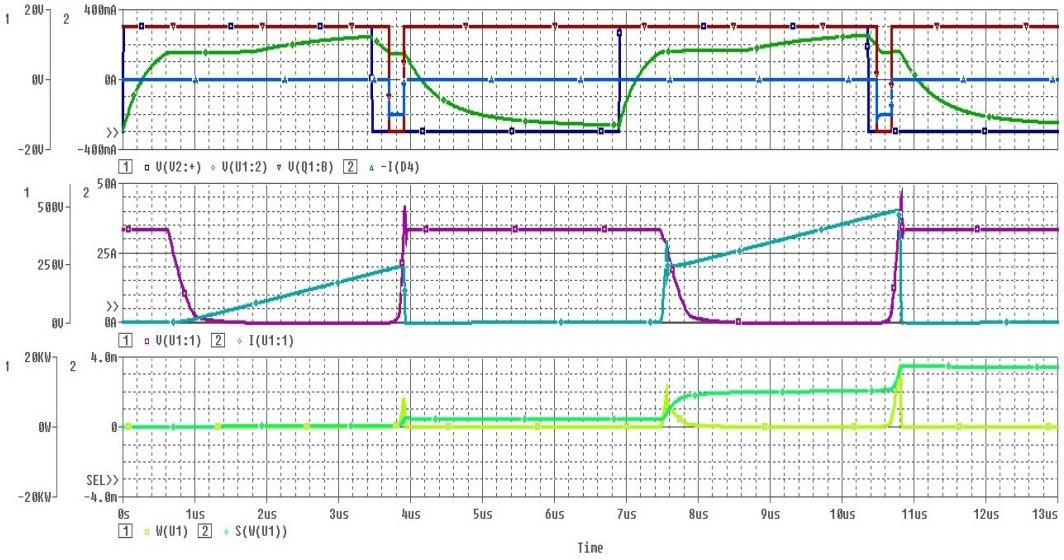

Fig. 48 - Simulation phase of Turn - OFF which shows the voltage signal input (in dark blue), the gate voltage (in dark green), the current pulse (in blue), the voltage pulse that regulates the current (in dark red), the collector voltage (in purple), the collector current (in light blue), power (in light green) and the energy dissipation (in green).

As said for switching losses at turn ON is also true at turn OFF. So simulations were made changing the value of R_G so as to be able to determine the losses of the device during switching.

Figures 49 and 51 show waveform of collector voltage and current changing the value of R_G. Figures 50 and 52 show the waveform of power and energy losses at the same condition.

Therefore, figures 49 and 50 show the waveforms by changing the $R_{G(ON)}$ for the value 33Ω, 47Ω and 68Ω while the $R_{G(OFF)}$ is constant to the value of 100Ω. It can be observed that increasing the gate resistance $R_{G(ON)}$ an increase of *dv/dt* and a reduction of *di/dt* is caused. This means a smaller region of Miller, then a quick shutdown of the device and the increase in overvoltages and losses.

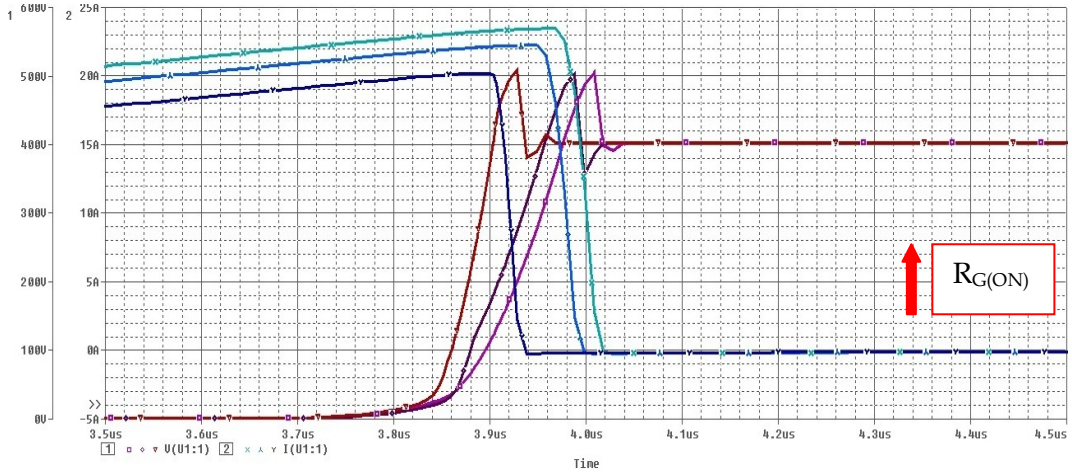

Fig. 49 - Simulation phase of Turn - OFF which shows the collector voltage (in purple) and the collector current (in blue) changing the $R_{G(ON)}$.

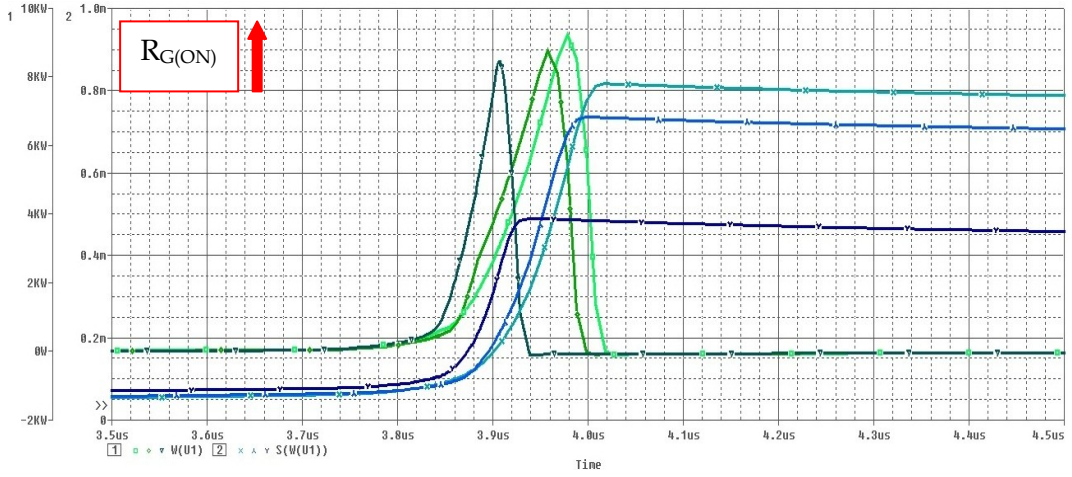

Fig. 50 - Simulation phase of Turn - OFF which shows the power (in green) and the energy losses (in blue) changing the $R_{G(ON)}$.

Figures 51 and 52 show the waveforms by changing the $R_{G(OFF)}$ for the value 47Ω, 68Ω and 100Ω while the $R_{G(ON)}$ is constant to the value of 33Ω. It can be observed that the increase of the gate resistance $R_{G(OFF)}$ causes a

reduction of *dv/dt* and *di/dt*. The drawback consists in the progressive increase of energy losses during switching.

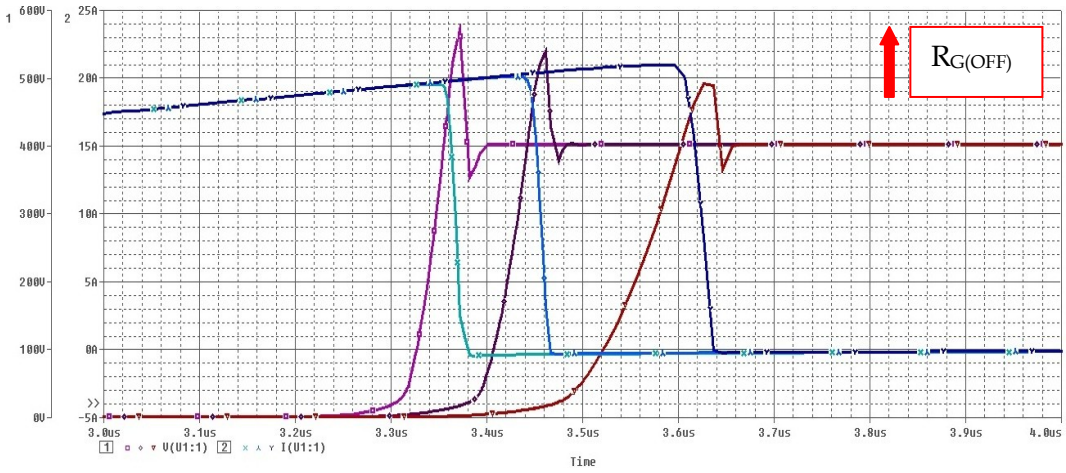

Fig. 51 - Simulation phase of Turn - OFF which shows the collector voltage (in purple) and the collector current (in blue) changing the $R_{G(OFF)}$.

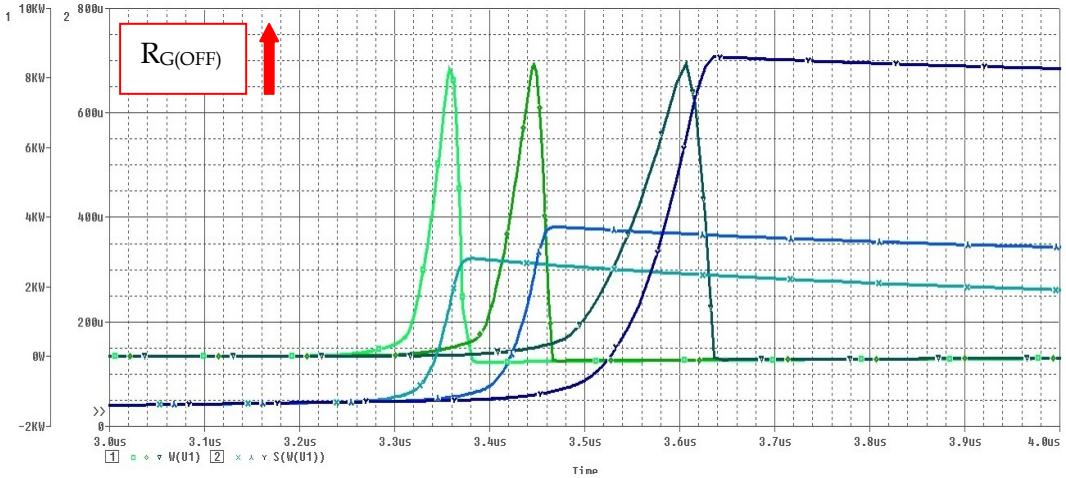

Fig. 52 - Simulation phase of Turn - OFF which shows the power (in green) and the energy losses (in blue) changing the $R_{G(OFF)}$.

Performance of the device

A more accurate and independent control of *dv/dt* and *di/dt* has been developed to significantly improve the performance of the device under test in terms of reduction of the switching losses, limitation of EMI and overvoltages on the collector, potentially destructive.

The values of energy dissipated during the switching transients for different value of gate resistances are shown below.

Gate Resistances		Energy Losses	
R_G ON [Ω]	R_G OFF [Ω]	E ON [μJ]	E OFF [μJ]
33	100	397,04	377,87
47	100	423,04	397,79
68	100	507,92	397,82
33	100	397,04	377,87
33	68	293,66	323,67
33	47	348,36	275,64

Tab. 6 - Energy dissipated changing the gate resistance ensuring $R_{G(OFF)}>R_{G(ON)}$.

In addition to overcurrents at Turn-ON and overvoltages at Turn-OFF a greater circuit complexity is added than the previous method, associated with the presence of circuits of the detection zone of Miller and a monostable circuit, but it has the advantage of having reduced losses.

4.2. Comparison between the driving techniques

The traditional approach of hardswitching has been then overcome with the introduction of techniques based on the active control of the dynamics of turning ON and OFF exploiting feedback signals.

In fact, in open loop driver circuits, the current used to charge the gate capacitance of the IGBTs is limited by selecting a suitable value of the gate resistance. Using such an approach, the dynamic control of the commutation can not be achieved as well as the independent control of current and voltage profiles. In order to optimize the device commutation it is necessary to decouple the control of the *di/dt* and *dv/dt*, aiming to get the best compromise among commutation losses, EMI and stress on the device.

Basically, starting from an open loop driver, a feedback control of the gate voltage is considered. The idea consists in detecting the beginning of the Miller zone using a derivative circuit in turn-ON and turn-OFF, then, a current generator is activated injecting a supplementary charge into the gate until the Miller zone is over.

During the turn-ON, because the current transient is completely extinguished as soon as the device enters in the Miller zone, the abrupt increasing of the charges injected into the input gate capacitance causes a significant increasing of the *dv/dt*, without changing the *di/dt*. During the turn-OFF, if the reduction of the delay time is of primary of concern, the optimization technique consists by connecting, in parallel to the principal driver circuit, an auxiliary path able to increase the amount of charge subtracted from the input capacitance of the device.

Such a method can be realized detecting the slope variations of the V_{GE} by mean of a simple derivative circuit (RC) and, then, activating a "current sink", for example a totem pole circuit, in order to extract charges from the gate capacitance just before the transient of the voltage, when the V_{GE} is in the Miller zone. A large reduction of the IGBTs delay time is obtained at the turn-OFF, in addition, switching-ON the same circuit as soon as the Miller zone is over, it is possible to shape the current profile increasing its slope.

Finally, a more accurate independent control of *dv/dt* and *di/dt* has significantly improve of the performance of the device under test in terms of reduction of the switching losses, limitation of EMI and overvoltages on the collector, potentially destructive.

In this thesis, a new approach for IGBTs turn-OFF optimization is suggested to get two main goals: overvoltage control together with commutation losses reduction. Both targets can be reached choosing an appropriate value of the turn-OFF gate resistance ($R_{G(OFF)}$) in combination with an auxiliary driver circuit. At the turn-ON, using the gate-emitter voltage only, a feedback control is realized to reduce the commutation losses, while for the turn-OFF the collector-emitter voltage has been used to control in a "closed loop" scheme the overvoltages on the device. Then, selecting an appropriate value of R_G resistance than in the case of

"hardswitching" commutations, such a strategy allows to obtain two main goals: overvoltage control and commutation losses reduction.

In figure 53, 54, 55 and 56 the graphs representing the switching losses versus different values of the gate resistances are show: the blue waveform represents the energy loss in the driving circuit in Hardswitching, the red waveform the feedback loop by means of the generator ideal current and the green waveform that is related to the third method by the use of a monostable circuit.

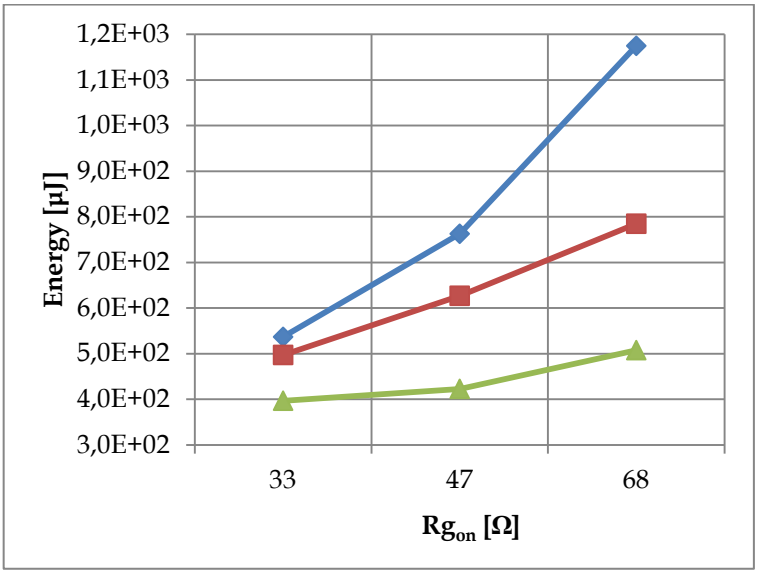

Fig. 53 - Switching losses at Turn - ON with RgOFF=100Ω.

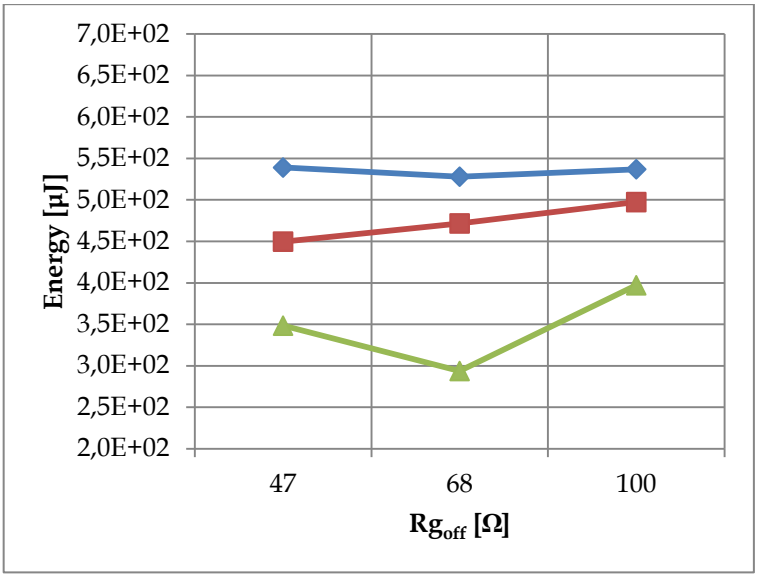

Fig. 54 - Switching losses at Turn - ON with RgON=33Ω.

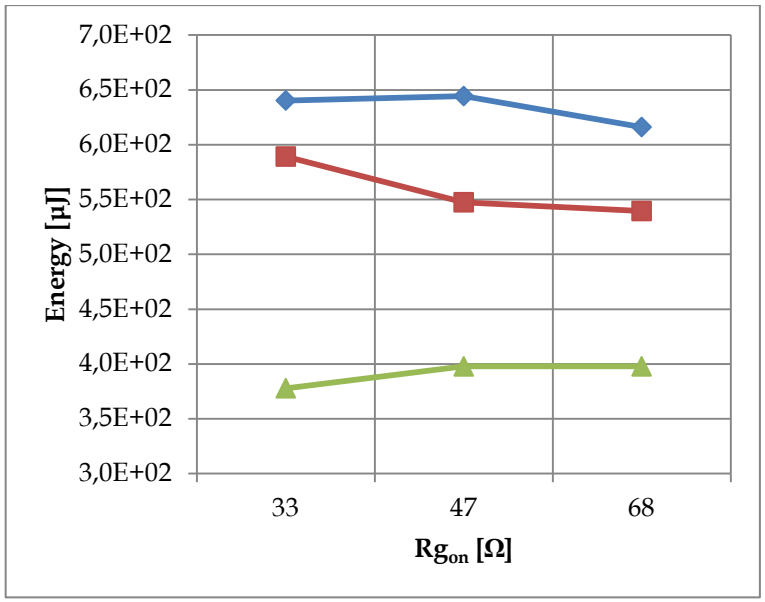

Fig. 55 - Switching losses at Turn - OFF with RgOFF=100Ω .

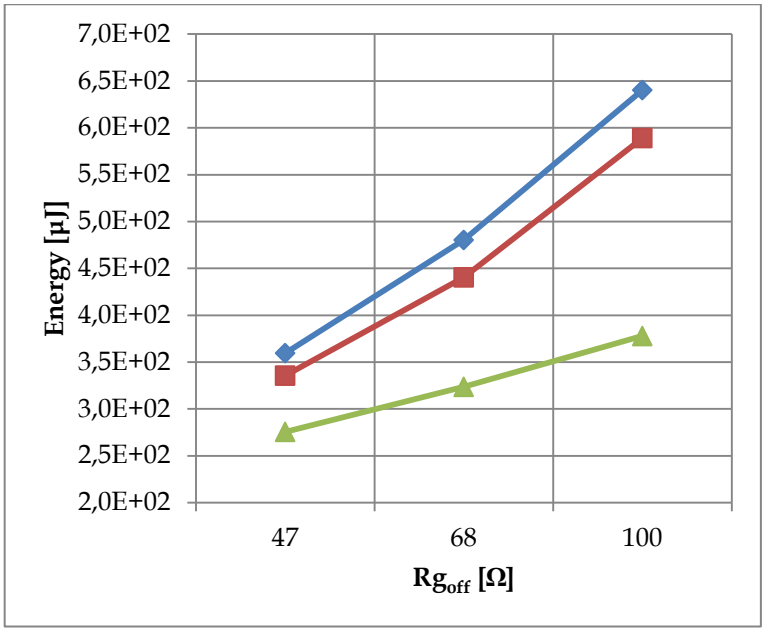

Fig. 56 - Switching losses at Turn - OFF with RgON=33Ω.

The solution adopted is a good tradeoff between conflicting requirements as the switching speed, energy losses, EMI, overvoltages and overcurrents. So the proposed method arises as a synthesis of the best features of the techniques described before. In fact the use of shunts circuits and a monostable circuit allows to obtain a reduction of energy losses of 40% at Turn ON and of 35% at Turn OFF.

CONCLUSIONS

In modern power converters, the optimal driving of each device is a critical design issue because a good tradeoff must be found among different constraints such as switching losses, electromagnetic interference generated by gradients of current, overvoltage and overcurrent related to parasitic phenomena. These phenomena are connected to non ideal behavior of real devices and stray circuit parameters. Steep profiles of current lead to large ElectroMagnetic Interference (EMI) and overvoltages, while rapid variations of the voltage can produce phenomena of "latch-up" in single IGBT or unwanted commutations. On the other hand, slow commutations are characterized by low values of *dv/dt* and *di/dt*, causing excessive losses in those power application during commutations.

The traditional approach in hardswitching has been overcome by the feedback methods on the gate. In fact, as seen above, these methods allow independent control of *dv/dt* and *di/dt* with the consequent reduction of energy losses during switching. Therefore, the solutions adopted are the result of tradeoff between often conflicting requirements, and depend on the characteristics of the used IGBT, the type of application and the target assumed on the design phase.

In conclusion, a novel technique that arises as a synthesis of the best features of the cases dealt with above has been proposed.
The proposed technique allows a reduction of energy losses of 40% at Turn ON and of 35% at Turn OFF.

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