
UNIVERSITA' DEGLI STUDI DI CATANIA

Dottorato di Ricerca Internazionale in Ingegneria dei Sistemi,
Energetica, Informatica e delle Telecomunicazioni
XXXI ciclo

**ALESSANDRO PARISI**

# Compact architectures for dc-dc converters with galvanic isolation

Ph.D. Thesis

**Coordinatore:**
Prof. P. ARENA

**Tutor:**
Prof. G. PALMISANO

**Co-tutor:**
Prof. E. RAGONESE

**Anno Accademico 2017/2018**

# SUMMARY

This thesis summarizes the main activities that I have been carried out during three years of Ph.D. studies at the RF-ADC, a joint research group between University of Catania and STMicroelectronics Catania.

Recently, galvanic isolation for both power supply and data communication is becoming mandatory in several application fields to guarantee safety and reliability, especially in harsh operative environments. A wide range of applications adopts galvanic isolation, e.g., sensor interfaces, serial link transceivers, low-power medical devices, and housekeeping power, such as gate-drivers or controllers for power converters. State-of-the-art isolators that manage both power and data transmission mainly adopt magnetic coupling by means of post-processed micro-transformers or fully integrated on-chip transformers. The galvanic isolation issue and the state-of-the-art of semiconductor isolators are presented in Chapter 1 along with the technology platforms adopted for this work, especially concerning

the implementation of galvanic isolation. It is worth noting that power and data functionalities of the proposed systems do not depend on the technology platform used for the isolation components, which can be manufactured either in post-processing technology or exploiting the SOI BCD process provided by STMicroelectronics. Therefore, this work does not address the design of the isolation transformer, but it is mainly focused on the architecture and the design of a galvanically isolated system for power and data transfer with the aim of reducing complexity and hence cost while preserving performance. Clearly, the technology platform greatly affects both efficiency and power density of the overall application.

By referring to the main limitations of the state-of-the-art solutions, this work presents three novel architectures, which implement galvanically isolated dc-dc converters with different target of applications. The main object of the proposed systems is the reduction of the number of isolated links while preserving both power and data functionalities. Chapter 2 will be focus on the design of a 100-mW galvanically isolated dc-dc converter with bidirectional data communication. The converter delivers regulated output power by means of a dedicated power link, while a second isolated channel is shared by control feedback loop and data transmission. The output voltage ranging from 2.4 V to 3.3 V and the variable output power make the proposed system very suitable for a wide range of applications. Chapter 3 will deal with a 100-mW dc-dc converter with galvanic isolation which is mainly addressed towards gate driver applications. It takes advantage of a customized architecture, which uses the isolated power link to feedback the control signal. The third isolated system will be presented in Chapter 4 and it has been designed to meet the requirements of sensor applications. The architecture is

made up of only one isolation component since power transfer, data communication and control feedback loop are implemented on the same isolated link.

Chapters 2-4 validate the functionalities and performance of the proposed systems with measurements and/or simulations, which are reported at the end of each chapter. Specifically, the dc-dc converter in Chapter 2 has been integrated and measured, so the experimental results are showed in detail. As regarding the systems in chapters 3 and 4, only simulations are provided since the exploited isolation component is under manufacturing and hence is not available for measurements. However, the active core of these systems has been integrated (see micrograph in Appendix B) and the experimental characterization will be performed as soon as possible. Finally, all the proposed architectures have been patented thus showing the industrial interest towards this Ph.D. research activity.

Besides the main topic, during my Ph.D. studies I was involved in the design of fully standard CMOS voltage references with micro- and nano-current consumption for ultra-low-power applications. Specifically, two voltage reference circuits have been designed to meet the requirements of RF-powered systems. The circuit description and measurements of these references are reported in [1] and [2].

# Content

# List of Tables

# List of Figures

# Nomenclature

| ACRONYM | DESCRIPTION |
|---|---|
| ADC | Analog-to-digital converter |
| AGC | Automatic gain control |
| ASK | Amplitude shift keying |
| BER | Bit error rate |
| CAN | Controller Area Network |
| CMT | Common-mode transient |
| CMTI | Common-mode transient immunity |
| CSA | Canadian Standards Association |
| CTR | Current transfer ratio |
| DC | Duty cycle |
| DEMUX | Demultiplexer |
| EA | Error amplifier |

| ACRONYM | DESCRIPTION |
|---|---|
| EM | Electromagnetic |
| EMI | Electromagnetic immunity |
| EN | European Norms |
| HS | High speed |
| HS DET | High speed detector |
| IEC | International Electrotechnical Commission |
| LDMOS | Lateral-diffused MOS |
| LED | Light emitting diode |
| LPF | Low-pass filter |
| LS | Low speed |
| LS DET | Low speed detector |
| MCU | Micro-controller unit |
| Multiplexer | MUX |
| NPG | Negative pulse generator |
| PFD/CP | Phase-frequency detector/charge pump |
| PLL | Phase-locked loop |
| PPG | Positive pulse generator |
| PWM | Pulse width modulated |
| PWM-CTR | Power control circuit |
| PVT | Process, voltage and temperature |
| rms | Root mean square |
| RF | Radio frequency |
| RF-ADC | Radio Frequency Advanced Design Center |
| RX | Receiver |
| SC | Switched capacitor |
| S/ENC | Sampler/encoder |
| SEM | Scanning electron microscope |
| SiO2 | Silicon dioxide |

| ACRONYM | DESCRIPTION |
|---|---|
| SiP | System in Package |
| SOI BCD | Silicon on Insulator Bipolar-CMOS-DMOS technology |
| TX | Transmitter |
| UL | Underwriters Laboratories |
| UPS | Uninterruptible power supply |
| VCO | Voltage-controlled oscillator |
| VDE | Verband Deutscher Elektringenieure |
| VHF | Very High Frequency |

# Chapter 1.

# Galvanic isolation: definition, requisites and applications

## 1.1. Introduction

This chapter introduces galvanic isolation issue and main isolation standards to be fulfilled in electronic devices, while illustrating how isolation can be implemented from a technological point of view and the applications which require isolation. Moreover, state-of-the-art solutions for both power and data transfer with galvanic isolation are reported for completeness and comparison purpose. Finally, an overview about the adopted galvanic isolation technology platforms is provided.

Galvanic isolation is used to separate electrically two domains while allowing at the same time an exchange of energy and/or information between them. It eliminates any direct path connections, thus preventing unwanted dc and ac current flows in both directions. A general block diagram of a galvanically isolated system is depicted in Fig. 1.1. Two domains, A and B, are isolated since one of them is subject to hazardous voltages and/or requires a different ground reference. Data signals are transferred across the galvanic isolation barrier to enable bidirectional communication between the two domains, while an isolated power supply for domain B is provided from domain A by a power transfer technique. For low-power applications, isolated power levels between 100 mW and 1 W with data rate up to 100 Mbit/s are typically required.

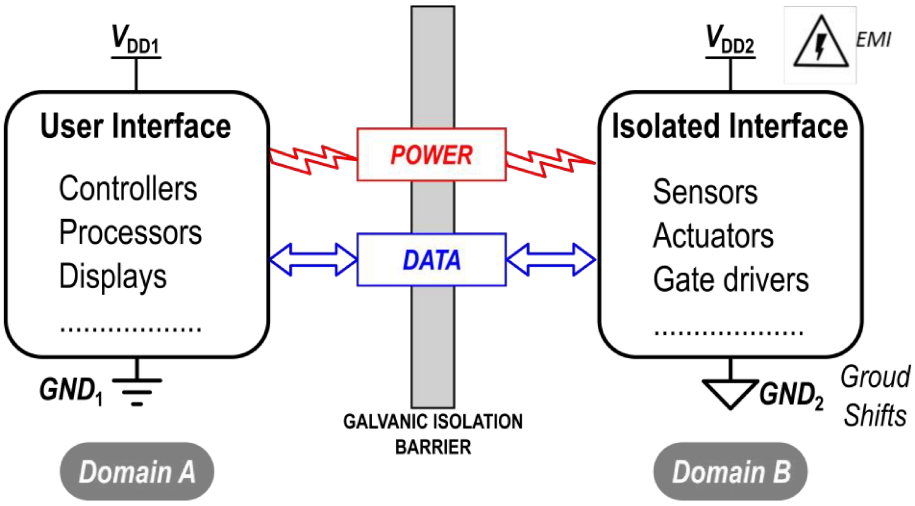



Fig. 1.1. Simplified block-diagram of a galvanically isolated system.

Galvanic isolation is mandatory when high power equipment is operated by human beings or to guarantee better reliability in harsh industrial

environments. Galvanic isolation is also required for relatively low power levels e.g., sensor interfaces, serial link transceivers, low-power medical devices, and housekeeping power, such as gate-drivers or controllers for power converters. Fig. 1.2 summarizes the most application fields where galvanic isolation is adopted.

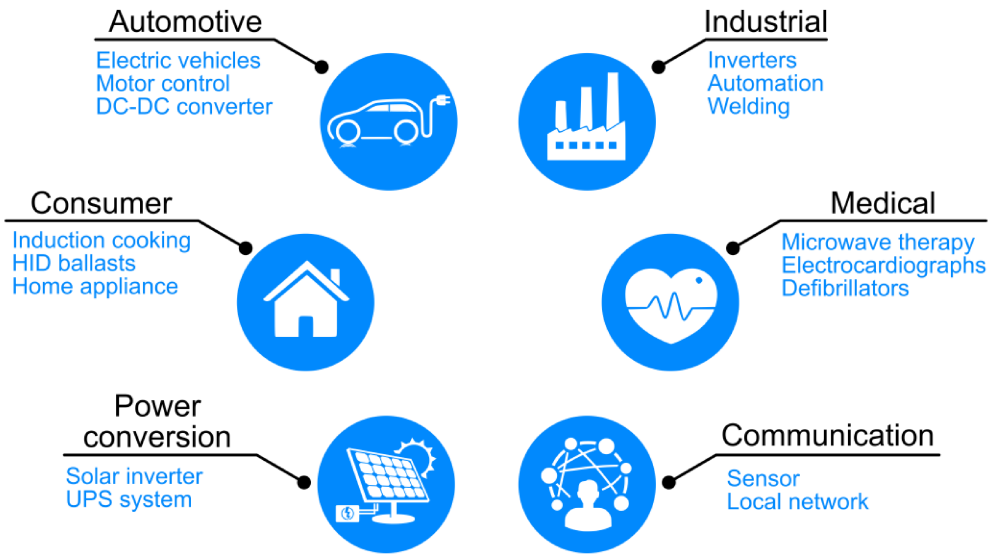



Fig. 1.2. Galvanic isolation application fields.

The research towards galvanic isolators has gained a lot of interest during the last decade due to the wide range of applications which need isolation either for proper operation or to meet the safety standards requirements. Several efforts have been made to increase the level of isolation while maintaining good efficiency performance. Nowadays, the research interests are addressed to the implementation of galvanic isolation by means of electromagnetic coupling, either using capacitive or inductive transfer

techniques, thus replacing traditional optocoupler and discrete transformers which are expensive and bulky.

This chapter is organized as follows. Section 1.2 deals with the safety reasons of galvanic isolation while the application fields are briefly described in Section 1.3. The isolation techniques and the state-of-the-art isolators are reviewed in Section 1.4. Finally, the main outcomes of this work are summarized in Section 1.5.

## 1.2. Safety isolation requirements

The most important motivations for providing galvanic isolation concern human safety in high voltage/current domains. Both in industrial and consumer environment, the employment of high power circuits is growing up thus leading towards several design challenges to meet safety requirements against electrical shock. Specifically, the currents, which are produced within the electronic appliances, can flow into the human body if no proper isolation is implemented, thus involving physiological effects such as involuntary movement, ventricular fibrillation or, ultimately, death [3]. Fig. 1.3 shows the range of current (expressed in rms value) which provides each effect [4]. The figure refers to a sinusoidal current source whose frequency is set at the value of 60 Hz. The electrical stimulus is applied by means of a copper cable which is held in the hands by a human being from 1 to 3 seconds. The weight of the human is about 70 kg. It can be notice that the minimum value of current that produces a slight warmth sensation is about 0.5 mA, while a current higher than 6 mA leads to the inability to *let go* (i.e., detach voluntarily from the

current source). Even higher currents determine burns, injuries and death, especially coupling them with extra-high voltages.

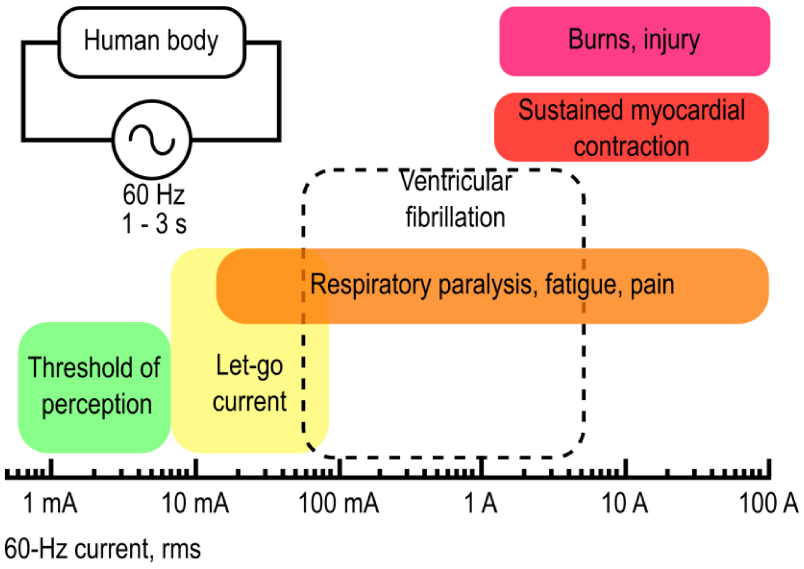



Fig. 1.3. Physiological effects of electricity.

The harms due to electrical shock have driven the definition of design standards and certification processes which establish the requirements for insuring human safety. Over time, national and international standards were developed. Some examples of commonly used system standards are reported in Table 1.1. System-level national regulations are defined by regional bodies, such as VDE, UL, and CSA, for Germany, United States, and Canada, respectively. Whereas international agencies such as the IEC and the EN, define the international standards. However, certification requirements can vary across the different regions of the world even when the same safety standards are referenced [5], though national and international bodies are

working to simplify the certification process, reducing the complexity caused by the high number of standards.

TABLE 1.1
SYSTEM-LEVEL STANDARDS INVOLVING ISOLATION BY MARKET AND REGION [5].

| | **Household** | **Industrial** | **Information technology** | **Measurement and control** | **Medical** |
|---|---|---|---|---|---|
| **International** | IEC 60065 | IEC 60204 | IEC 60950 | IEC 61010-1 | IEC 60601 |
| **Germany** | VDE 860 | | EN 60950 | VDE 410/ 0411 | VDE 0750 |
| **USA** | UL 60065 | UL 508, UL 60947 | UL 60950 | UL61010 | UL 60601 |
| **Canada** | | CSA. 14-10 | CSA 60950 | CSA 61010 | CSA 601 |

The main purpose of these standards is the definition of isolation degree in an electrical system. Commonly, the isolation levels are classified into four categories, i.e. functional, basic, double and reinforced [6]-[8], as shown in Fig. 1.4. The functional isolation consists of a simple separation of ground references which guarantees the proper operation of the system but does not provide protection against electrical shock. When safety is concerned, a galvanic barrier withstanding several kilovolts is adopted to electrically separate the user interface from the isolated interface. By using only one galvanic barrier a basic isolation is achieved. However, for a higher level of safety, a double isolation is required, which is implemented with two isolation barriers connected in series. Double isolation inherently improves the overall galvanic isolation and provides redundancy in case one of the two barriers fails. Finally, the reinforced isolation provides the highest level of isolation

available in commercial products and consists of a single isolation barrier which performs the equivalent isolation of the double level.

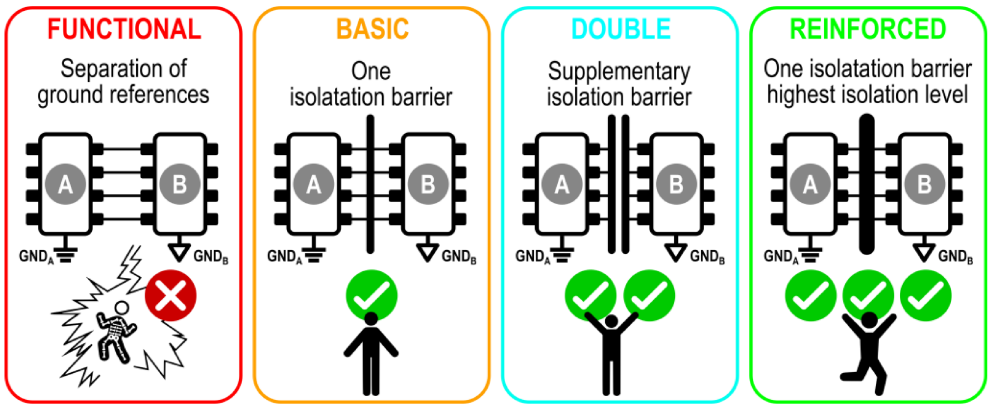



Fig. 1.4. Isolation levels and main additional features.

For a given application, system designers must choose the insulation characteristics of each component to meet system-level standards. The insulation specifications of a single device are defined by additional component-level standards which certify the safety requirements of the component, without guaranteeing the isolation level of the overall system. Commonly adopted component-level standards are:

- IEC 60747: Semiconductor Devices—Part 1: General
- UL 1577: Standard for Optical Isolators
- VDE 0884-10: Semiconductor Devices—Magnetic and Capacitive Coupler for Safe Isolation.

These standards provide the definition of several parameters and testing methodologies which are used to classify the isolation characteristic of the component. Specifically, the IEC 60747 and UL 1577 standards refer to the isolation specifications and testing parameters of optocoupler devices, while the VDE 0884-10 standard features the isolation requirements for highly integrated transformer-based and capacitive isolators.

The main parameters which quantify the high-voltage isolation performance and reliability of an isolator are the maximum transient isolation voltage, $V_{IOTM}$, the maximum repetitive voltage, $V_{IORM}$, and the maximum surge isolation voltage, $V_{IOSM}$. They are defined by the standards IEC 60747-5-5 and VDE 0884-10 and represent the isolator's capability to handle high-voltage stresses of different magnitude and transient profile without damage. $V_{IOTM}$ is defined as the peak transient voltage that the isolator can handle without breaking down for very short periods of time, while $V_{IORM}$ is the maximum repetitive peak voltage that the isolator can withstand over a specific long time. Finally, $V_{IOSM}$ quantifies the ability of the isolator to withstand very high voltage impulses of a certain transient profile. Both $V_{IOTM}$ and $V_{IORM}$ are measured together by means of two testing methodologies [9], Method A and Method B1, which are described by the VDE 0884-10 standard. The Method A is used during certification and its test profile is shown in Fig. 1.5. The isolator is stressed at $V_{ini}=V_{IOTM}$ for a $t_{ini}$ as long as 60 seconds. A following partial discharge test is carried out at a $V_m$ of 1.6 times $V_{IORM}$ for a $t_m$ of 10 seconds. On the other hand, the Method B1 is used during production manufacturing. Every device must pass this test before being released to the market. As shown in Fig. 1.6, during the process, the isolator is stressed at $V_{IOTM}$ for only one second, with a following partial

discharge test at 1.875 times $V_{IORM}$ for one more second. Differently from Method B1, the Method A is a destructive test since high values of $t_{ini}$ and $t_m$ are used which compromise safety level of devices. On the other hand, the values of $t_{ini}$ and $t_m$ in the Method B1 are chosen to do not deteriorate the isolation capability of devices.

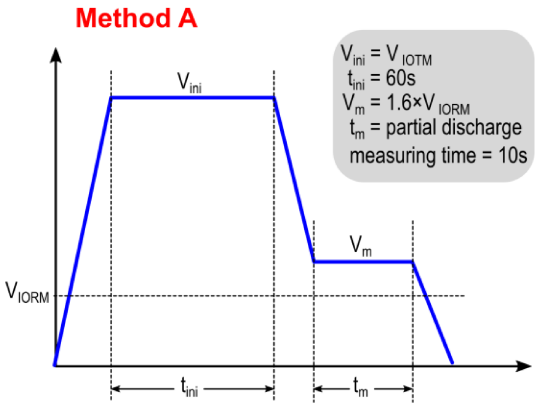



Fig. 1.5. Simplified Method A test profile.

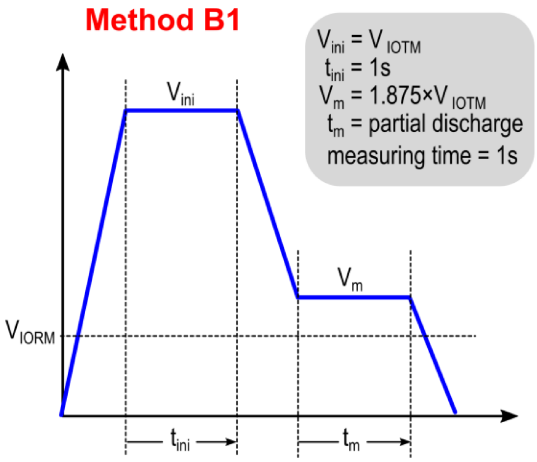



Fig. 1.6. Simplified Method B1 test profile.

Fig. 1.7 depicts the surge test profile which is adopted to claim a certain $V_{IOSM}$.

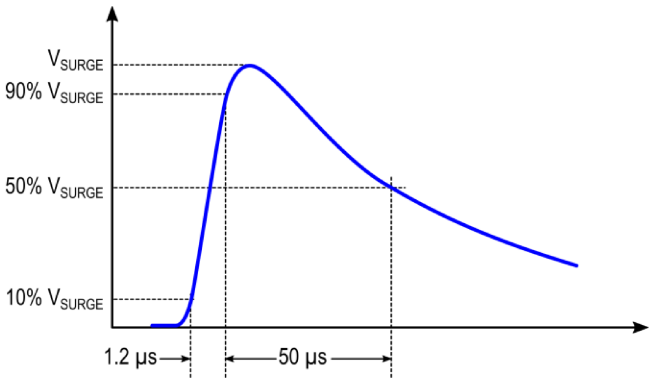



Fig. 1.7. Simplified surge test profile.

The surge test assesses the isolation level of an isolator. The basic isolation is achieved if the isolator passes the surge test at a peak voltage of 1.3 times $V_{IOSM}$, while the reinforced isolation is certified if the isolator passes the surge test with a $V_{SURGE}$ greater than 10 kV.

It is also worth noting that isolation requires specifications on the clearance (i.e. distance through air) and creepage (i.e. distance along the surface) of the isolator's package [6], as defined in Fig. 1.8, and its fabrication materials.

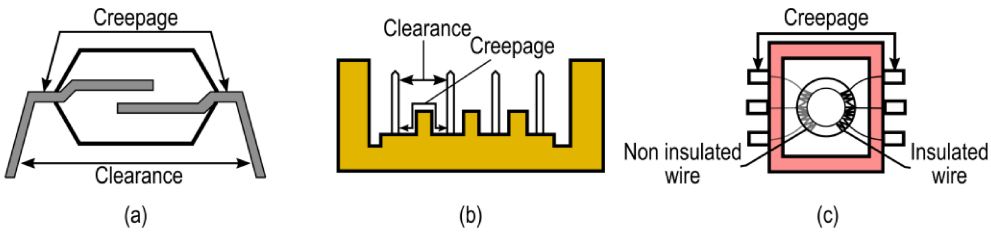



Fig. 1.8. Definition of clearance and creepage [3]: (a) optoisolator, (b) connector, (c) transformer.

## 1.3. Applications

The isolation is crucial for signal integrity, system protection, and user safety, thus becoming mandatory in the wide field of applications involving digital control and measurement. This section focuses on the main low power applications of galvanic isolators which are: wireline networks, current monitoring and gate driver systems.

### 1.3.1. Wireline networks

The most widespread applications of wireline networks are industrial process control, automotive, power supply regulation and point-to-point communications between computers [10]. Typically, data communication is supported by various types of physical networks, such as RS-232, RS-485, and the CAN. The main drawbacks of these networks are signal distortion and data loss due to the ground potential difference which can be established between the nodes of the networks. For instance, in RS-485 networks [11] the distances between the interconnected systems can reach up to 4000 meters thus leading to different ground references for each node. Fig. 1.9(a) shows a common situation in wireline networks. A ground loop exists between two devices (A and B) that are interconnected to exchange power and/or information. There are multiple ground paths which act as a large loop antenna and can induce currents into the system by picking up noise from the environment [12]. Moreover, ground shifts can occur in B (or A) thus causing overvoltage in A (or B) and consequently damage to the system. These problems are avoided by means of an isolator which breaks the ground loop, as shown in Fig. 1.9(b).

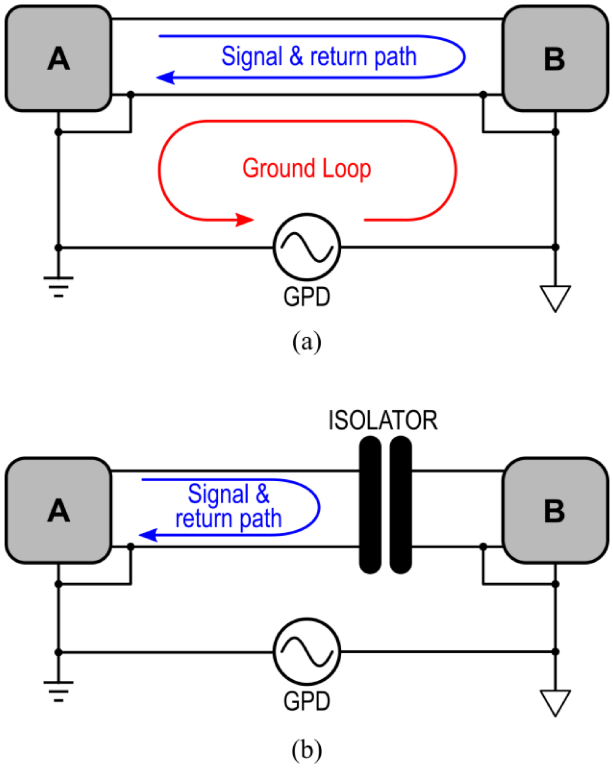



Fig. 1.9. Ground loops problem in wireline communication systems. Without (a) and with (b) a galvanic isolator.

The common supply voltage of low-power wireline transceivers for RS-232, RS-485 and CAN bus networks ranges from 3.3 to 5 V along with a current consumption up to tens milliamps [13]-[15]. Therefore, an isolated power supply providing around few tens of milliwatts of output power, working with supply voltages from 3.3 to 5 V is highly desirable to simplify wireline network's design.

### 1.3.2. Current monitoring

The measurement of current flow is required in a wide range of applications, such as hybrid electrical vehicles, electrical vehicles [16] and

power line monitoring. In such systems galvanic isolation is mandatory to provide safety both in automotive and domestic environments.

Fig. 1.10 shows the simplified architecture of a current monitoring system [17] which is based on a resistor $R_{shunt}$ of few hundreds micro-ohms to measure current flows up to hundreds of amps. Specifically, the Ohm's law is exploited to indirectly measure the values of current by means of the measurement of the voltage across the resistor.

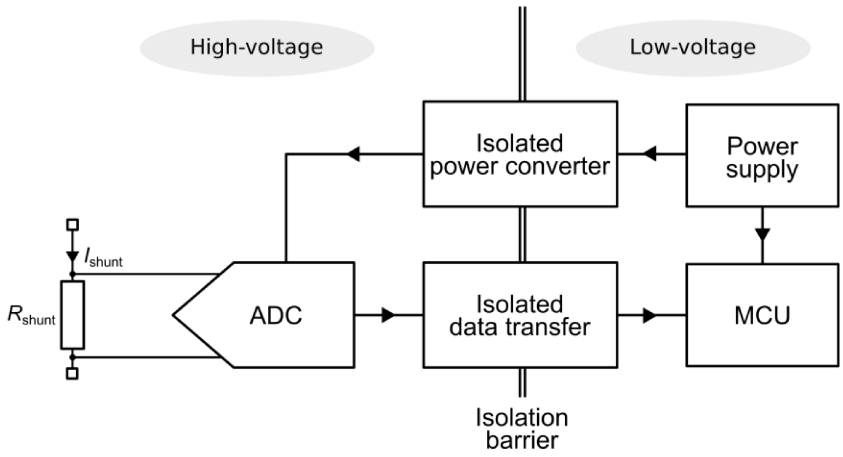



Fig. 1.10. Simplified current-monitoring system architecture based on the shunted-resistor technique.

By referring to Fig. 1.3, the user interface must be separated from measurement side since the current levels to be measured can involve lethal effects on human beings. Therefore, an isolation barrier is exploited to provide the separation between low voltage and high voltage sides. Moreover, an analog-to-digital converter is typically used on the high voltage side to send digital data information across the galvanic isolation barrier. The supply power for the ADC and the other circuits on the isolated side is provided by

an isolated dc-dc converter, while a digital data isolator performs data transmission from ADC (i.e., high voltage side) to the micro-controller unit (i.e., low voltage isolated side). The power consumption of the ADC is about few milliwatts thus requiring a low power dc-dc converter, while the specifications for the digital data isolator are related to data communication speed which depends on the specific application.

### 1.3.3. Gate drivers

Renewable energy sources have gained a lot of interest in the last years due to their *green* impact on the environment. Clean alternatives, such as photovoltaic plants and wind turbines entail power conversion systems that can handle power from hundreds of watts to several kilowatts. Therefore, human safety and protection of low power circuits are essential in these applications [18].

Switched-mode power electronics is the common technique which is adopted in modern power conversion systems since it achieves high efficiency both for power conditioning and control. An example of power conversion system is the gate driver for motor control. Fig. 1.11 shows a simplified architecture for motor drive applications which exploit a half-bridge topology for the N-type power switches [19]. Power MOSFET and IGBT-based inverters transform a rectified input voltage into a variable frequency voltage that drives a motor. The gate drivers are the interface between the controller and the power stage. They minimize conduction loss and switching time of the power switching devices, while avoiding destructive conditions that occur when both devices, $Q_1$ and $Q_2$, are conducting at the same time.

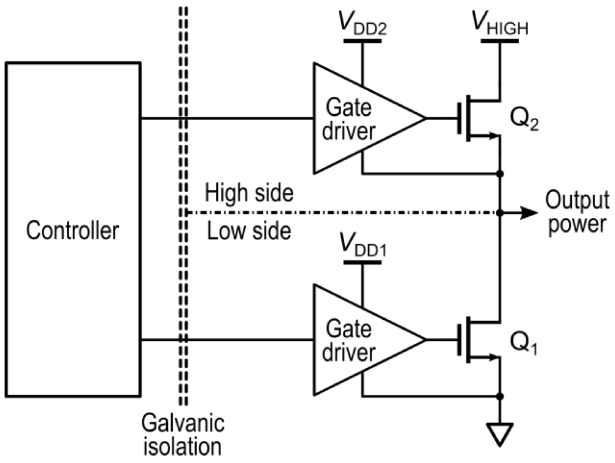



Fig. 1.11. Simplified half-bridge circuit.

The supply voltages for the gate drivers on the low-side and high-side are $V_{DD1}$ and $V_{DD2}$, respectively. It can be noticed that the value of $V_{DD2}$ must be very close to the ones of $V_{HIGH}$ for proper operation of the power switch $Q_2$. In such a condition, boost capacitors technique is typically exploited but it poses limitations on the start-up, the duty cycle, and the maximum off time for the high-side switches of the converter. while latch-up on the low-side gate-driver can occur during inductive spikes or free-wheeling diode conduction. These limitations and the risk of latch-up can be eliminated by providing to each gate driver an auxiliary galvanically-isolated supply voltage, while connecting each gate driver's ground to the source of the corresponding power switch. As a result, galvanic isolation is provided not only between controller and gate drivers but also between the low-side and high-side.

The main applications of gate driver are 600/1200V inverters, UPS equipment, solar inverters, and motor drivers in hybrid and electric vehicles [20], [21]. Common IGBTs can require a gate charge of about hundred

nano-coulombs and a voltage swing higher than 6 V [22]. According to such specification a galvanically-isolated dc-dc converter with an output power of few hundreds of milliwatts with an output voltage higher than 6 V can be exploited as auxiliary power supply for isolated gate drivers.

## 1.4. State-of-the-art

Traditionally, galvanic isolation is provided by means of optocouplers and discrete transformers which allow data transmission and power transfer, respectively. Actually, research interests are addressed towards the miniaturization of galvanic isolators, both in academic and industrial environments. The main reason is the implementation of less bulky and expansive systems than the aforementioned traditional solutions.

Galvanically isolated silicon-integrated data transmission systems have been proposed in [23]-[26], which exploit RF links [23] or capacitive [24] and magnetic coupling [25], [26] to provide galvanic isolation. The magnetic approach is also used to implement power transfer across a galvanic barrier since it provides a more efficient solution than the capacitive ones. Consequently, isolation transformer is becoming the most promising solution for the implementation of galvanic isolation since it allows both power and data transfer. Recently, several efforts have been made to improve the integration level of the inductive components by means of post-processing devices [27] (i.e., micro-transformers) or directly on silicon wafer [28]-[30] (i.e., on-chip transformer). This section provides an overview of galvanic isolators throughout the past years, from the traditional optocouplers to the most recent micro and on-chip transformers.

### 1.4.1. Optocouplers

The optocouplers were introduced at the end of 1970s and provide the highest level of galvanic isolation in data transfer systems. The data communication between the two isolated interfaces is performed by converting electrical signal to light, typically near the infrared region.

Fig. 1.12(a) and Fig. 1.12(b) depict the internal structure of an optocoupler and the x-ray scan of a device [31], respectively.

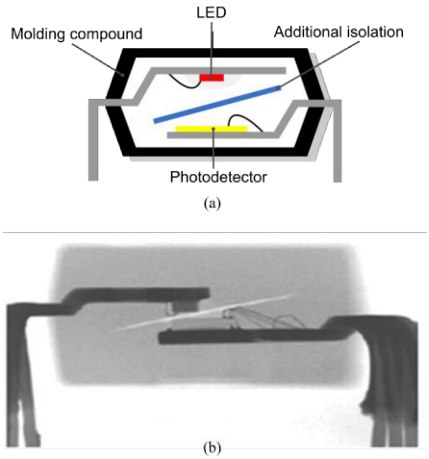



Fig. 1.12. (a) Typical optocoupler structure and (b) X-ray cross-section.

The architecture of an optocoupler is made up of an infrared light emitting diode and a photo-sensitive device (photodetector). The LED converts analog or digital signals to light which is detected by the photodetector. The latter recover data signals by re-converting the light to electrical signals. Both LED and photodetector are placed on two different metal frames which are separated by a physical gap depending on the isolation rating of the device. This gap can contain one or more additional transparent isolation layers to

improve isolation performance while reducing input-output coupling capacitance [32]. Finally, a plastic package enclosures the overall structure thus shielding from external light source and mechanical stresses.

Fig. 1.13 shows the common equivalent circuit of an optocoupler. The speed of data transmission depends on the bandwidth of the device and is related to the biasing current. Typically, data rates of about ten megabits/s require a biasing current of ten milliamps. The input current, $I_{IN}$, is required to turn on the LED, while the output current, $I_{OUT}$, is provided by the photo-transistor when the light is detected. The ratio between $I_{IN}$ and $I_{OUT}$ defines the current transfer ratio. It can be noticed that CTR depends on the photo-transistor current gain which is affected by variability due to biasing current, temperature and process variations. These dependencies are accentuated by the aging degradation of the LED brightness, which is accelerated by the high working current level of the device. This leads to a trade-off between performance and lifetime of optocouplers, which makes more complex their design.

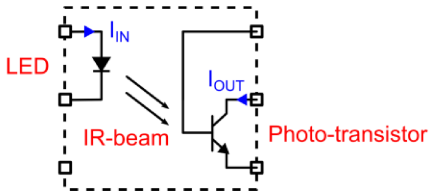



Fig. 1.13. Simplified schematic of an optocoupler device.

### 1.4.2. Capacitive isolators

Capacitive isolators rely on high-voltage capacitors to sustain the required voltage rating and provide isolation. Although advanced technologies for the

implementation of high-performance isolation capacitors have been proposed [33], the most diffused isolation approach in CMOS silicon technology exploits the inter-metal dielectric, i.e. silicon dioxide, to realize low-cost isolation capacitors that enable the mass production of fully integrated digital isolators. $SiO_2$ presents several advantages such as high dielectric strength (i.e., as high as 850 V/μm [33]) which provides high isolation performance by using thin dioxide layer. Moreover, $SiO_2$ layers are available in most silicon back-ends, thus achieving high integration level by combining CMOS devices and isolation barriers on a single die.

Fig. 1.14 shows a typical capacitive isolator system [34] with simplified cross section of the high voltage capacitor.

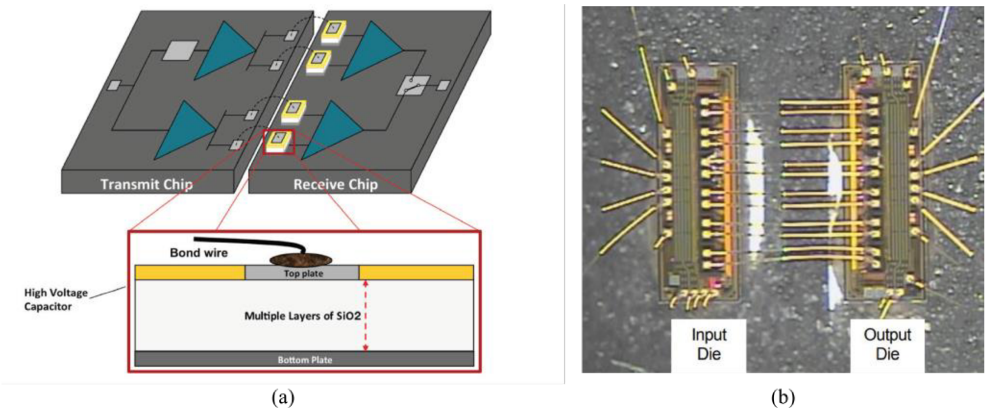



Fig. 1.14. (a) Typical capacitive isolator system with simplified cross section of the high-voltage capacitor. (b) Photo of a six-channel capacitive digital isolator.

The top and bottom plates of the capacitor are implemented by using standard metal layers, while several layers of thin-film $SiO_2$ provide the galvanic isolation. Two dice attached on separate metal frames house transmitters and receivers, respectively. The receiver chip in the figure houses

the isolation capacitor, whose top plate is connected to the transmitter output by bonding wires. Fig. 1.14(b) shows a micrograph of the isolator before packaging. Six data channels have been implemented within two chips. A great advantage of capacitive digital isolators is the low power consumption, typically only few milliamps in the state-of-the-art. In addition, a high common-mode transient immunity performance can also be achieved. These features make capacitive isolators a more reliable solution compared to optocouplers. The state-of-the-art of capacitive digital isolators includes also systems with reinforced isolation [8], which can be implemented simply by series connecting more isolation capacitors.

The capacitive isolators are typically adopted to implement data communication systems, while they are not suitable for power transfer applications. For instance, Fig. 1.15 shows the power transfer across the capacitive isolation barrier which is implemented by capacitors $C_{ISO}$. Resistor $R_L$ and capacitor $C_L$ are the external load to be supplied. It can be notice that the ac input voltage, $V_{IN}$, is highly reduced at the load level due to the capacitive partition between $C_{ISO}$ and $C_L$ which causes ac power loss and power efficiency degradation. The reduction of output power for a given input power is also due to the bottom plate parasitic capacitances of $C_{ISO}$ which decrease the isolation barrier efficiency.

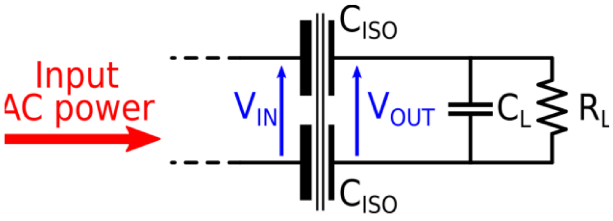



Fig. 1.15. Simplified electrical scheme for power transfer system.

The power efficiency degradation can be limited by means of subharmonic resonant approach [35], but the isolation rating of such system is lower than the state-of-the-art results.

### 1.4.3. Magnetic isolators

The magnetic coupling is the most suitable approach to provide galvanic isolation since it allows both power and data transfer. A typical data transfer architecture consists of a transmitter and a receiver, which exchange data information through a planar isolation transformer by using either amplitude shift keying modulated RF signals or voltage pulses. Fig. 1.16 depicts the simplified block diagram of data transfer system with magnetic isolator.

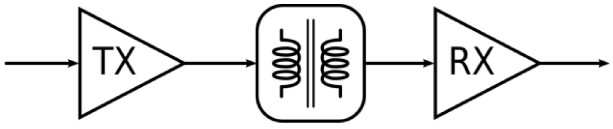



Fig. 1.16. Data transfer architecture for magnetic isolator systems.

The transformer can be housed in a standalone chip or can be placed within the transmitter or receiver die, thus achieving the highest level of integration (i.e., only two chips). The first highly integrated magnetic isolators were introduced by the Analog Devices in 2001 with the iCoupler technology [36]. The iCoupler technology adopts micro-transformers realized with post processing steps to implement a multi-chip System in Package solution. A cross-section of the iCoupler technology is shown in Fig. 1.17(a). Galvanic isolation up to 5-kVrms is performed by a 20-25 μm-thick polyimide layer, which separates the two windings of the micro-transformer. The top coil of the transformer exploits a 4 μm-thick electroplated Au layer, while the bottom

spiral is realized on a standard IC top metal layer. A photo of a four-channel digital isolator realized with the iCoupler technology is shown in Fig. 1.17(b). State-of-the-art transformer-based digital isolators have maximum data-rate up to 6000 Mbs. Thanks to a lower parasitic capacitance between the two interfaces they also exhibit a better CMTI performance than capacitive isolators, though magnetic isolators require a more advanced technology.

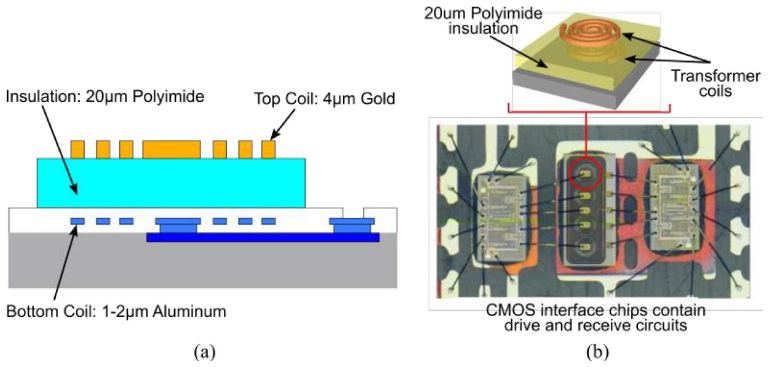



Fig. 1.17. iCoupler technology. (a) Cross-section. (b) Photo of a four channels digital isolator before packaging.

Differently from optocouplers and isolation capacitors, magnetic isolators provide an efficient solution to implement power transfer across a galvanic barrier. Fig. 1.18 shows the simplified block diagram of a power transfer system which exploits a magnetic isolator.

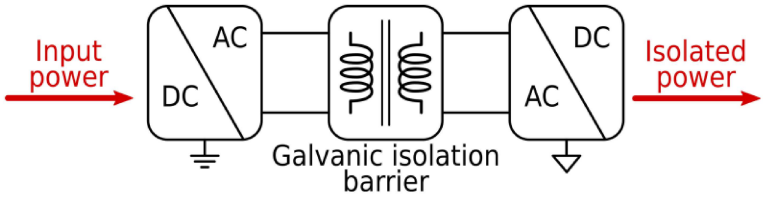



Fig. 1.18. Power transfer system architecture.

The key component of such a system is the transformer which provides the galvanic isolation between the two separated interfaces. Since the transformer allows the ac signals transmission while rejecting the dc component, both dc-ac and ac-dc converters are exploited to transfer power across the galvanic barrier and convert back the ac power to the dc isolated output power, respectively. The isolation transformer is typically implemented on-chip or by post-processing steps.

Fig. 1.19(a) depicts the cross-section of the isoPower technology [37] which has been introduced by Analog Devices to realize power micro-transformers.

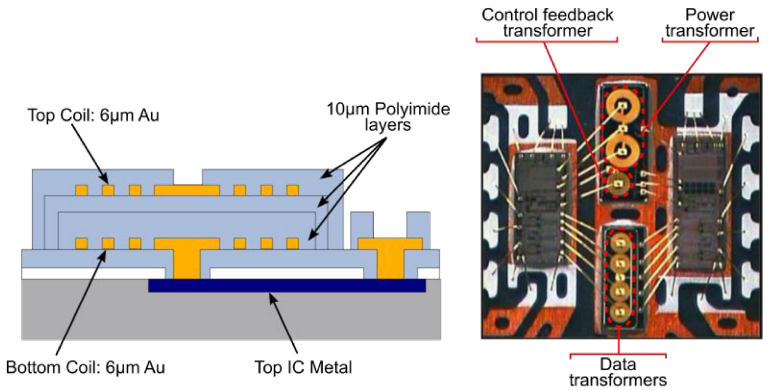



Fig. 1.19. (a) Cross-section of the isoPower technology. (b) Photo of an isolated dc-dc converter with 4 isolated data links before packaging.

Both transformer's coils are implemented with thick Au metals to achieve good efficiencies. Fig. 1.19(b) shows the first multi-chip SiP dc-dc converter which combines power and data transfer capability by adding isolated data channels within the same multi-chip SiP solution. Based on this approach,

many products are available on the market [38] which deliver output power levels ranging from tens to hundreds of milliwatts, while providing separated isolated channels for data communication. Differently from the commercially available products, an interesting architecture of isolated dc-dc converter with data transmission was proposed in [39], [40]. It uses the same transformer for both data and control feedback signals thus reducing the number of isolated channels and hence the overall costs of the system. However, the best results for the reduction of the power density (i.e., the ratio between the output power and the overall area of the system) has been achieved thanks to the fully-integrated on-chip isolation transformers which have been introduced by STMicroelectronics in [41], [42]. Nowadays, only digital data isolators exploiting this technology are commercially available [20], but the power transfer feasibility was demonstrated by several fully integrated systems with power levels ranging from 20 mW to 1 W [28]-[30]. The key of this technology is the possibility to implement both active devices and isolation transformers within the same die thus leading to a two chips implementation of an isolated system. It is achieved thanks to a standard 0.35-μm-BCD process enriched with a thick-oxide module in the back-end-of-line that provides a 5-kV isolation rating between the two top metal layers thus ensuring basic isolation. The scanning electron microscope (SEM) cross-section of the four metals back-end along with the photo of a 200-mW two-chips dc-dc converter assembled on board [29] are shown in Fig. 1.20(a) and Fig. 1.20(b), respectively. Higher level of integration (i.e., only two chips) and competitive power efficiencies (i.e., from 10% to 30%) has been achieved with respect to the isolated systems which exploit isoPower technology.

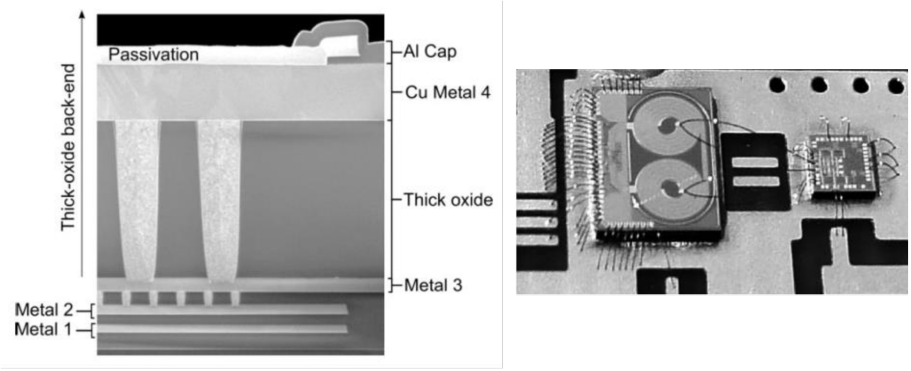



Fig. 1.20. (a) SEM cross-section of the 0.35-µm BCD process metal stack with thick-oxide option. (b) Photo of a 200-mW isolated power transfer system assembled on board.

## 1.5. Thesis overview

The big challenge in the design of dc-dc converters with galvanic isolation is the reduction of the number of isolated links while performing the required power and data functionalities. The main reasons can be summarized in the decreasing of both system complexity and system area occupation, with evident advantages in terms of reliability and manufacturing costs. In the last decade, several architectures of power and data transfer systems with galvanic isolation have been proposed [28], [40], [43], as shown in Fig. 1.21.

Commercially available products [43] exploit at least four isolated links which consist of:

- An isolated link for the power transmission (isolated power channel);
- An isolated link for the feedback loop of the output power control;

- At least two isolated data links for bidirectional data communication (i.e., from A to B and from B to A).

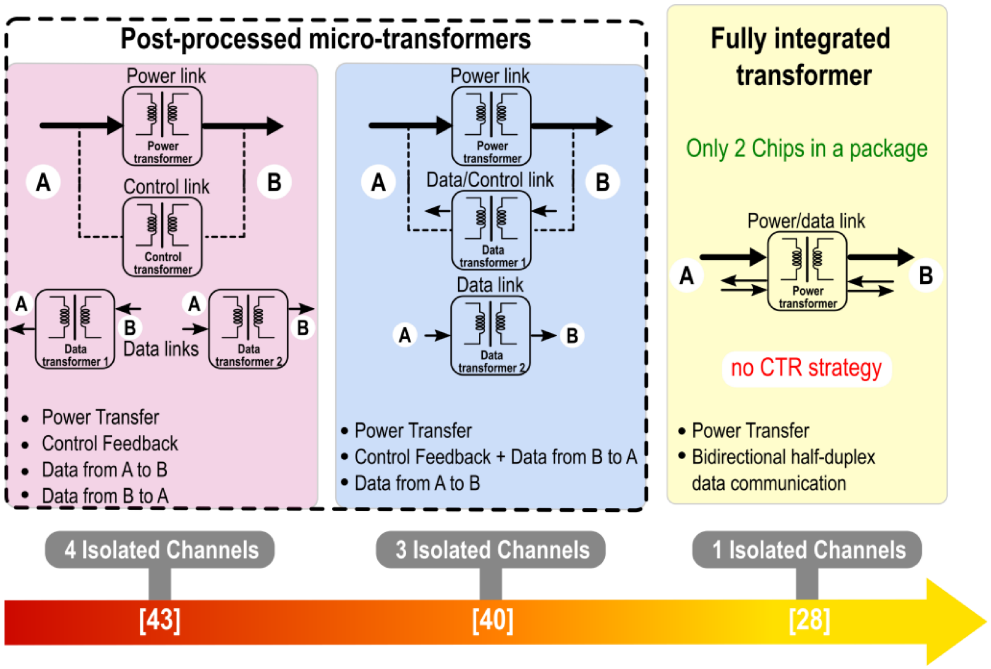



Fig. 1.21. Architectures of power and data transfer systems with galvanic isolation.

The number of isolated links has been reduced from four to three channels in [40]. As mentioned in the previous section, the isolated control channel is avoided, and the control signal is multiplexed into the data bit streams which are transmitted from B to A.

Finally, the architecture in [28] implements power and data transfer by using a single isolated channel. Specifically, it exploits an ASK modulation of the power signal to perform bidirectional half-duplex data communication.

However, the output power control is not performed, and a further isolated link is required to implement the dc-dc converter functionality.

By referring to the main limitations of the state-of-the-art architectures for isolated power and data transfer, this thesis focuses on circuit and system design techniques to implement galvanically isolated dc-dc converters, with or without data communication, exploiting the minimum number of isolated links. Therefore, novel architectures which are able to perform power and data functionalities by sharing the same isolated link have been proposed during my research activity at the *RF-ADC*. It is worth noting that technology aspects regarding the implementation of galvanic isolation are not covered, since the whole technology platform was supplied and tested by STMicroelectronics.

In the next sections, the adopted technology platforms and the design procedure for both area and efficiency performance optimization will be presented. Finally, the topics of this work will be described highlighting the main results.

### 1.5.1. Technology platform

This section presents the manufacturing processes which have been exploited for the implementation of the proposed systems, with emphasis on the technology platform used for the realization of isolation components.

Fig. 1.22 depicts the typical architecture of a power transfer system with galvanic isolation which consists of a VHF power oscillator (i.e., the dc-ac converter), an isolation transformer (i.e., galvanic isolator) and a rectifier (i.e., the ac-dc converter). It is worth noting that the integration level of the system depends on how the transformer is implemented. Post-processing

transformers achieve good efficiency performance but lead to a three chips implementation since the isolation component is manufactured in a standalone chip, i.e., chip T in Fig. 1.21(a). On the other hand, a two chips implementation can be achieved by manufacturing the isolation component on the same chip of the VHF oscillator, i.e., chip A in Fig. 1.22(b). This is obtained thanks to the BCD technology provided by STMicroelectronics.

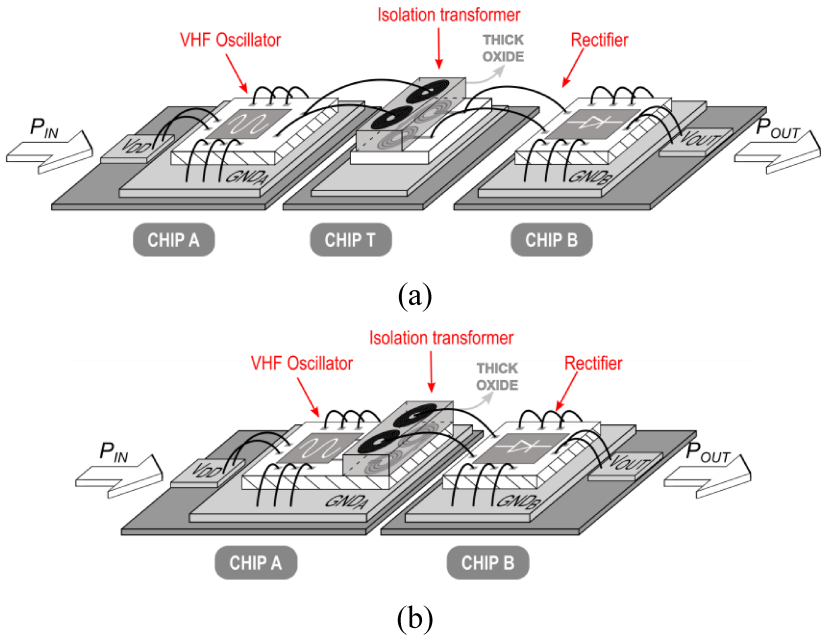



Fig. 1.22. Typical architecture of a power transfer system with galvanic isolation. (a) Three chips implementation; (b) two chips implementation.

The cross-section of the adopted post-processing technology is shown Fig. 1.23(a) and consists of thick Au metal layers exploited for the transformer's coils and a polyimide layer which guarantees the galvanic isolation between primary and secondary windings. The deposition of the polyimide layer is provided by means of step-by-step processes which allow different thickness

to be implemented. Consequently, different levels of isolation (from basic to reinforce) can be achieved.

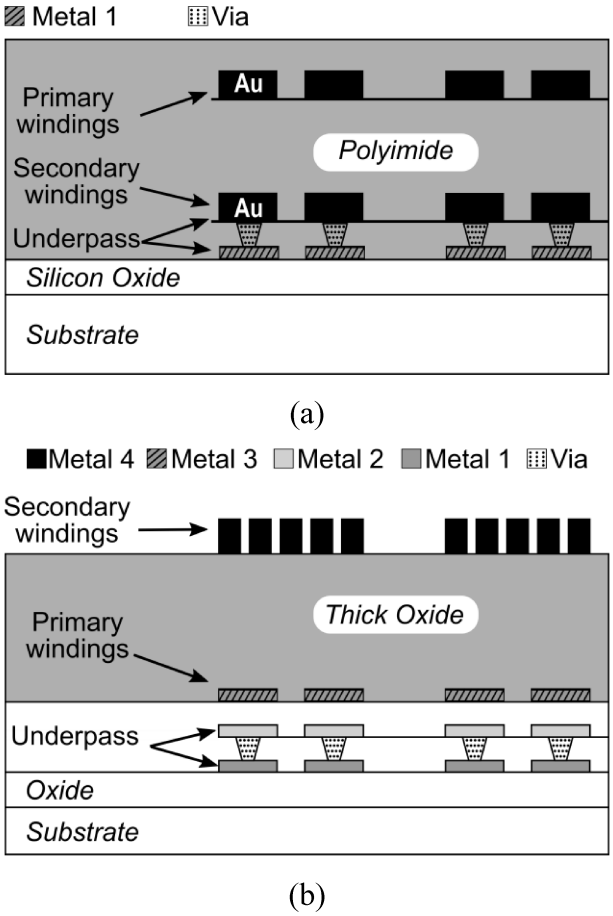



Fig. 1.23. Cross-section of: (a) prost-processing technology and (b) BCD back-end for galvanic isolation.

Finally, Fig. 1.23(b) depicts the cross-section of the 0.35-µm SOI-BCD process. This technology features both 3.3-V and 5-V CMOS transistors and several lateral-diffused MOS devices for high-voltage capabilities. Three Al metal layers with 0.45/0.55/0.9 µm thickness, respectively, and a 3.7-µm

thick top Cu layer are available for routing. The process was enriched with a thick-oxide module of several μm of thickness, which has been tested by the technology provider for a 5-kV isolation rating [42]. The primary and secondary windings of the transformer are implemented with the third and fourth metal layers, respectively, being the thick oxide located between these metals. An isolation rating of 6 kV can be also achieved by using the oxide layer between metal 3 and metal 2.

The third technology adopted in this work is a 0.13-μm standard CMOS process which provides high voltage Schottky diode with sub-GHz operation capability for the rectifier implementation.

All technologies were provided by STMicroelectronics.

### 1.5.2. Main results

During my research activity, three novel architectures for galvanically isolated converters have been designed with different target of applications. The proposed systems overcame the main limitations of the state-of-the-art solutions concerning the implementation of more than one power and data functionalities by sharing the same isolated link, thus drastically reduce silicon area, package size and hence costs of the overall system.

Firstly, a 6-kV isolated dc-dc converter with bidirectional half-duplex data communication up to 50 Mb/s has been designed. It takes advantage of the BCD process enriched with a thick-oxide module to implement fully-integrated on-chip isolation transformers, thus achieving the highest level of integration. Indeed, the converter is made up of only two dice. Moreover, a novel control feedback loop is provided which allows data

communication to be performed on the same control channel. Therefore, only two isolated components have been exploited which are the control/data link and the power link. The latter delivers up to 93 mW output power and output voltage ranging from 2.4 V to 3.3 V thus providing an efficient solution for many applications both in medical and consumer environments.

The second system is mainly addressed to gate driver applications. It is a 100-mW step-up dc-dc converter providing around 20-V output voltage from 5-V supply voltage. The main object of this system was to perform control feedback loop on the same isolated link exploited for power transfer by means of data communication.

Finally, the third system is a galvanically dc-dc converter which has been designed to meet the requirements of sensor applications. It exploits the power link both for control feedback loop and data communication of N data channels. Therefore, it definitively provides the minimum number of isolated link while performing the required power and data functionalities which are: power transfer, data communication and control feedback loop.

It is worth noting that power and data functionalities of the proposed systems do not depend on the technology platform used for the isolation components, which can be manufactured either in post-processing steps or exploiting the SOI BCD technology. However, the technology platforms greatly affect both efficiency performance and power density.

The architecture description of the first system is presented in Chapter 2 along with experimental results which have been recently published in [44].

The second and third system are described in Chapter 3 and Chapter 4, respectively. They exploit a post-processed transformers which are under manufacturing. Therefore, simulation results have been provided for the sake

of completeness. The characterization of these two systems will be done as soon as possible. All the three architectures have been patented [45]-[47].

# Chapter 2.

# A fully integrated galvanically isolated dc-dc converter with data communication

## 2.1. Introduction

This chapter presents a fully integrated galvanically isolated dc-dc converter with data communication which exploits only two isolated links. As introduced in the first chapter, the reduction of the number of isolated links is mandatory to reduce application cost and size while maintaining all power and data functionalities. The minimum number of isolated links has been achieved by [28] in which only one isolated link is used for both power transfer and bidirectional half-duplex data communication. The main idea is

to use the isolated power channel also for a bidirectional (half-duplex) data communication by means of an ASK modulation of the power signal at the primary or the secondary windings of the isolation transformer. However, variable power functionality is not included since data communication on power channel is not compliant with an efficient power control that exploits on/off modulation (i.e., PWM modulation, Bang-Bang control scheme). Indeed, data communication requires the presence of the power signal while on/off modulation involves shutdown of the power oscillator to preserve efficiency. Moreover, considering that power and data use the same channel, important performance such maximum output power, power efficiency, data rate, and common mode transient immunity must be traded-off. Specifically, high efficiency power transfer requires large isolation power transformer which involves high parasitic capacitances between primary and secondary windings. This is against the need for a high CMT rejection.

To maximize power efficiency while performing high CMT rejection on data communication, power and data must be separated and a further transformer is needed. Based on these considerations, an improvement of the architecture in [28] is proposed. Fig. 2.1 shows the block diagram of the proposed architecture. The basic principle is to use an additional isolated link to feedback the signal control for power regulation purpose. This control link is also used to perform data communication between the two isolated interfaces. In this way the power link is dedicated for power transfer only, and it can be designed to maximize system efficiency without constrains due to CMT rejection performance.

The proposed dc-dc converter delivers up to 93-mW output power with 19% maximum power efficiency and an output voltage ranging from 2.4 V to

3.3 V, while achieving a data rate up to 50 Mb/s. The variable output power control enables a large range of low-power applications, e.g. sensor interfaces requiring up to 100 mW of isolated output power.

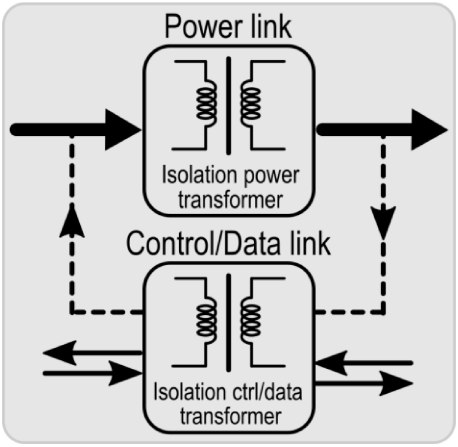



Fig. 2.1. Basic principle of the proposed architecture.

## 2.2. System Description

The simplified block diagram of the proposed system is depicted in Fig. 2.2. The converter is based on a novel architecture [47], which consists of a dedicated isolated link for high efficiency power transfer and an isolated signal link that is used for both output voltage/power regulation and bidirectional half duplex data communication. The dc output voltage, $V_{ISO}$, is delivered from chip A to chip B across the galvanic barrier thanks to a power link, which is made up of a power oscillator operated at 350 MHz, an isolation transformer, $T_P$, and a power rectifier. Output voltage $V_{ISO}$ is regulated in the range 2.4 V−3.3 V by means of a feedback control link that exploits a

low-power RF oscillator operated at about 900 MHz, whose oscillation amplitude changes according to the output power imposed by reference voltage $V_{REF,OUT}$ and load resistance $R_L$. The galvanic isolation of the control link is guaranteed by the transformer, $T_D$. The oscillation voltage of the RF oscillator is the control variable. It drives the power control block that produces a pulse width modulated signal, $V_{CTR}$, to turn on and off the power oscillator. The frequency, $f_{PWM}$, of control signal $V_{CTR}$ is the switching frequency of the power oscillator and can be set up to few hundreds of

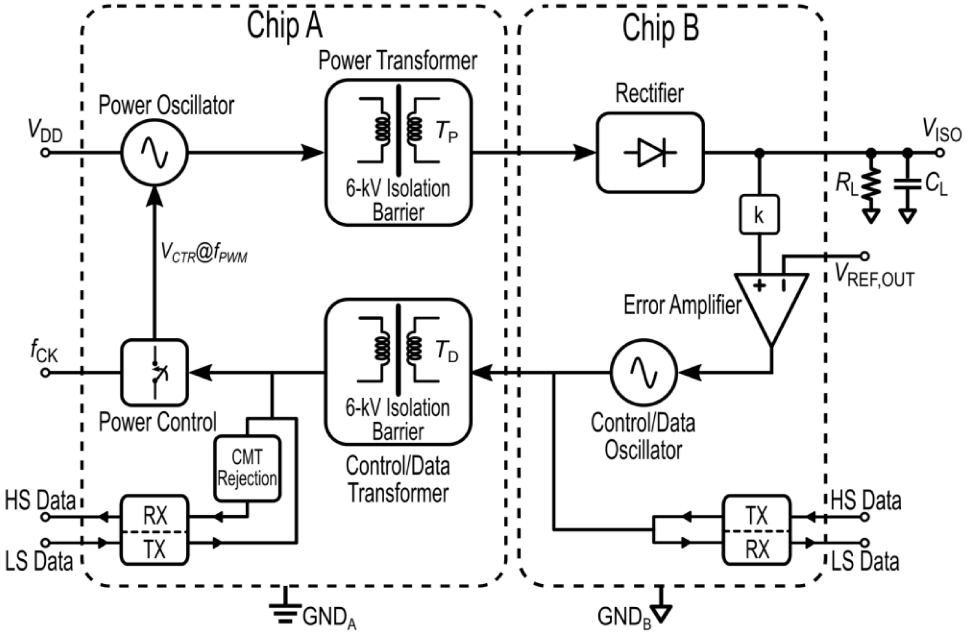



Fig. 2.2. Simplified block diagram of the dc-dc converter with bidirectional data communication.

kilohertz. PWM power control preserves system power efficiency while allowing a wide range of power levels to be achieved. The control link is also exploited for bidirectional half-duplex data communication by means of

amplitude modulation of the RF oscillation signal [28], [47]. High speed data stream from chip B to chip A takes advantage of the common mode transient rejection block to improve CMT immunity. A low speed data communication from chip A to chip B is also provided for those applications where configuration data are required to set chip B operation.

The system was fabricated in a 0.35 µm BCD technology enriched with a galvanic isolation thick-oxide back-end provided by STMicrolectronics [41]. The thick-oxide option was used only for chip A, which includes the isolation transformers, while chip B was fabricated in a standard BCD technology. Differently from traditional galvanic isolation approaches [39], [40], [48]-[53], the transformers are completely integrated into the silicon technology and do not use post-processing steps or discrete components [28]. An isolation rating, $BV_{AC}$, of 5 kV is guaranteed by the oxide layer between a Cu-thick metal 4 and an Al-thin metal 3, while 6 kV isolation can be also achieved by using the oxide layer between metal 3 and metal 2. The isolation performance was previously assessed by the technology provider using several test structures [41]-[42].

## 2.3. Power Link

The power link is the core of the dc-dc converter and determines the efficiency performance of the overall system. It was designed to deliver a dc output power, $P_{ISO}$, higher than 100 mW at a nominal output voltage, $V_{ISO}$, of 3.3 V with a 3.3 V power supply, $V_{DD}$. A simplified schematic of the power link is shown in Fig. 2.3. The architecture is made up of a transformer-based

power oscillator and a capacitive-coupled full bridge rectifier, which perform dc-ac and ac-dc conversions on chip A and chip B, respectively. Coupling capacitors $C_C$ are properly exploited to optimize the performance of the dc-ac conversion. The power oscillator benefits of high current/high voltage LDMOS transistors, $M_{1,2}$, which are operated in D class [54] thus producing an oscillation amplitude of about two times

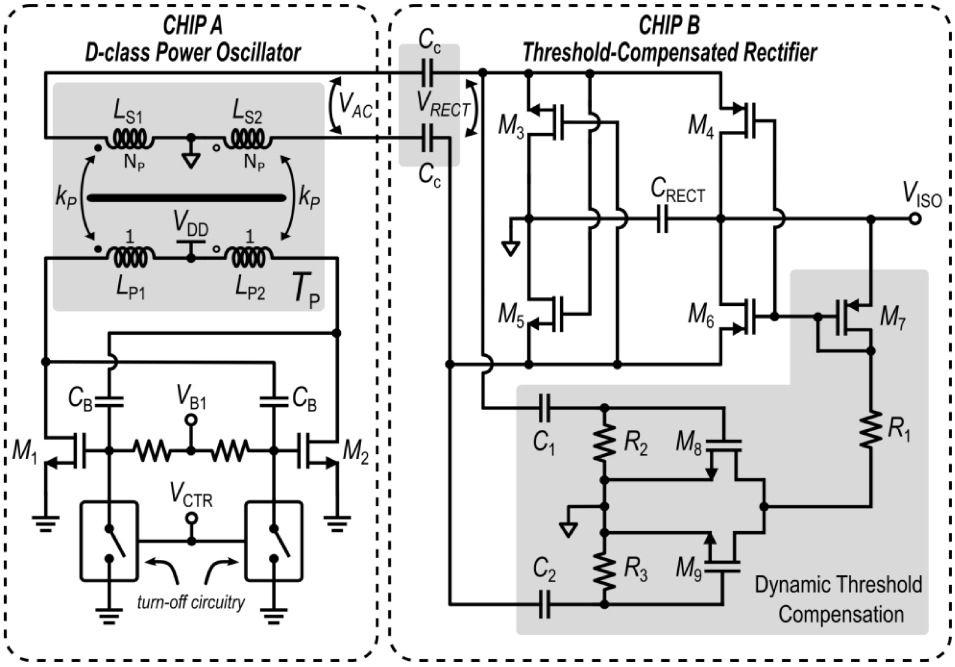



Fig. 2.3. Power link schematic.

the supply voltage (i.e., about 7 V), which maximizes power efficiency. A capacitive partition performed by coupling capacitors $C_B$ with the gate-source capacitances of $M_{1,2}$ is used to set the peak value of $V_{GS}$ and avoid gate-oxide breakdown. The on-off switches driven by PWM signal $V_{CTR}$ allow cross-coupled pair $M_{1,2}$ to be properly switched, thus delivering a variable

output power at constant efficiency. Isolation transformer $T_P$, here represented as magnetically coupled inductors, adopts a differential stacked configuration [30], as shown in Fig. 2.4. Primary ($L_{P1,2}$) and secondary ($L_{S1,2}$) windings are built in metal 2 and metal 4, respectively, to guarantee 6 kV galvanic isolation rating. The lower metallization layer of the process (i.e., metal 1) is exploited

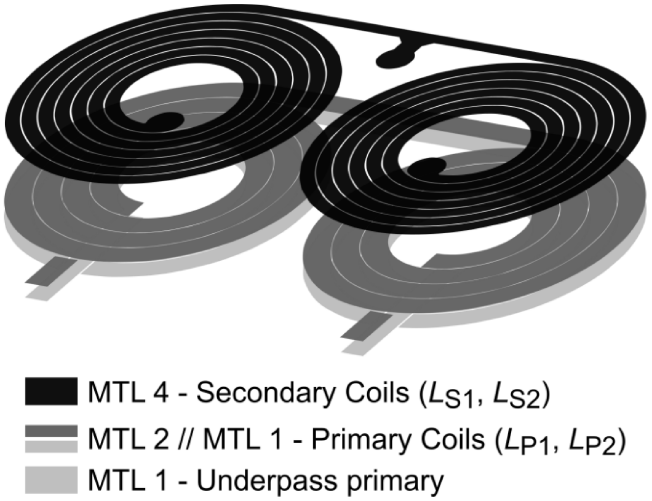



Fig. 2.4. Structure of the power isolation transformer ($T_P$).

TABLE 2.1
GEOMETRICAL PARAMETERS OF THE POWER TRANSFORMER.

| **Parameters** | **Primary Coil (half structure)** | **Secondary Coil (half structure)** |
|---|---|---|
| Number of turns ($n$) | 3.5 | 6.5 |
| Width ($w$) [µm] | 69.4 | 36.3 |
| Spacing (s) [µm] | 1 | 5 |
| Internal diameter ($d_{IN}$) [µm] | 300 | 300 |
| Outer diameter ($d_{OUT}$) | 841 | 841 |

for the underpasses and selectively shunted to metal 2 to reduce the resistive losses of the primary winding. The geometrical parameters of half of the transformer coils are summarized in the Table 2.1. With a transformer ratio, $N_P$, of about 2, $T_P$ performs a voltage step-up conversion, thus producing a peak voltage of about 12 V at the secondary winding. Finally, the oscillation voltage is properly reduced to comply with the breakdown limit of the rectifier transistors, $M_{3\text{-}9}$ (i.e., about 5.5 V), by means of the partition between coupling capacitors $C_C$ and the rectifier input admittance, $Y_{RECT}$, Therefore, such architecture performs a double conversion, i.e. a step-up followed by a step-down conversion, by means of the transformer turn's ratio, $N_P$, and the capacitive partition at the rectifier input, respectively. A simplified expression for the voltage gain of the power links is reported below:

$$\frac{V_{ISO}}{V_{DD}} \cong 2k_P N_P \cdot \left| \frac{4\pi j f_P C_C}{4\pi j f_P C_C + Y_{RECT}} \right| \cdot \frac{2}{\pi} \cong 1 \qquad (2.1)$$

where $f_P$ is the power oscillation frequency, $k_P$ is the magnetic coupling factor of $T_P$ and $2/\pi$ is the ideal conversion loss of the rectifier. In a standard dc-dc converter architecture (i.e., without capacitors $C_C$) $N_P$ would be around unity ($k_P \approx 0.8$) to guarantee an almost unitary $V_{ISO}/V_{DD}$ voltage gain, thus limiting the oscillation amplitude at the drains of $M_{1,2}$ (i.e., less than $2V_{DD}$) and hence reducing the oscillator core efficiency. Thanks to this step-up/step-down architecture, an improvement of the oscillator active core efficiency of about ten percentage points is achieved, which turns in an improvement of the dc-ac conversion efficiency of about five percentage points.

The ac-dc conversion is performed by a CMOS full bridge rectifier with a dynamic gate biasing. Indeed, transistors $M_4$ and $M_6$ in a full-bridge rectifier topology are diode connected or use static gate biasing. However, both approaches reduce the conversion efficiency especially at high current level. Indeed, the former is affected by the threshold voltage [28] and the latter by the reverse current on the on-chip rectifier capacitance, $C_{RECT}$. The proposed dynamic gate biasing overcomes these limitations since it sets the gate voltages of $M_4$ and $M_6$ to $V_{ISO}-V_{TH}$ only when the current flows towards the load, otherwise both $M_4$ and $M_6$ are turned off to prevent the flow back currents [55], thus preserving power efficiency.

The rectifier design was based on a trade-off between the conversion efficiency, $\eta_{RECT}$, and the reactive part of $Y_{RECT}$ [30]. Moreover, a trade-off is also required for the oscillation frequency. Indeed, a higher oscillation

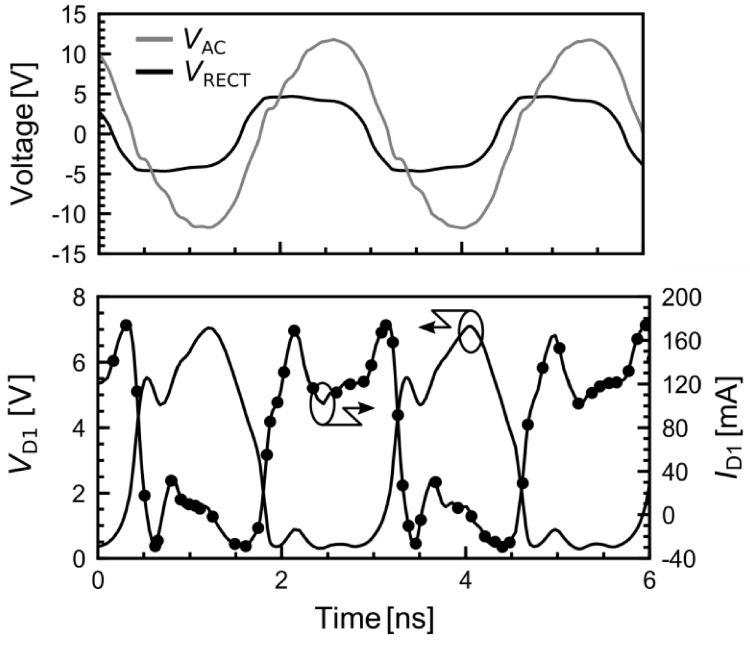



Fig. 2.5. Power link simulated *V*/*I* waveforms ($P_{ISO}$ = 100 mW, $V_{ISO}$ = 3.3 V).

frequency usually improves the power oscillator performance, but it can negatively impact the rectifier efficiency due to its frequency limitation. The power link optimization was carried out using the approach in [30] by means of an iterative EM based co-design between the oscillator core and the transformer.

Fig. 2.5 shows simulated single-ended voltage/current waveforms at the LDMOS drains, differential voltage $V_{AC}$ at the secondary windings of $T_P$, and rectifier input voltage $V_{RECT}$.

For the sake of completeness, the design parameters of the overall power link are summarized in Table 2.2, whereas Table 2.3 reports the simulated efficiency breakdown of the power link at maximum $P_{ISO}$ and at $V_{ISO}$ of 3.3 V.

The bottleneck for the overall power link efficiency is represented by the isolation transformer that is further exacerbated since a 6-kV isolation

TABLE 2.2
DESIGN PARAMETERS OF THE POWER LINK.

| Block | Parameter | Value | Unit |
|---|---|---|---|
| Power oscillator active core | $W_{1,2}$ | 2.36 | [mm] |
| | $C_B$ | 2.6 | [pF] |
| | $V_{B1}$ | 1 | [V] |
| | $f_P$ | 350 | [MHz] |
| Isolation transformer, $T_P$ | $L_{P1,2}$ \| $L_{S1,2}$ | 17.5 \| 53 @ $f_P$ | [nH] |
| | $Q_{P1,2}$ \| $Q_{S1,2}$ | 3.5 \| 7.9 @ $f_P$ | |
| | $k_P$ | 0.88 | |
| Coupling capacitors | $C_C$ | 8.2 | [pF] |
| Rectifier | $W_{3,5}$ | 0.86 | [mm] |
| | $W_{4,6}$ | 0.29 | [mm] |

TABLE 2.3
SIMULATED EFFICIENCY BREAKDOWN OF THE POWER LINK ($P_{ISO}$ = 100 mW, $V_{ISO}$ = 3.3 V).

| Block | Efficiency |
|---|---|
| Oscillator core | 72 % |
| Isolation transformer | 52 % |
| Bonding wire and coupling capacitors | 90 % |
| Rectifier | 68 % |

back-end was used. Indeed, the transformer power efficiency (as low as 52%) is manly ascribed to poor $Q$-factors (i.e., 3.5 and 7.9 for primary and secondary coils, respectively). Despite this drawback, an overall power link efficiency as high as 23 % was achieved, which is about ten percentage points higher than the one in [28]. This improvement is mainly ascribed to a better performance of the power oscillator and rectifier, as result of the proposed power link architecture and circuit arrangements.

## 2.4. Control/Data Link

The control signal for the output voltage and power regulation is related to the peak of the oscillation voltage of the control/data oscillator. Moreover, its amplitude is properly modulated to perform bidirectional half-duplex data communication across the isolation barrier. Therefore, the control and data links share the same isolation transformer, $T_D$, which is the resonant tank of the control/data oscillator within chip A. A description of the control loop along with the stability analysis is reported in Section 2.4.1, whereas the data

link is described in Section 2.4.2. Section 2.4.3 details the design of isolation transformer $T_D$.

### 2.4.1. Control Link

A simplified schematic of the control loop is sketched in Fig. 2.6. Output voltage $V_{ISO}$ is reduced by the resistive partition, $R_4$ and $R_5$ (i.e., $k$ in Fig. 2.2), and then compared with the reference voltage, $V_{REF,OUT}$, by means of an error amplifier. The output signal of the error amplifier, $V_{EA}$, drives the gate of

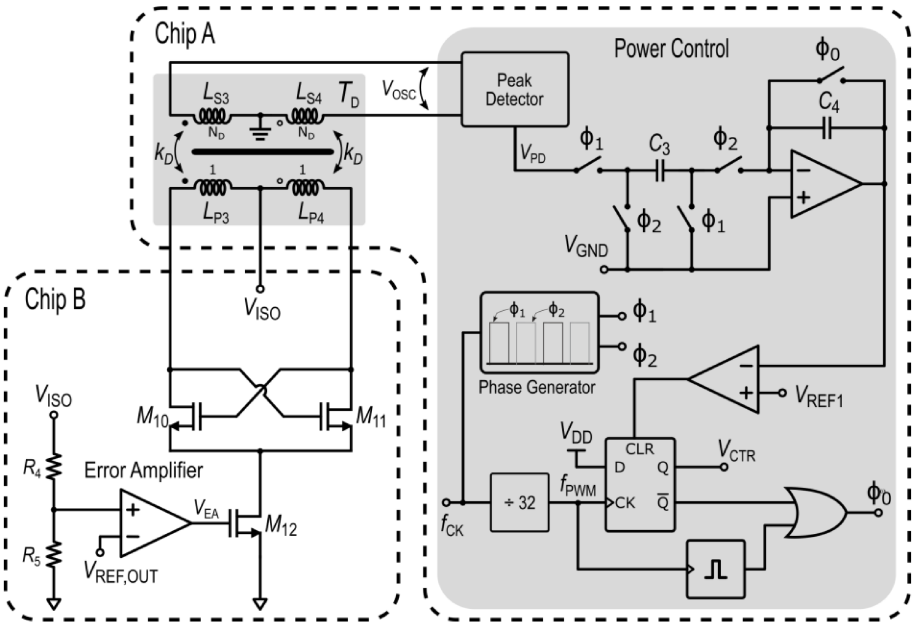



Fig. 2.6. Control link simplified schematics.

transistor $M_{12}$ that sets the bias current of the control/data oscillator. The maximum and minimum value of this current are set to provide the minimum and maximum duty cycle of the PWM control signal, which are 10% and 100%, respectively. Since the oscillation peak voltage at the secondary

winding of $T_D$ depends on $V_{EA}$, a peak detector is used to draw the control signal, $V_{PD}$, after the galvanic barrier. The peak detector has a negative gain and thus $V_{PD}$ is maximum when $V_{EA}$ is minimum and vice versa. Then, a switched capacitor integrator produces a voltage ramp whose slope is proportional to $V_{GND}-V_{PD}$, which is compared with the reference voltage $V_{REF1}$ to set the duty cycle of the control signal, $V_{CTR}$, by clearing the D flip-flop output. An external reference clock, $f_{CK}$, is exploited to generate both the non-overlapped phases $\phi_1$ and $\phi_2$ for the SC integrator and the control frequency, $f_{PWM}$ (i.e., $f_{PWM}=f_{CK}/32$). Finally, the SC integrator is periodically restored through $\phi_0$ at the beginning of each period or when $V_{CTR}$ is low. Differently from conventional continuous time control loops, the proposed approach based on the SC integrator and an external clock generator allows the PWM control frequency to be set according to the application requirements such as output ripple frequency content.

The loop stability analysis was carried out considering a single pole approximation for each block of the control loop. By referring to the simplified model in Fig. 2.7, the open loop gain, $T_O$, can be written as

$$T_0 \cong k \cdot A_{EA} \cdot A_{OSC} \cdot A_{CTR} \cdot A_P \tag{2.2}$$

where $k$ is the resistive partition, $A_{EA}$ is the error amplifier gain and $A_{OSC}$, $A_{CTR}$, $A_P$ are the gains of the control/data oscillator, the power control block, and the power link, respectively, which are given by

$$A_{OSC} = \frac{dV_{OSC}}{dV_E} = gm_{1,2}\frac{2}{\pi}R_P k_D N_D \tag{2.3}$$

$$A_{CTR} = \frac{dDC}{dV_{OSC}} = |A_{PD}| \frac{32\frac{C_3}{C_4}DC^2}{V_{GND} - V_{REF1}} \tag{2.4}$$

$$A_P = \frac{dV_{ISO}}{dDC} = \frac{1}{2}\sqrt{\frac{R_L \cdot P_{ISO,max}}{DC}} \tag{2.5}$$

being $gm_{1,2}$ the transconductance of $M_{1,2}$, $R_P$, $k_D$ and $N_D$ the equivalent loss resistance at the primary winding of $T_D$ [56], the magnetic coupling factor and the turn's ratio of $T_D$, respectively, $A_{PD}$ the gain of the peak detector, $DC$ the duty cycle of $V_{CTR}$, and $P_{ISO,max}$ the maximum power delivered to $R_L$, which can be considered constant in a first order approximation.

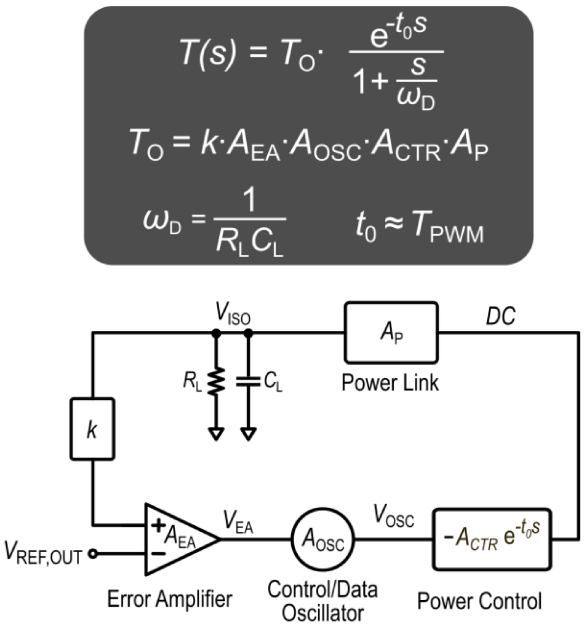



Fig. 2.7. Simplified model of the control link for stability analysis.

A single pole approximation can be used for the evaluation of the control loop frequency behavior, since high frequency poles can be neglected. The expression of open loop gain in the *Laplace*-domain is

$$T(s) = T_O \frac{e^{-t_0 s}}{1 + \frac{s}{\omega_D}} \tag{2.6}$$

where $\omega_D$ is the dominant pole due to the dc-dc converter output load (i.e., $R_L$ and $C_L$) and $t_0$ is the delay introduced by the power control block, whose maximum value is about equal to the period of the PWM control signal (i.e., $T_{PWM}$). Considering equation (2.4) and (2.5), a unitary duty cycle is the worst case for system stability since it gives maximum gain. A dominant pole compensation can be easily carried out by increasing filtering capacitance $C_L$ at the dc-dc converter output. The open loop gain, $T_O$, is about 30 dB (for DC=1), which turns out in a compensation capacitor, $C_L$, of a few microfarad to guarantee stability for a 100 kHz PWM control signal, according to

$$C_L = \frac{T_O \cdot T_{PWM}}{R_L \cdot \left(\frac{\pi}{2} - PM\right)} \tag{2.7}$$

where *PM* is the required phase margin expressed in radians. Such values of $C_L$ provide adequate performance in terms of both output voltage ripple and transient responses.

### 2.4.2. Data Link

A bidirectional half-duplex data communication is performed by using ASK modulation that preserves the peak of the RF control signal. HS (from chip B to chip A) and LS (from chip A to chip B) data transfers are performed

by means of impedance mismatch at primary ($L_{P3,4}$) and secondary windings ($L_{S3,4}$) of transformer $T_D$, respectively. To this purpose, on/off switch resistances and capacitors $C_{P1,2}$ and $C_{S1,2}$, are used as shown in Fig. 2.8. A PWM coding is adopted to simplify both coding and clock/data recovery circuitry. Differently from [28] and thanks to the symmetry, half duplex data rates at tens of megabit/s in both directions can be achieved. However, communication from chip A to B in this design was targeted to low data rate for configuration purposes (i.e., up to 5 Mb/s), thus saving power consumption. Both envelope signals are available for detection at the transformer windings, i.e. at the primary and secondary windings for the LS and HS data stream, respectively. Therefore, the LS detector was directly connected at primary winding of $T_D$ ($V_{P1}$, $V_{P2}$). A different solution was instead adopted for the main data communication (i.e., the HS data communication) with the aim of improving the robustness against CMTs, which otherwise would be quite poor using a direct connection to the secondary winding of $T_D$. Actually, a high CMTI is mandatory for the main data stream to reduce bit error rate degradation due to dynamic ground shifts between chip A and chip B, which are typically in the order of several tens of kV/μs and appear as a common mode voltage disturbance, $V_{CM}$, at the transformer windings. To this purpose, the HS ASK detector, was connected at the output ($V_{D1}$, $V_{D2}$) of the CMT rejection circuit in Fig. 2.8. This circuit has to cope with very rapid ground shifts that inject a common mode current, $I_{CM}$, due to parasitic capacitances ($C_{AB}$) between the windings of $T_D$. This current can produce dangerous overvoltage and/or demodulation errors. Current $I_{CM}$ has a strong dc component, which is proportional to both $C_{AB}$ and

the maximum slope, $dV_{CM}/dt$, of the CMT. Moreover, it also contains significant high frequency harmonics. State-of-the-art approaches based on a

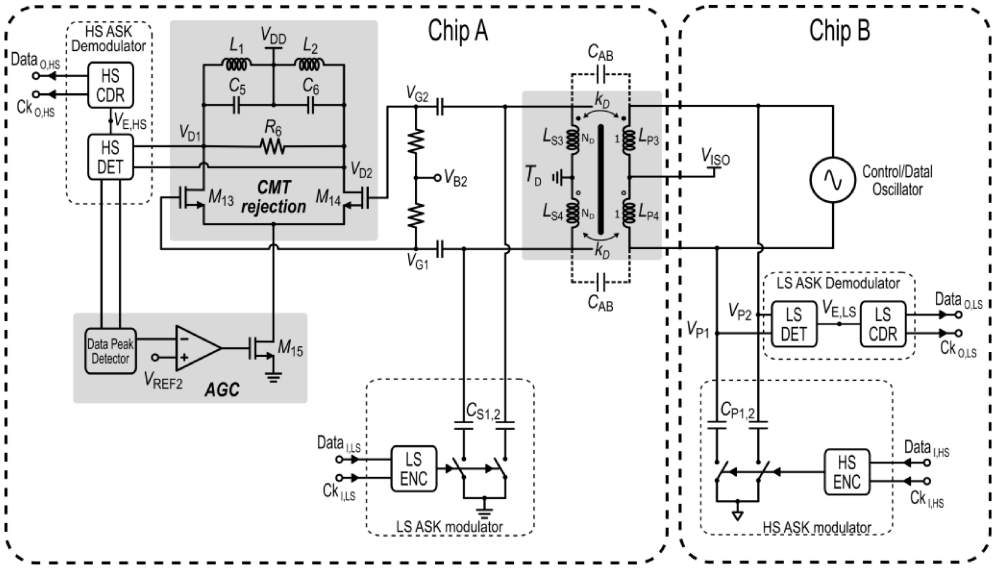



Fig. 2.8. Data link simplified schematics.

common mode feedback circuitry [57]-[58] are not very effective when high coupling integrated transformers are used. Indeed, due to the limited bandwidth of the common mode feedback amplifiers, they are not compliant with high CMTI performance in the presence of significant parasitic capacitances. The alternative approach exploiting a multi resonant passive filtering network with high-$Q$ on board isolation devices [59] could guarantee CMTI performance up to 150 kV/µs, as demonstrated in [60], but it is not suited for integrated dc-dc converters due to the low quality of inductive components. In this work, a CMT rejection circuit was adopted as shown in Fig. 2.8 [61], which provides a low impedance path for dc and low frequency components of $I_{CM}$, by connecting to ground or power supply the center taps of the isolation transformer, $T_D$. Moreover, it performs an active filtering to

greatly attenuate high-frequency components of $I_{CM}$. This is achieved with an *LC* differential amplifier, which rejects the residual high frequency common-mode spurious thanks to high-*Q* common mode *LC* load resonators, while preserving the envelope frequency content of the differential signal thanks to differential resistor $R_6$ that properly enlarges the differential signal bandwidth. This arrangement only performs very selective common mode filtering, but it does not affect data communication (i.e., the differential signal). Differently from [59]-[60], this approach guarantees constant CMTI performance at increasing data rate. The automatic gain control in the CMT rejection circuit provides constant envelope signal to be delivered to the HS DET, regardless of the variation of the carrier peak level imposed by the power control. Both resistance $R_6$ and AGC loop were set to comply with the *PVT* variations of the oscillation frequency (i.e., 900 MHz ± 9%). Fig. 2.9 shows simulated single ended signals of the HS data link at 25 Mb/s in presence of a 25 kV/μs CMT. The ASK modulated signal at the secondary winding of transformer $T_D$ (i.e., $V_{G1,2}$) is affected by a common mode disturbance, which is not compatible with an accurate demodulation. As apparent in Fig. 2.9, this disturbance is removed at the output of the CMT rejection circuitry. For the sake of completeness, Fig. 2.10 and Fig. 2.11 show the schematics of the HS and LS ASK detectors. They both exploit a high-gain common-source topology with adaptive biasing [62]-[64]. Each detector provides the envelope signal, $V_{O,HS}$ or $V_{O,LS}$, and its average value, $V_{AV,HS}$ or $V_{AV,LS}$, respectively, to a comparator, which delivers a rail–to–rail signal to the clock and data recovery digital blocks. Each detector topology was customized to the data rate specifications to reduce current consumption. The input pair of the HS detector, $M_{16,17}$, provides an RF rectified current at

its output, which is modulated by an amplified envelope signal. This current flows into the Sallen&Key filter composed of $Q_1$, $R_{7,9}$ and $C_{7,8}$, which

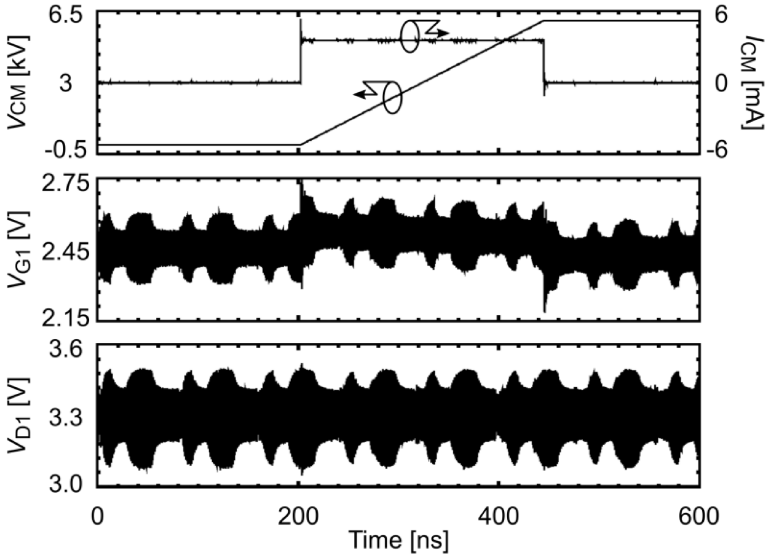



Fig. 2.9. Simulation of HS data link in presence of 25-kV/μs CMT.

provides the envelope signal, $V_{O,HS}$, around an average component, $V_{AV,HS}$, but with greatly reduced RF harmonics. A replica path comprising $Q_2$ and $R_8$, along with a high filtering capacitance, $C_9$, is used to extract $V_{AV,HS}$. Voltages $V_{O,HS}$ and $V_{AV,HS}$ are then compared by the HS comparator to achieve a rail-to-rail envelope signal, $V_{E,HS}$. The average signal at the base of $Q_2$ feeds the error amplifier whose output sets the bias voltage, $V_{B3}$, of the input pair. The HS detector and error amplifier form a control loop that sets the voltage across $R_9$ to the reference voltage, $V_{REF3}$, and hence the average current in $M_{16,17}$ is well controlled, thus guaranteeing robustness to *PVT* variations. The detector was designed for data communication up to 50 Mb/s. Its current

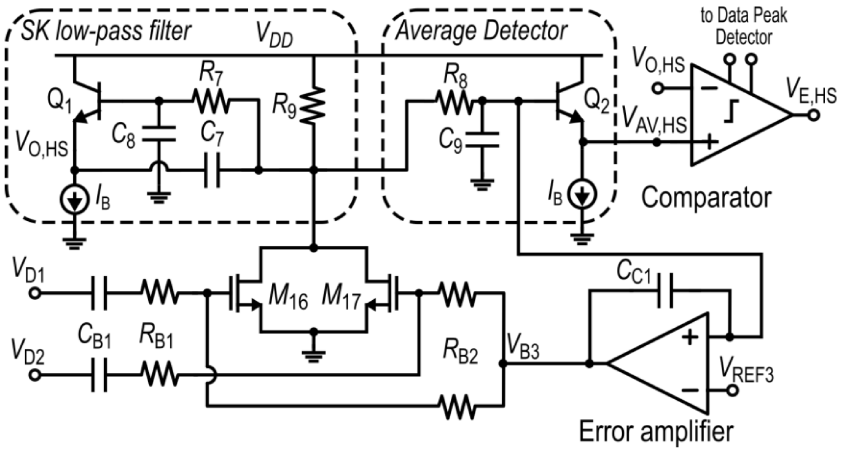



Fig. 2.10. HS detector schematic.

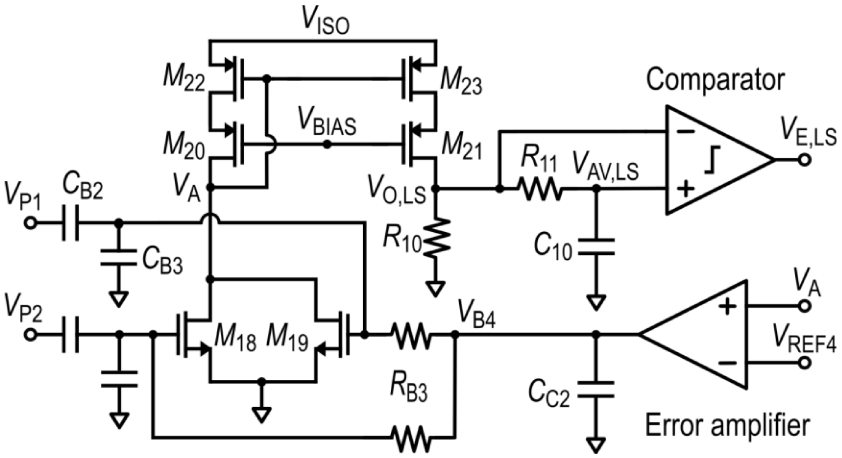



Fig. 2.11. LS detector schematic.

consumption is about 400 μA. The input pair of the LS detector, $M_{18,19}$, is ac-coupled to the primary winding of the control/data isolation transformer, $V_{P1,2}$. Low-voltage cascode current mirror $M_{20\text{-}23}$ delivers the output current of $M_{18,19}$ to load resistance $R_{10}$ and produces output voltage $V_{O,LS}$. Due to both low bit rate and current mirror/load frequency limitations no further filtering

is required for the RF harmonics. A low-pass filter made up of $R_{11}$ and $C_{10}$ recovers the envelope average voltage, $V_{AV,LS}$. The feedback signal, $V_A$, for the error amplifier was taken at the drains of $M_{18,19}$ to bypass time constant $R_{11}$-$C_{10}$ and make possible dominant pole compensation. The current consumption of the LS detector is about 30 μA to achieve bit rates up to 5 Mb/s.

### 2.4.3. Control/Data Isolation Transformer

Transformer $T_D$ guarantees galvanic isolation for the control/data link. Its simplified structure is shown in Fig. 2.12, while the geometrical parameters are reported in Table 2.4.

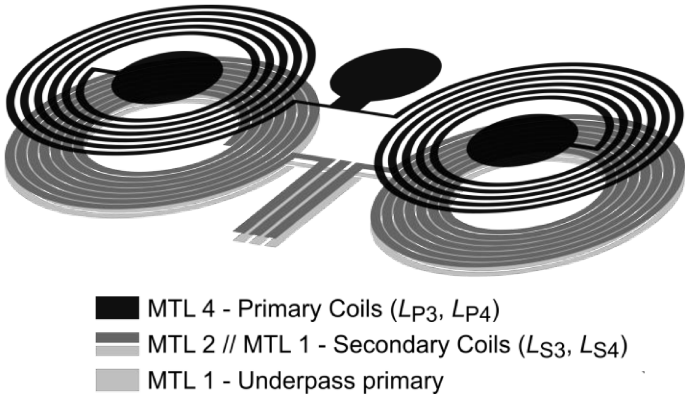



Fig. 2.12. Structure of control/data transformer $T_D$.

It adopts the same vertical structure of the power isolation transformer, $T_P$, thus achieving the same isolation rating of 6 kV. However, since the control/data oscillator was included in chip B, primary and secondary windings were built in metal 4 and metal 2/metal 1, respectively, and the center tap of the primary winding was used for the oscillator power

TABLE 2.4
GEOMETRICAL PARAMETERS OF THE CONTROL/DATA TRANSFORMER.

| **Parameters** | **Primary Coil (half structure)** | **Secondary Coil (half structure)** |
|---|---|---|
| Number of turns ($n$) | 5.5 | 7 |
| Width ($w$) [µm] | 7.4 | 9.2 |
| Spacing ($s$) [µm] | 4.7 | 1 |
| Internal diameter ($d_{IN}$) [µm] | 148 | 136 |
| Outer diameter ($d_{OUT}$) | 285 | 285 |

supply (i.e., $V_{ISO}$) through a bonding wire connection. Moreover, an *S*-shape coil connection was exploited to improve the *EMI* of the data link, which is important to avoid *BER* degradation due to external magnetic fields. Thanks to this spiral configuration, the current flowing in the primary winding has a clockwise direction in one coil, and a counter clock wise direction in the other one. The same happens for the current that flows in the secondary winding. Therefore, the magnetic flux linked to the coils produces the sum of in-phase induced voltages. On the contrary, an external magnetic interference would produce a flux in the same direction in both windings and thus out of phase induced voltages would be produced.

Transformer parameters were chosen to trade-off contrasting design issues such as maximization of winding inductances and quality factors for lower current consumption and minimization of transformer area to reduce parasitic capacitance $C_{AB}$ that determines the CMT currents. Finally, the magnetic coupling factor, $k_D$, was maximized by using the same external diameter, $d_{OUT}$, for both primary and secondary windings.

## 2.5. Experimental Results

Fig. 2.13 and Fig. 2.14 show the chip micrographs of the dc-dc converter with main blocks labelled. The die sizes are 3.7 mm × 1.8 mm and 2.2 mm × 1.1 mm for chip A and chip B, respectively.

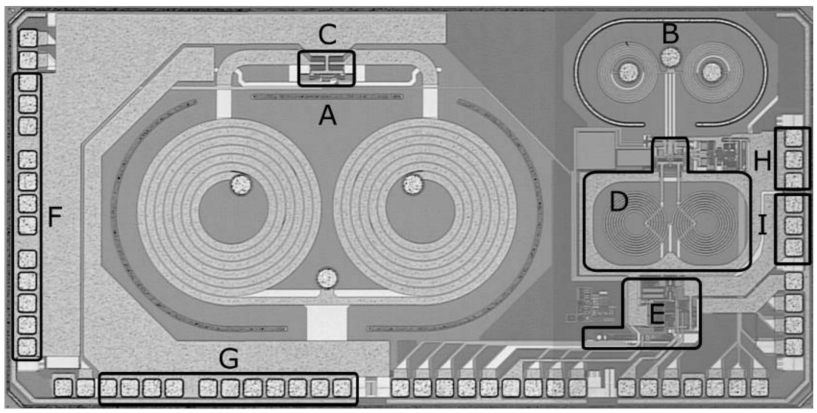



Fig. 2.13. Micrograph of the dc-dc converter (Chip A).

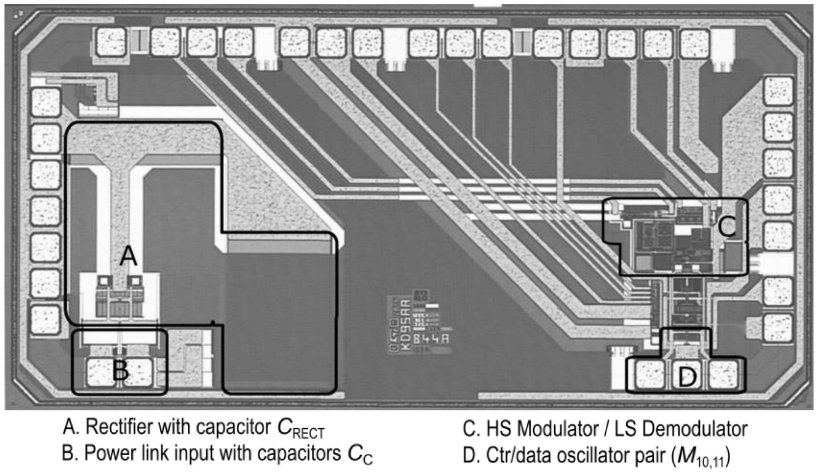



Fig. 2.14. Micrograph of the dc-dc converter (Chip B).

Chip A includes the galvanic barriers for both power and control/data links performed by the integrated transformers (A and B). It also houses the power oscillator (C) that is connected to ground and power supply by means of large Cu metals and multiple bonding wires (F and G) to reduce power efficiency degradation due to resistive/inductive parasitics. The cross-talk between the power and control/data links, taking place on chip and via bonding wires, is minimized by a proper floorplan. Indeed, the power link blocks are placed on the left-hand side, while the control/data section is developed on the

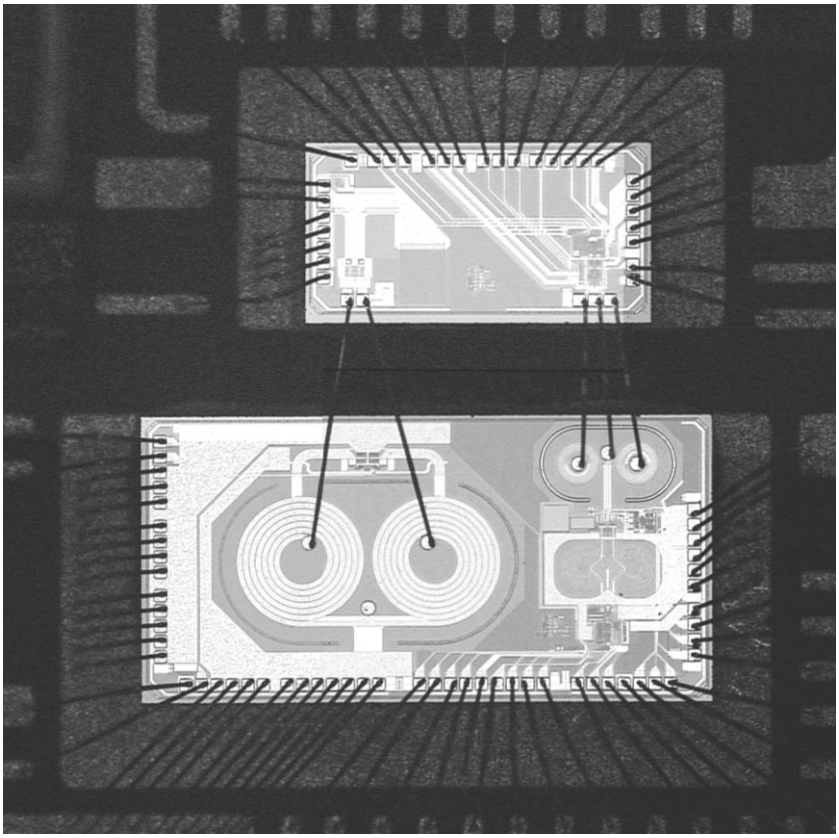


Fig. 2.15. Micrograph of the dc-dc converter assembled on board.

right-hand side. Moreover, separated on chip supply and ground planes are adopted (F, G, H, and I). Finally, power and control/data chip to chip connections are properly spaced to reduce the magnetic coupling between bonding wires. Chip B houses the ac coupled power rectifier (A and B) and the control/data link oscillator (D) on the left and right-hand sides, respectively. The HS modulator/LS demodulator blocks are placed close to the control/data oscillator. The dc-dc converter was assembled on board for characterization, as shown in Fig. 2.15. Measurements were performed at 3.3-V power supply.

Fig. 2.16 summarizes the performance of the dc-dc converter in terms of power conversion efficiency, $\eta_{DC\text{-}DC}$, as a function of the output power, $P_{ISO}$, for different values of the isolated output voltage, $V_{ISO}$. Efficiency $\eta_{DC\text{-}DC}$ is higher than 15% at low values of $P_{ISO}$. It remains quite constant in a large range of power values. Thanks to the voltage/power control loop, the dc-dc converter performance is guaranteed at different $V_{ISO}$ with variations of $\eta_{DC\text{-}DC}$ by less than three percentage points for maximum power. The converter is able to deliver up to 93 mW at 3.3-V output voltage with a $\eta_{DC\text{-}DC}$ of about 19%. Measurements of the power link with external PWM control signal confirmed that the control/data link affects the overall dc-dc converter efficiency by only one percentage point.

Fig. 2.17 shows the transient response of the output voltage $V_{ISO}$ to a step from 2 V to 3.1 V of the reference voltage, $V_{REF,OUT}$, which corresponds to a variation of $P_{ISO}$ from 36 mW to 87 mW on a load resistance of about 110 Ω. Two values of the output capacitance, $C_L$, have been used to verify the trade-off between speed and output ripple.

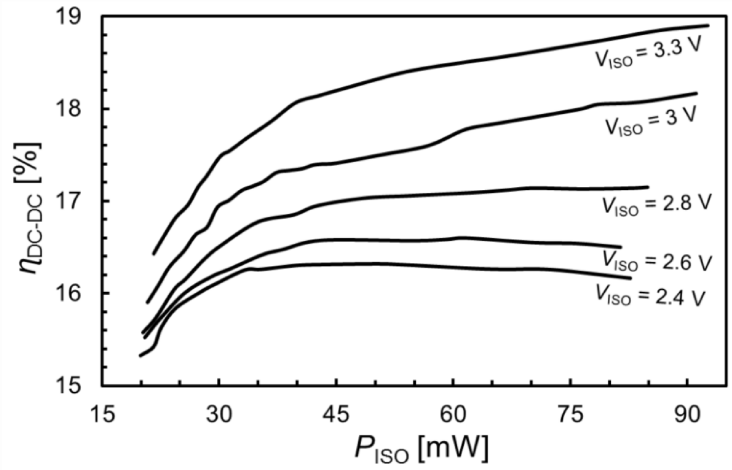



Fig. 2.16. Power efficiency, $\eta_{DC-DC}$, as a function of the dc output power, $P_{ISO}$ at different values of the isolated output voltage, $V_{ISO}$.

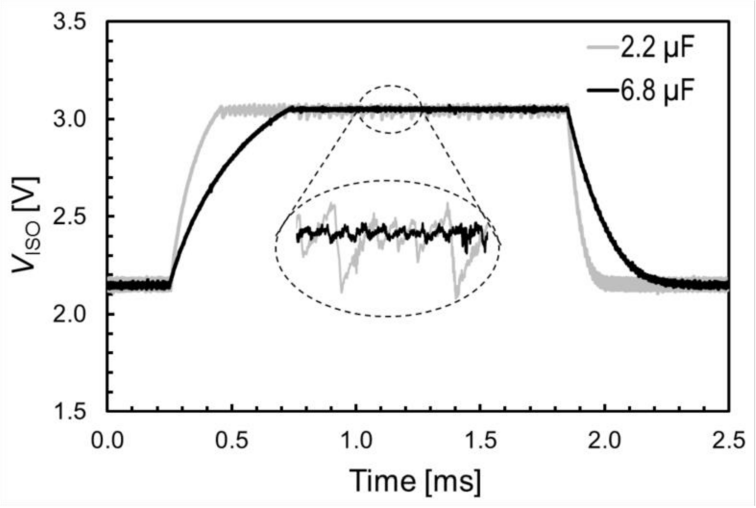



Fig. 2.17. $V_{ISO}$ transient response with two values of $C_L$ ($R_L$=110 Ω).

Fig. 2.18 shows the start-up transient of output voltage $V_{ISO}$ using a 6.8 µF output capacitance. $V_{REF,OUT}$ of 3.1 V and $R_L$ of 120 Ω were imposed, which set the steady-state output power to 75 mW and the duty cycle of the PWM

control signal to 83%. After a delay of about 2 ms, $V_{ISO}$ reaches 90% of the steady state value in 0.75 ms.

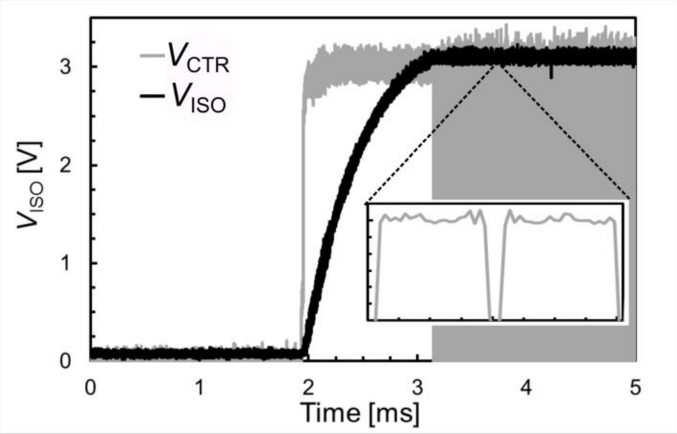



Fig. 2.18. $V_{ISO}$ start-up transient and corresponding PWM control signal $V_{CTR}$ ($V_{REF,OUT}$ = 3.1 V, $f_{PWM}$ = 100 kHz, $C_L$ = 6.8 µF, $P_{ISO}$ = 75 mW).

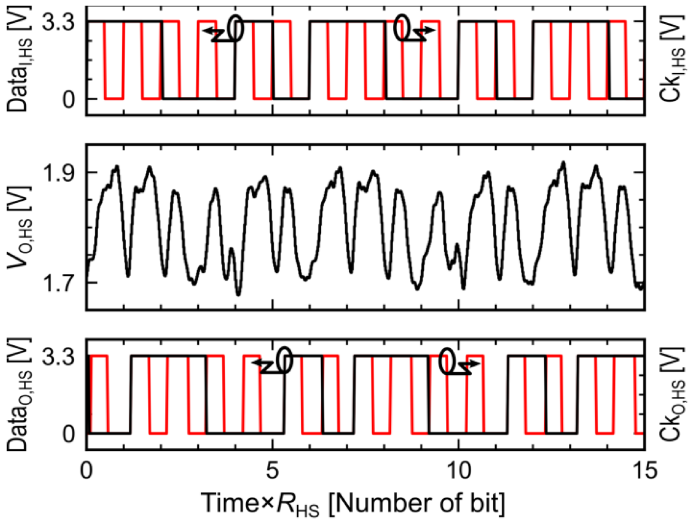



Fig. 2.19. HS data link at maximum data rate ($R_{HS}$ = 50 Mbps, $V_{ISO}$ = 3.3 V).

Fig. 2.19 depicts the measured waveforms of the HS link for a 50 Mb/s PWM coded ASK signal at $V_{ISO}$ of 3.3 V. Signal $V_{O,HS}$ of the envelope

detector before the limiting comparator (see Fig. 2.10) is about 200 $mV_{PP}$. Clock/data signals, $Ck_{O,HS}/Data_{O,HS}$, at the HS CDR circuit are correctly demodulated. A *BER* better than $10^{-4}$ was measured for bit rates up to 50 Mbit/s. The LS data link was also measured with data rates up to 5 Mb/s. The performance of the dc-dc converter is summarized and compared with the state of the art in Table 2.5.

TABLE 2.5
SUMMARIZED PERFORMANCE AND COMPARISON WITH THE STATE OF THE ART

| **Parameters** | **[40]** | **[28]** | **This Work** |
|---|---|---|---|
| $V_{DD}$ [V] | 3.3 | 3 | 3.3 |
| $V_{ISO}$ [V] | 3.3 | 2 (1) | 3.3 |
| $P_{ISO,max}$ w/o data [mW] | 9.1 / 10 | 20.4 / 23.7 | 93 / 107 |
| $\eta_{DC\text{-}DC}$ w/o data [%] | 22 / 24 | 9 / 11 | 19 / 20 |
| $f_P$ [MHz] | 200 | 330 | 350 |
| Control scheme / frequency [kHz] | Bang-bang / 1700 | n.a. (1) | PWM / 100 |
| No. of data channels | 2 (3) | 2 (4) | 2 (4) |
| Max data rate [Mb/s] | 6.8 (x 2) | 40 / 3 | 50 / 5 |
| Isolation [kV] | 5 (5) | 5 | 6 |
| CMTI [kV/μs] | n.a. | n.a. | 50 (6) |
| Silicon technology | 0.25-μm CMOS, 0.35-μm DMOS, Schottky diode | 0.35-μm BCD | |
| Isolation technology | Post–processed transformer | On-chip Transformer | |
| No. of transformers | 1 power, 2 data/ctrl | 1 | 1 power, 1 data/ctrl |
| No. of die | 6 | 2 | 2 |

(1) Output voltage is not controlled (2) pulse modulation
(3) n. 3 (multiplexed) data channels + n.1 configuration/clock channel
(4) half-duplex (5) rms (6) Simulated value

# Chapter 3.

# Galvanically isolated dc-dc converter exploiting a single isolated link

## 3.1. Introduction

This chapter deals with the design of a novel architecture for power transfer systems with galvanic isolation which performs power functionalities by using a single isolated link, as shown in Fig. 3.1. Only one isolated link is used to transfer both power and control signal, while on/off control scheme is adopted to regulate the output power at maximum efficiency regardless the load. The main challenge of the dc-dc converter with a single isolated link is performing the feedback of control signal from chip B (i.e., load side) to

chip A (i.e., power oscillator side) on the same channel used for power transfer.

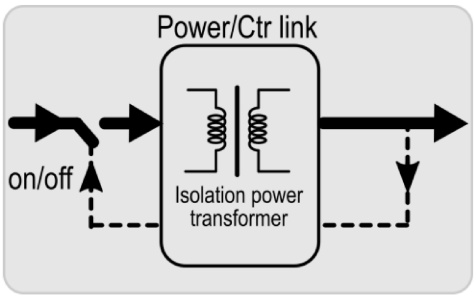



Fig. 3.1. Architecture of a galvanically isolated dc-dc converter using a single isolated link

The power regulation technique proposed in chapter 2 is based on relating the control signal on the peak of the oscillation voltage of the control/data oscillator which performs the feedback. This approach is not compliant with a single link solution since the only available oscillation voltage is the power signal whose peak value depends on the power oscillator in chip A. Following these considerations, a novel power regulation technique has been conceived and the simplified block diagram of the proposed system is shown in Fig. 3.2. The dc output power, $P_{ISO}$, is detected by monitoring the output isolated voltage, $V_{ISO}$, for a fixed load, $R_L$. An error amplifier compares $V_{ISO}$ with a reference, *REF*, and produces the error signal $\varepsilon$ (i.e., the control signal) that is converted into a bitstream by an analog-to-digital converter. This bitstream is sampled and transmitted by means of ASK modulation of the power signal at the secondary winding, similarly to data transmission from chip B to chip A in [28]. Finally, the received bitstream on the power oscillator side is converted into an analog signal or is used as on/off control signal to regulate the output power by a power control circuit. Differently from [44] that exploits an analog approach, in the proposed system the control

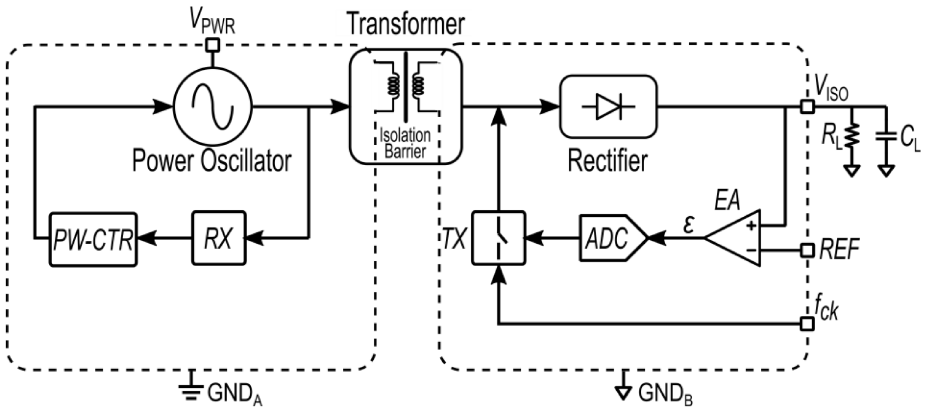



Fig. 3.2. Basic principle to feedback the control signal on the same channel of power signal.

signal is digitally transferred across the galvanic barrier by modulating the power signal with a modulation index lower than 5%, thus preserving the overall system efficiency.

The proposed architecture is technology-independent from the point of view of the isolation component (i.e., the isolation transformer) since it does not affect the functionalities of the overall system but defines the performance in terms of power efficiency and isolation rating. Therefore, this solution is suitable with either two or three chips implementation. Indeed, the isolation transformer (i.e., the unique isolated link) can be manufactured either on a stand-alone chip, by using a dedicated process steps, or on the same chip of the power oscillator, exploiting an integrated approach as the one described in Chapter 2.

The proposed dc-dc converter delivers a regulated output power up to 150 mW with a power efficiency of 23%, thus making the proposed system very suitable to gate driver applications. The chapter is organized as follows. Section 3.2 deals with system description and technology. The

power/ctr link is presented in Sections 3.3, while simulation results are shown in Section 3.4.

## 3.2. System Description

The simplified block diagram of the proposed system is depicted in Fig. 3.3. The converter is based on a patented architecture [45], which consists of a single isolated link used both for highly efficient power transfer and control signal feedback loop. The dc output voltage, $V_{ISO}$, is delivered to the external load, $R_L$-$C_L$, across the galvanic barrier thanks to a power-ctrl link, which is made up of a power oscillator operated at 350 MHz, an isolation transformer, $T$, and a power rectifier. Output voltage $V_{ISO}$ is regulated at the value of 18 V by means of a PWM control scheme which guarantees maximum efficiency regardless of the power level to be achieved. Specifically, $V_{ISO}$ is compared with a reference voltage, $V_{REF,OUT}$, thus producing an error signal, ε, that changes according to the output power imposed by $V_{REF,OUT}$ and load resistance $R_L$. The PWM block, which works as an 1-bit ADC, converts ε into a square wave voltage, $V_{CTR,B}$, whose duty cycle, $DC_{(VCTR,B)}$, depends on the dc value of ε, while the frequency is set according to an external reference clock, $f_{CK}$, properly divided by an N factor. The reference clock, $f_{CK}$, is also used as master clock for the transmitter to sample and transmit $V_{CTR,B}$ across the galvanic barrier by means of amplitude modulation of the power oscillation signal. The receiver on the oscillator side, recovers both data, $V^*_{CTR,B}$, and clock, $f^*_{CK}$, signals which drive the PW-CTR block to turn on and off the power oscillator. The PW-CTR block is based on a phase-locked loop which exploits a sample and hold operation on the recovered clock

signal, $f^*_{CK}$, thus avoiding an external reference clock for the PWM control signal that drives the power oscillator, $V_{CTR,A}$. During the on-phase of the power oscillator, the PLL is operated in a closed-loop mode

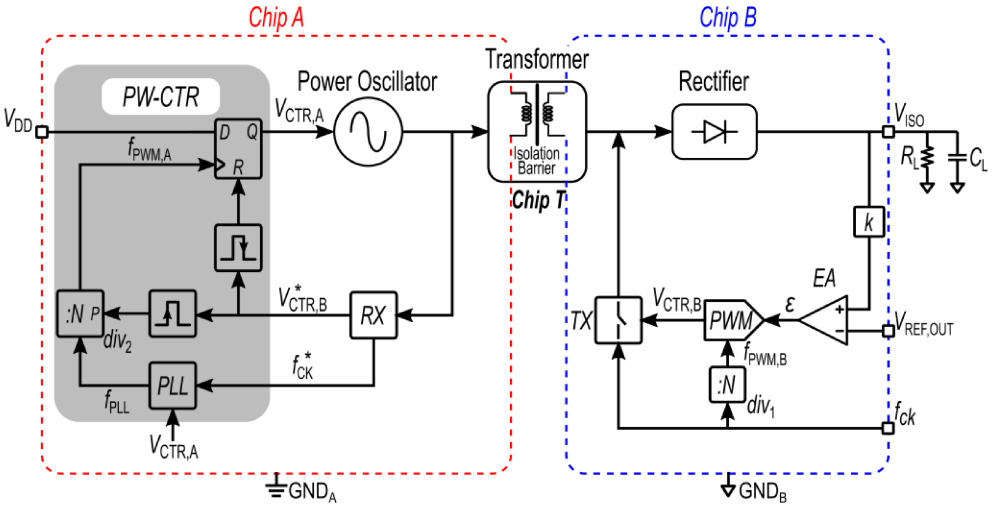



Fig. 3.3. Simplified block diagram of the dc-dc converter exploiting a single isolated link.

and captures $f^*_{CK}$, while, during the off-phase of the power oscillator, the PLL holds the reference clock by switching in an open-loop condition, thus ensuring the availability of the reference clock even when the power oscillator is turned off. Then, the locked signal, $f_{PLL}$, is properly divided by an N factor, thus providing the reference clock, $f_{PWM,A}$, to the positive edge-triggered D-flip flop which turns on and off the power oscillator according to the rising edge of $f_{PWM,A}$ and the falling edge of $V^*_{CTR,B}$, respectively. Note that the control signal $V_{CTR,A}$ is equal to $V_{CTR,B}$ since they have both the same frequency and duty cycle. Indeed, their frequency is set by $f_{PWM,A}$ and $f_{PWM,B}$, which are the same (i.e., $f_{PWM,A} = f_{PWM,B} = f_{CK}/N$), while the rising and falling edges of $V^*_{CTR,B}$ performs the synchronization of the edges between $V_{CTR,A}$ and $V_{CTR,B}$. Therefore, the duty cycle of $V_{CTR,A}$ is directly related to the error

signal ε, thus allowing the on/off output power regulation. The frequency $f_{PWM,A}$, of control signal $V_{CTR,A}$ is the switching frequency of the power oscillator and can be set up to few hundreds of kilohertz. Thanks to this architecture, which takes advantage of a digital transmission of the control signal, the feedback loop can be achieved on the same isolated channel generally dedicated for power transfer. Although the feedback loop performs a data communication, no CMT rejection circuit is required since the loss of control bits does not affect the power regulation whose time constant is much higher than the period of a single control bit. Moreover, the sample and hold operation on the recovered reference clock allows the on/off control mode of the isolated output power without an additional external reference clock. This guarantees high matching of frequency between $V_{CTR,A}$ and $V_{CTR,B}$ that is essential to proper operation of the feedback loop.

The system was fabricated taking advantage of three different technologies. The isolation transformer was implemented in post-processed technology, as described in chapter 1, while 0.18 µm BCD and 0.13 µm CMOS processes are used for the power oscillator chip and rectifier chip, respectively. Differently from the previous galvanically isolated system (i.e., power-data-control system exploiting two isolated links described in chapter 2), this novel architecture exploits three chips implementation, thus leading to a customized design for each building blocks with the aim of maximizing the efficiency performance. Indeed, the post-processed technology allows the *ad-hoc* design of the isolation transformer (i.e., Chip T) providing low resistivity metal layers for the primary and secondary windings. The 0.18 µm BCD technology features Double Diffused Metal Oxide Semiconductor process for power and high-voltage elements, thus

ensuring high power design of the power oscillator (i.e., Chip A). Finally, the 0.13 μm standard CMOS process provides high-voltage Schottky diodes with sub-GHz operation capability, that achieve high efficiency for power rectifier (i.e., Chip B) thanks to low threshold voltage and high switching activity.

## 3.3. Power-Ctr Link

This Section focuses on the power-ctrl link with a detailed description of the transistor-level design for the main building blocks. The power-ctr link is the core of the dc-dc converter since it determines both power functionalities and efficiency performance of the overall system. It was designed to deliver a dc output power, $P_{ISO}$, higher than 100 mW at a nominal output voltage, $V_{ISO}$, of 18 V with a 5-V power supply, $V_{PWR}$. The output power is regulated by means of a PWM control scheme. The control signal for the output voltage and power regulation is related to the duty cycle of a square-wave signal which is sampled and transmitted across the galvanic barrier by properly modulating the power oscillation voltage. Therefore, both power and control links share the same isolation transformer, $T$, which is the resonant tank of the power oscillator. A description of the power link is reported in Section 3.3.1, whereas the control loop along with the stability analysis is described in Section 3.3.2.

### 3.3.1. Power Link

A simplified schematic of the power link is shown in Fig. 3.4. The architecture presents the fundamental scheme typically adopted for galvanic isolation and consists of a transformer-based power oscillator and a

full-bridge rectifier, which perform efficient dc-ac and ac-dc conversions, respectively. The power oscillator takes advantage of LDMOS transistors, $M_{1,2}$, which are the active core of the oscillator operating in D class [54]. Thanks to the oscillator topology and the high voltage/current capability of LDMOS transistors, a voltage oscillation amplitude, $V_{OSC,P}$, of about two

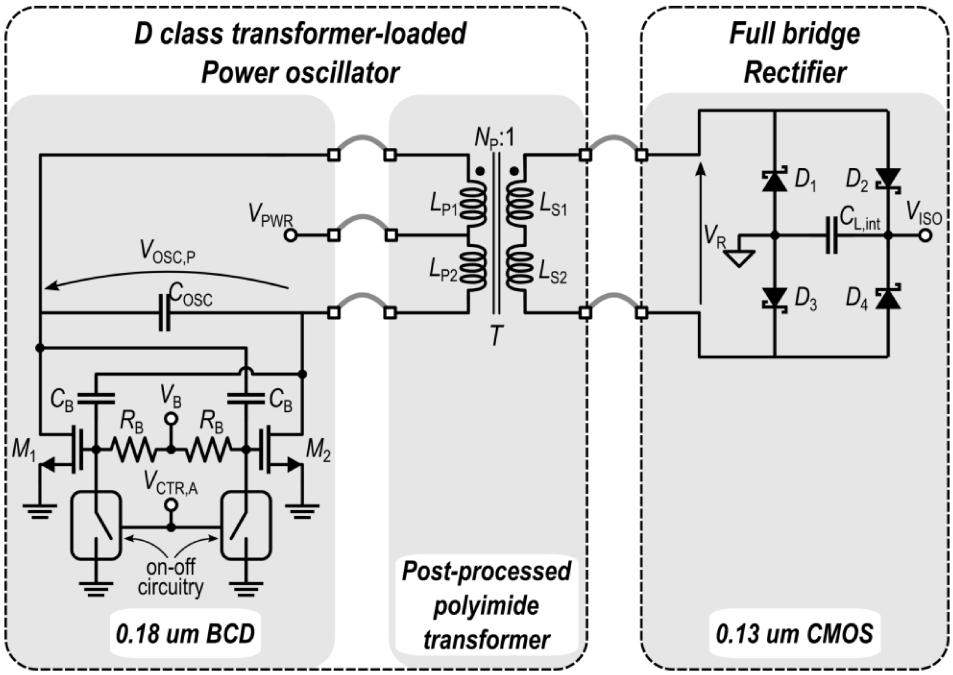



Fig. 3.4. Schematic of the power link.

times the supply voltage (i.e., about 10 V) is achieved, thus maximizing power efficiency. This oscillation voltage is properly reduced at the gate terminals of $M_{1,2}$ by means of capacitive partition between coupling capacitors $C_B$ and gate-source capacitances of $M_{1,2}$, thus preventing the gate-oxide breakdown. The gate terminals of $M_{1,2}$ are also connected to on-off switches which are driven by the PWM control signal $V_{CTR,A}$, thus allowing

the oscillator to be turned on and off for output power regulation purpose. The resonant tank of the oscillator includes the isolation transformer *T*, which is represented as magnetically coupled inductors. The geometrical structure of the transformer is shown in Fig. 3.5 and presents the same differential stacked configuration of the power transformer used in [44], but, differently from the latter, it was manufactured in a dedicated post-processed technology whose features have been detailed in chapter 1. Primary ($L_{P1,2}$) and secondary ($L_{S1,2}$) windings are built in thick Au metal to reduce resistive losses, while thick polyimide layer separates the two windings of the transformer thus performing galvanic isolation up to 10-kV. The geometrical parameters of half of the transformer coils are summarized in Table 3.1.

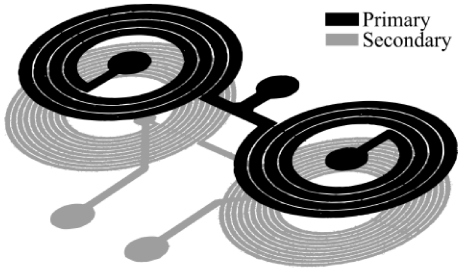



Fig. 3.5. Structure of the power isolation transformer.

TABLE 3.1
GEOMETRICAL PARAMETERS OF THE POWER-CTR TRANSFORMER.

| **Parameters** | **Primary Coil (half structure)** | **Secondary Coil (half structure)** |
|---|---|---|
| Number of turns ($n$) | 3.75 | 10 |
| Width ($w$) [μm] | 37 | 9.8 |
| Spacing ($s$) [μm] | 9.5 | 9.5 |
| Internal diameter ($d_{IN}$) [μm] | 300 | 300 |
| Outer diameter ($d_{OUT}$) | 676 | 686 |

For the sake of completeness, the design parameters of the overall power link are summarized in Table 3.2. The power link design was carried out using the approach described in [30], [65]. The first step is the definition of the rectifier size which depends on the output voltage and power level to be provided. The adopted full bridge rectifier is made up of Schottky diodes which consist of elementary cells with an active area of about 100 $\mu m^2$. The number of elementary cells, $M$, was chosen as a trade-off between power efficiency, $\eta_{RECT}$, and input capacitance of the rectifier that affects both rectifier bandwidth and power oscillator performance. Moreover, a trade-off is also required for the oscillation frequency since a higher oscillation frequency improves the $Q$-factor of the transformer but increases the power losses of the active switching components. Therefore, EM based co-design between the oscillator core and the transformer is mandatory to optimize the overall efficiency performance.

TABLE 3.2
DESIGN PARAMETERS OF THE POWER LINK.

| **Block** | **Parameter** | **Value** | **Unit** |
|---|---|---|---|
| Power oscillator active core | $W_{1,2}$ | 560 | [μm] |
| | $C_B$ | 1.5 | [pF] |
| | $C_{OSC}$ | 12 | [pF] |
| | $f_P$ | 350 | [MHz] |
| Isolation transformer, $T_P$ | $L_{P1,2}$ \| $L_{S1,2}$ | 16.7 \| 116.8 @ $f_P$ | [nH] |
| | $Q_{P1,2}$ \| $Q_{S1,2}$ | 11.6 \| 8.7 @ $f_P$ | |
| | $k_P$ | 0.74 | |
| Rectifier | $M$ | 20 | |

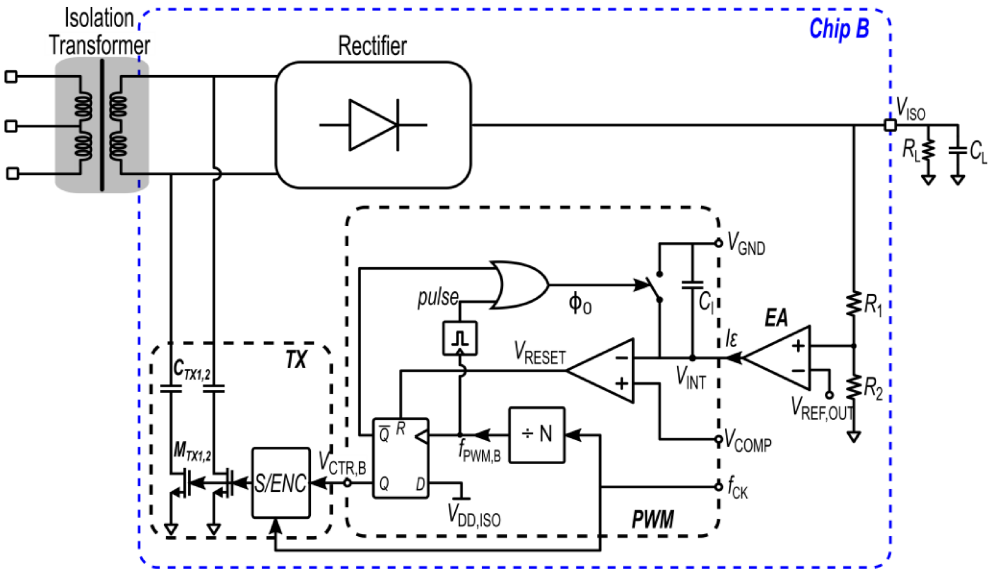
### 3.3.2. Control Link

A simplified schematic of the control loop is sketched in Fig. 3.6(a) and Fig. 3.6(b) which show Chip B and Chip A, respectively. Output voltage $V_{ISO}$ (see Fig. 3.6(a)) is reduced by the resistive partition, $R_1$ and $R_2$ (i.e., $k$ in Fig. 3.3), and then compared with the reference voltage, $V_{REF,OUT}$, by means of an error amplifier which is implemented by an operational transconductance amplifier. The output signal of the error amplifier drives the PWM block which provides a PWM signal, $V_{CTR,B}$, whose duty cycle is related to the error signal. The output current of $EA$, $I\varepsilon$, flows through the integration capacitor, $C_I$, thus providing a voltage ramp, $V_{INT}$, that is compared with the reference voltage, $V_{COMP}$. When this ramp goes up $V_{COMP}$, the comparator resets the output of the D Flip-Flop and the capacitor $C_I$ is discharged, thus restoring $V_{INT}$ to $V_{GND}$. The integration capacitor is also periodically restored through $\Phi_0$ either at the beginning of each period or when $V_{CTR,B}$ is low. For the sake of clarity, the steady-state operation of the PWM block is shown in Fig. 3.7, where a duty cycle of 60% was supposed. The expression of the duty cycle as function of $I\varepsilon$ is obtained by considering the charge phase of $C_I$ which is expressed in equation (3.1)

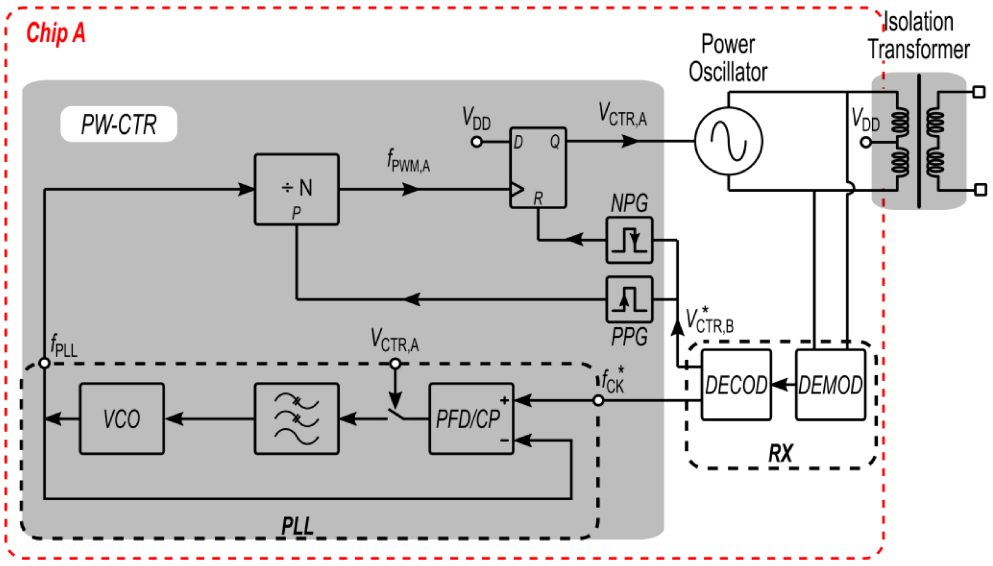
$$(V_{COMP} - V_{GND}) = \frac{I_\varepsilon}{C_I} t_C \tag{3.1}$$

where $t_c$ is the charge time of $C_I$ and corresponds to the on-phase of $V_{CTR,B}$, $t_{on}$. Therefore, the duty cycle, $DC$, is given by

$$DC = \frac{t_{on}}{T_{PWM,B}} = \frac{t_c}{N \cdot T_{ck}} = \frac{f_{ck}}{N} \times \frac{(V_{COMP} - V_{GND})}{I_\varepsilon} C_I \tag{3.2}$$




(a)




(b)

Fig. 3.6. Control link simplified schematics: (a) Chip A and (b) Chip B.

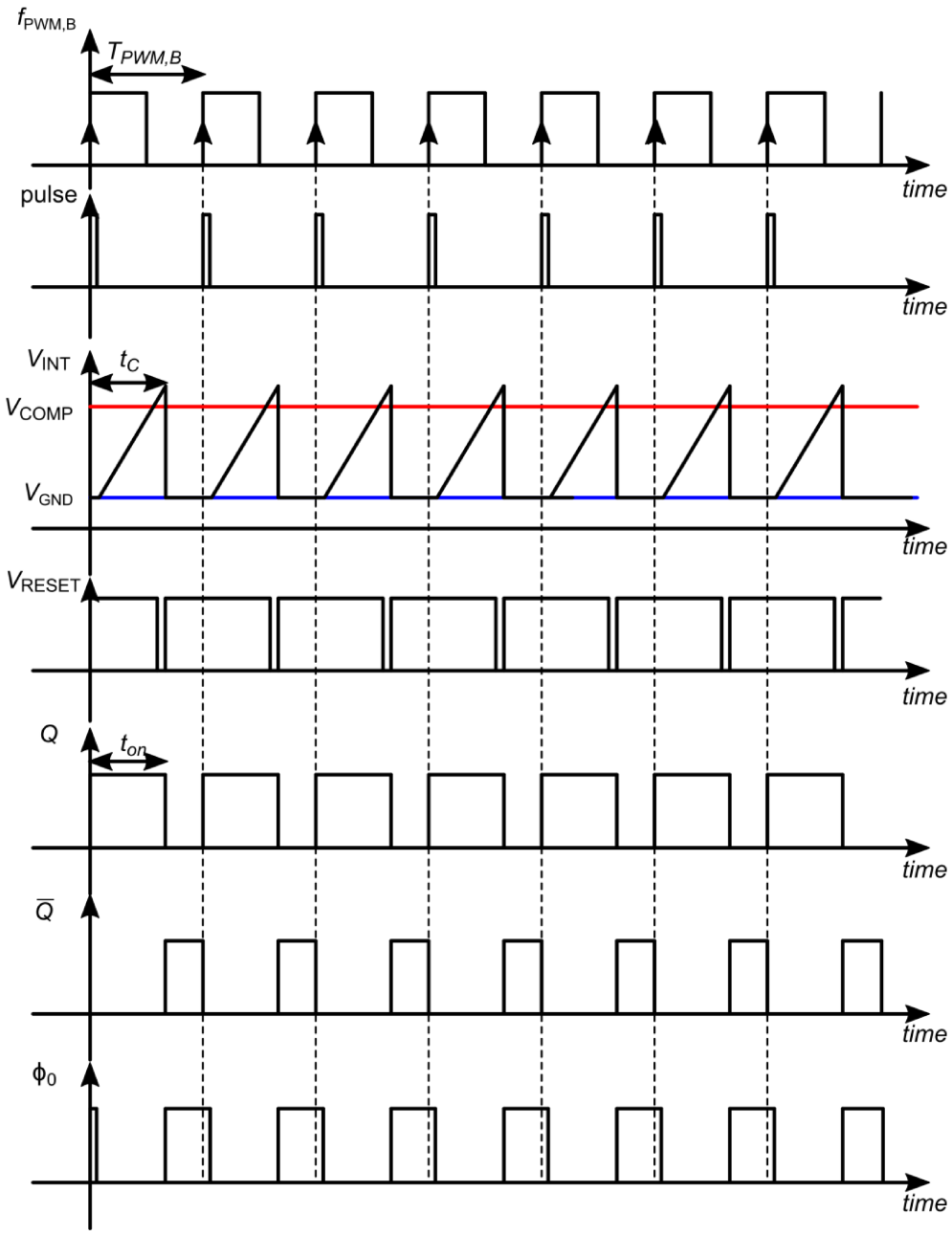



Fig. 3.7. Steady-state operation of the PWM block supposing a duty cycle of 60%.

The duty cycle is inversely proportional to the error current $I\varepsilon$ whose maximum value gives the minimum *DC*. The PWM signal $V_{CTR,B}$ is then transmitted through the galvanic barrier by means of a data communication from chip B to chip A which is performed exploiting an ASK modulation of the power oscillation voltage. To this purpose, capacitors $C_{TX1,2}$ and on/off switch resistances, which are implemented by MOS transistors $M_{TX1,2}$, are used as shown in Fig. 3.6(a). The control signal $V_{CTR,B}$ drives the sampler/encoder block which performs the sampling and encoding operation. PWM coding is adopted to simplify both coding and clock/data recovery circuitry. Moreover, PWM coding maximizes the efficiency of the overall system since the higher number of transmitted bits are bits 1. Indeed, the power oscillator is turned on during the on-phase of $V_{CTR,B}$, where only bits 1 are transmitted. This means that the oscillation voltage is maximum most of the on-time.

After the galvanic barrier (see Fig. 3.6(b)), a receiver block, which is made up of a demodulator and decoder, recovers both data and sampling clock during the on-phase of the power oscillator, while no data signals are available when the power oscillator is turned off. The recovered data and clock drive the power control block which allows the reconstruction of the control signal despite the loss of bits due to the shut-down of the oscillator. The PW-CTR block is made up of a PLL, which exploits an open-loop mode operation, a digital divider (÷N), a positive edge-triggered D flip-flop and two pulse generators, one on the positive edge (PPG), and the other one on the negative edge (NPG) of the input signal. The D Flip-Flop provides the PWM control signal $V_{CTR,A}$ to the power oscillator, thus switching on and off the power signal. Two conditions must be fulfilled to guarantee proper output

power regulation. The frequency and duty cycle of the control signal $V_{CTR,A}$ must be equal to the frequency and duty cycle of $V_{CTR,B}$. The frequency of $V_{CTR,A}$ is set by the reference clock $f_{PWM,A}$ which is achieved by means of digital division of the locked sampling clock, $f_{LL}$, thus satisfying the first condition (i.e., $f_{PWM,A} = f_{PLL}/N = f_{CK}/N = f_{PWM,B}$). On the other hand, the falling edge of the recovered data resets the D Flip-Flop thus bringing down $V_{CTR,A}$, which returns at high voltage level (i.e., at $V_{DD}$) when the rising edge of $f_{PWM,A}$ occurs. Therefore, the duty cycle of $V_{CTR,A}$ will be equal to the ones of $V_{CTR,B}$ only if both the rising edge of $f_{PWM,A}$ and $V^*_{CTR,B}$ are synchronized. For a better understanding, Fig. 3.8 shows the waveforms supposing no synchronization (Fig. 3.8(a)) and synchronization (Fig. 3.8(b)) between $f_{PWM,A}$ and $V^*_{CTR,B}$, thus highlighting the need of synchronization to preserve the duty cycle of $V_{CTR,A}$.

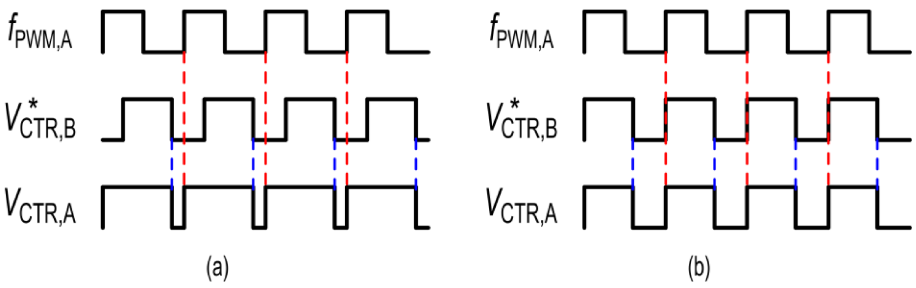



Fig. 3.8. Time domain waveforms for reference clock, $f_{PWM,A}$, recovered data, $V^*_{CTR,B}$ and control signal $V_{CTR,A}$ assuming: (a) no synchronization and (b) synchronization between $f_{PWM,A}$ and $V^*_{CTR,B}$.

The synchronization is achieved by pre-setting to $V_{DD}$ the outputs of the digital divider when a rising edge of $V^*_{CTR,B}$ is detected. Specifically, the digital divider is a simply N-bits down-counter whose operation starts when the rising edge of $V^*_{CTR,B}$ is noticed.

The PLL is the key circuit of the PW-CTR block since provides an accurate reference clock, $f_{PLL}$, for the control signal $V_{CTR,A}$. In such a condition, an additional external reference clock for the control signal $V_{CTR,A}$ cannot ensure the required high matching between $f_{PWM,A}$ and $f_{PWM,B}$ which is instead achieved thanks to the PLL operation. During the on-phase of the power oscillator, the PLL is operated in a closed-loop mode and locked to the recovered sampling clock. As soon as the falling edge of $V^*_{CTR,B}$ is detected, the control signal $V_{CTR,A}$ goes down turning off the power oscillator. Meanwhile, the PLL loop is opened by means of a switch placed between the charge pump and the filtering capacitors, thus freezing the control voltage, $V_{LP}$, of the voltage-controlled oscillator and, hence, its oscillation frequency, $f_{PLL}$. Then, the VCO output signal, $f_{PLL}$, is used to generate the reference clock for $V_{CTR,A}$, as widely discussed previously. The schematic of the phase-frequency detector/charge pump, PFD/CP, along with the low-pass filter is stacked in Fig. 3.9, while Fig. 3.10 shows the VCO topology.

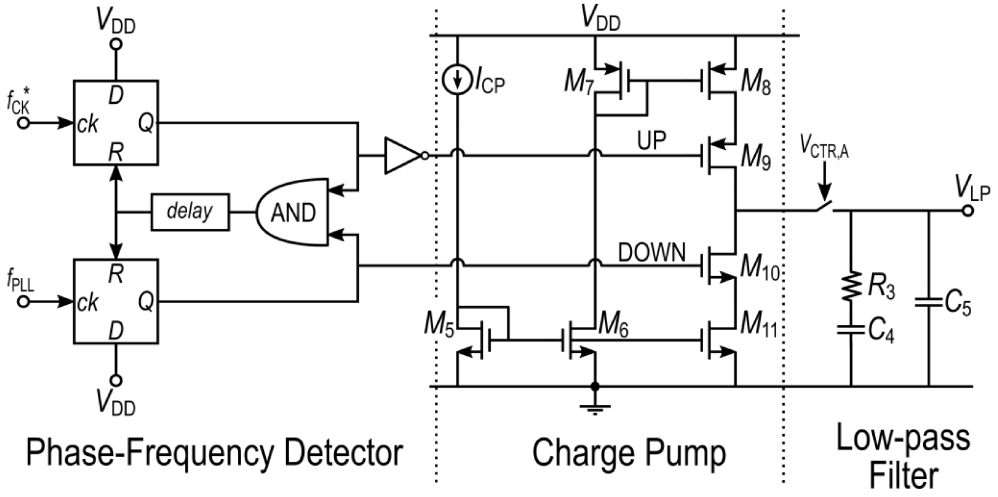



Fig. 3.9. Schematic of the PFD/CP along with the low-pass filter.

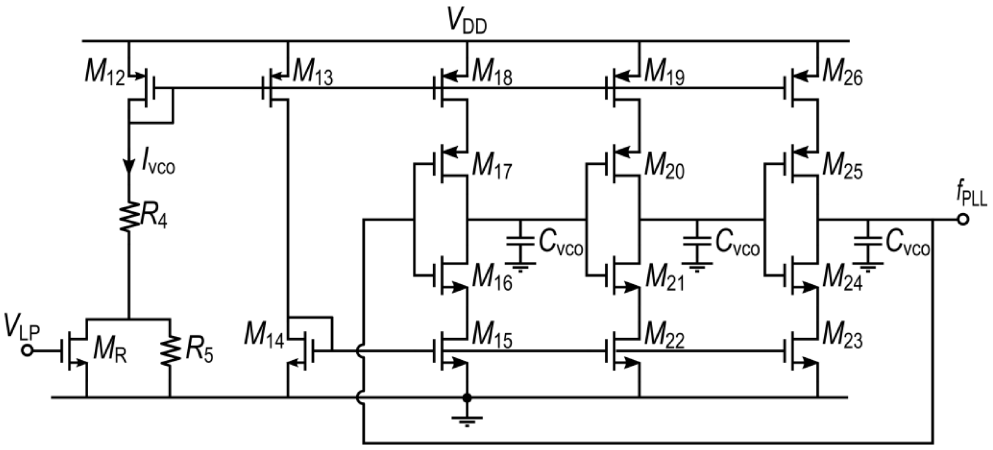



Fig. 3.10. Schematic of the VCO.

The PFD circuit is composed of two D flip-flops whose clock signals are the reference and feedback waveforms, $f^*_{CK}$ and $f_{PLL}$, respectively. The AND gate and the delay block ensure the proper operation of the PFD. The flip-flop outputs (i.e., UP and DOWN) drive the two MOS transistors $M_9$ and $M_{10}$ which implement the switches to enable the current generators of the charge pump. The output current of the PFD/CP block charges the second-order on-chip loop filter which is made up of resistor $R_3$ and capacitors $C_4$ and $C_5$. The switch placed between the charge pump and the filter is implemented by a transmission gate which exploits a complementary topology. The main constrain on the design of the switch is the minimization of the charge injected into the loop filter capacitors, which induces an instantaneous frequency shift of the reference clock $f_{PLL}$. The output voltage of the filter is the input or control signal of the VCO which is based on a ring oscillator topology (see Fig. 3.10). It consists of three inverting stages which are made up of a current controlled CMOS inverter along with a capacitor, $C_{VCO}$. Each stage provides a time-delay related to the voltage swing, $V_{SW}$, and the slew rate $I_{VCO}/C_{VCO}$,

where $I_{VCO}$ is the bias current of the VCO. The MOS transistor $M_R$, which is operating in triode-region, provides a variable resistance, $R_M$, as function of the filter output voltage $V_{LP}$ thus changing the bias current and hence the oscillation frequency of the VCO. Specifically, the expression of $f_{PLL}$ is reported in equation (3.3).

$$f_{PLL} = \frac{I_{VCO}}{2 \cdot 3 \cdot V_{SW} \cdot C_{VCO}} \tag{3.3}$$

The minimum and maximum oscillation frequency is set by the minimum and maximum value of the bias current $I_{VCO}$, respectively, which is expressed in equation (3.4)

$$I_{VCO} = \frac{V_{DD} - V_{SG12}}{R_4 + R_5 // R_M} \tag{3.4}$$

For the sake of completeness, the open transfer function, $T_{PLL}(s)$, of the PLL is reported in equation (3.5) and refers to the simplified schematic in Fig. 3.11

$$T_{PLL}(s) = \frac{k_C \cdot H(s) \cdot k_{VCO}}{s} \tag{3.5}$$

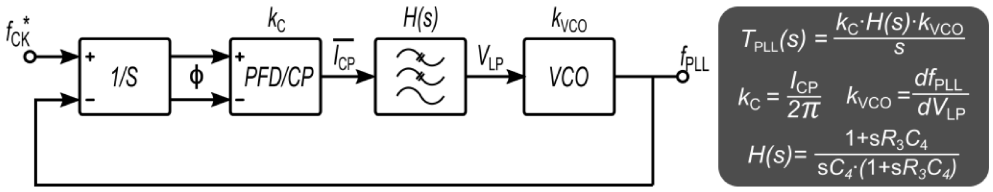



Fig. 3.11. PLL block diagram for the loop-gain evaluation.

The loop filter was sized to guarantee a phase margin around 60°, while no time settling requirements was targeted since the PLL operation affects only the start-up phase of the control loop which is dominated by the output load capacitance slew rate. The main design parameters of the PLL are reported in Table 3.3.

TABLE 3.3
DESIGN PARAMETERS OF THE PLL.

| Block | Parameter | Value | Unit |
|---|---|---|---|
| Charge pump, CP | Bias current, $I_{CP}$ | 1 | [µA] |
| Filter | $R_3$ | 295.2 | [kΩ] |
| | $C_4$ | 9.8 | [pF] |
| | $C_5$ | 0.7 | [pF] |
| Voltage controlled oscillator, VCO | $I_{VCO}$ @$V_{LP}$=$V_{DD}$/2 | 20 | [µA] |
| | $C_{VCO}$ | 300 | [fF] |
| | $R_4$ | 21.5 | [kΩ] |
| | $R_5$ | 77.5 | [kΩ] |
| | $W_{MR}$ | 0.28 | [µm] |
| | $L_{MR}$ | 0.4 | [µm] |

Finally, the loop stability analysis was carried out considering a single pole approximation for each block of the control loop. By referring to the simplified model in Fig. 3.12 , the open loop gain, $T_O$, can be written as

$$T_0 \cong k \cdot A_{EA} \cdot A_{CTR} \cdot A_{TX/RX} \cdot A_P \tag{3.6}$$

where $k$ is the resistive partition, $A_{EA}$ is the error amplifier gain and $A_{CTR}$, is the gain of the PWM block, which are the transfer factors from isolated output

voltage $V_{ISO}$ to the duty cycle of the PWM signal $V_{CTR,B}$ on chip B. Then, $V_{CTR,B}$ is sampled and transmitted across the galvanic barrier to chip A in which the control signal $V_{CTR,A}$ is achieved. These operations are performed by the transmitter, receiver, and power control, whose gains are embedded into the transfer factor $A_{TX/RX}$. Finally, $A_P$ is the gain of the power link.

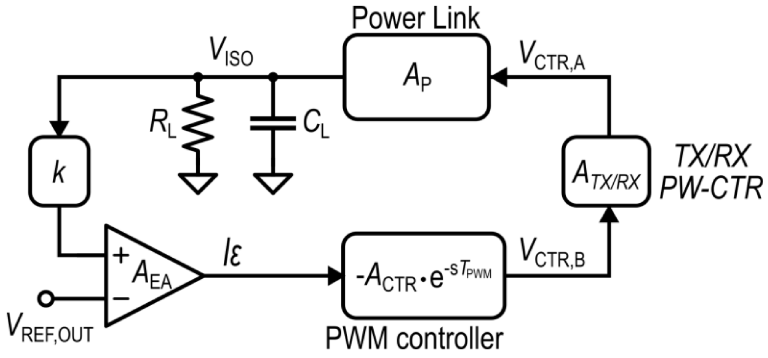



Fig. 3.12. Simplified model of the control link for stability analysis.

The expression of the gains which compose the control loop are reported from equation (3.7) to (3.10).

$$A_{EA} = \frac{dI_\varepsilon}{d(V_{ISO}/k)} = G_M \tag{3.7}$$

$$A_{CTR} = \frac{dDC_{(V_{CTR,B})}}{dI_\varepsilon} = -\frac{NDC^2_{(V_{CTR,B})}}{f_{ck}(V_{COMP} - V_{GND})C_I} \tag{3.8}$$

$$A_{TX/RX} = \frac{dDC_{(V_{CTR,A})}}{dDC_{(V_{CTR,B})}} \cong 1 \tag{3.9}$$

$$A_P = \frac{dV_{ISO}}{dDC_{(V_{CTR,B})}} = \frac{1}{2}\sqrt{\frac{R_L \cdot P_{ISO,max}}{DC_{(V_{CTR,A})}}} \tag{3.10}$$

being $G_M$ the transconductance of the error amplifier, $DC_{(VCTR,B)}$ and $DC_{(VCTR,A)}$ the duty cycle of $V_{CTR,B}$ and $V_{CTR,A}$, respectively, and $P_{ISO,max}$ the maximum power delivered to $R_L$, which can be considered constant in a first-order approximation.

An expression of the loop gain transfer function, $T(s)$, was evaluated by considering the two main low-frequency contributions, i.e. the pole of the power link at the output (i.e., $R_L$-$C_L$) and the delay introduced by the PWM block, which is the period of the PWM control signal (i.e. $T_{PWM}=N/f_{CK}$),

$$T(s) = T_O \frac{e^{-T_{PWM}s}}{1 + sR_LC_L} \tag{3.11}$$

In the worst case, a maximum 30-dB open loop gain $T_O$ was set. Therefore, a dominant pole compensation can be easily achieved increasing the load capacitance, $C_L$, whose value can be evaluated from

$$C_L = \frac{T_O \cdot T_{PWM}}{R_L \cdot \left(\frac{\pi}{2} - PM\right)} \tag{3.12}$$

where $PM$ is the required phase margin expressed in radians. As a result, to guarantee system stability with 50-kHz PMW control signal, a few-microfarads is required. Such values provide adequate performance in terms of both output voltage ripple and transient responses.

## 3.4. Simulation Results

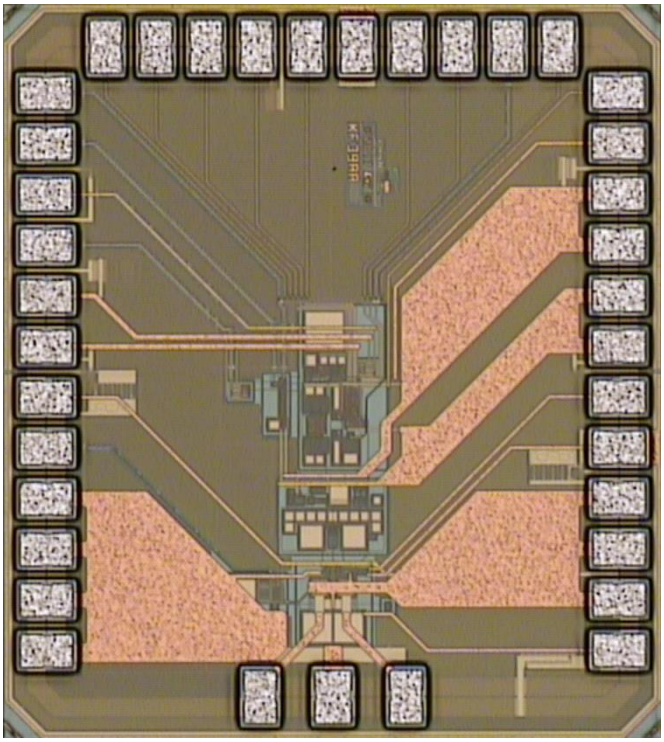
Fig. 3.13 show the micrograph of the dc-dc converter (excluding the transformer which is shown in Fig. 3.5). The chip sizes are 1.97 mm × 1.78 mm and 1.8 mm × 1.45 mm for chip A and chip B, respectively. The system was designed to deliver up to 130 mW with an isolated output voltage of 18 V (i.e., load resistance $R_L \approx 2.5$ kΩ). The output power is regulated by means of a control loop whose power consumption is negligible compared to the ones of the power link, thus avoiding power efficiency degradation. The simulated average current consumption of each building block of the control loop is reported in Table 3.4. The simulation results refer to a data rate for the control

TABLE 3.4
SIMULATED CURRENT CONSUMPTION OF THE CONTROL LOOP.

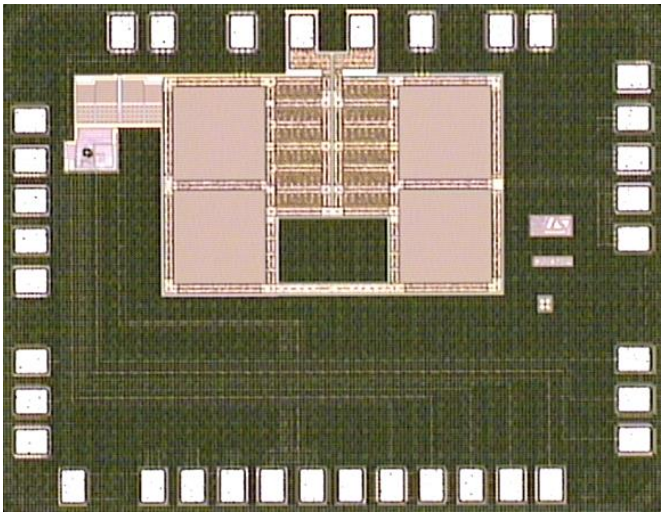
| | Block | Current consumption | Supply Voltage |
|---|---|---|---|
| Chip A | RX | 750 µA | 1.8 V |
| | PW-CTR | 120 µA | |
| Chip B | Error amplifier | 20 µA | 3.3 V |
| | PWM generator | 20 µA | |
| | TX | 150 µA | |

bits transmission of 12.8 Mbit/s (i.e., $f_{CK}$ = 12.8 MHz), while the frequency of PWM control signal was set to 50 kHz (i.e., N=256).

The supply voltage, $V_{DD}$, for the control loop blocks on Chip A was set to 1.8 V thus limiting the power consumption of the digital circuits, whereas the supply voltage, $V_{DD,ISO}$, on Chip B was set to 3.3 V to be compliant with the switches transistor $M_{TX1,2}$ used into the transmitter. $V_{DD}$ and $V_{DD,ISO}$ are derived from $V_{PWR}$ and $V_{ISO}$, respectively.



(a)



(b)

Fig. 3.13.Micrograph of the dc-dc converter: (a) Chip A, (b) Chip B.

Fig. 3.14 shows simulated single-ended voltage, $V_{D1}$, waveform at the LDMOS drains, differential voltage $V_{OSC,P}$ at the primary windings of $T$, and rectifier input voltage $V_R$. The amplitude of $V_{OSC,P}$ is about 10 V (i.e., two times the supply voltage), while the single-ended oscillation voltage at the LDMOS drains change from few millivolt to the maximum value of $V_{OSC,P}$, which are the typical waveforms of a D-class oscillator. The transformer turns' ratio performs the step-up conversion of the power signal thus providing a rectifier input voltage around 22 V which is properly rectified to obtain $V_{ISO}$.

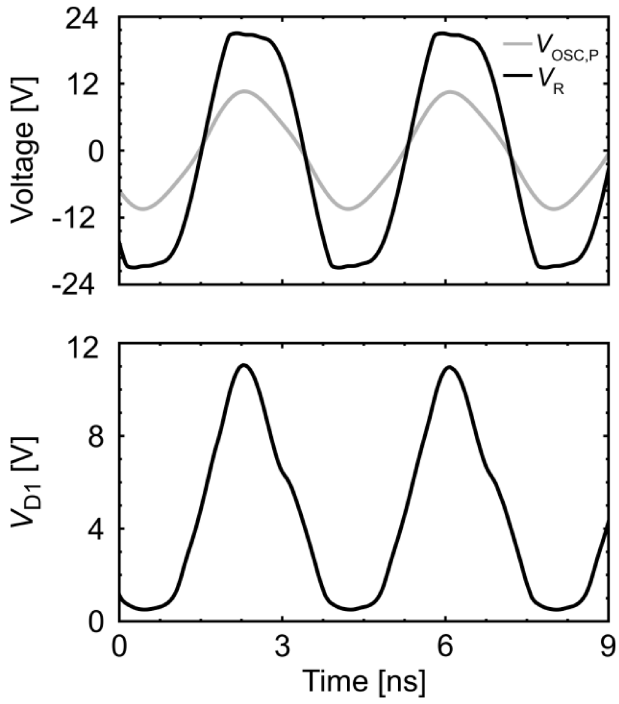



Fig. 3.14 Power link simulated waveforms ($P_{ISO}$ = 130 mW, $V_{ISO}$ = 18 V).

Fig. 3.15 shows the tuning range of the VCO which was simulated in typical condition and minimum and maximum corners. The input voltage, $V_{LP}$, is provided by the low-pass filter and it was changed from 0.4 V to 1.6 V which are the threshold voltage of the triode-MOS transistor $M_R$ and the maximum allowable output voltage of the charge pump, respectively. In such a condition, the VCO provides an oscillation frequency (i.e., $f_{PLL}$) ranging from 3.8 MHz to 21 MHz at nominal corner. The grey zone in the figure highlights the range of $f_{PLL}$ due to process tolerance which provides the frequency tuning from 9.5 MHz (i.e., maximum corner) to 16.2 MHz (i.e., minimum corner). Despite the reduction of the frequency control range, the VCO guarantees an oscillation frequency of 12.8 MHz which is the locked frequency for the PLL (i.e., $f^*_{CK}$).

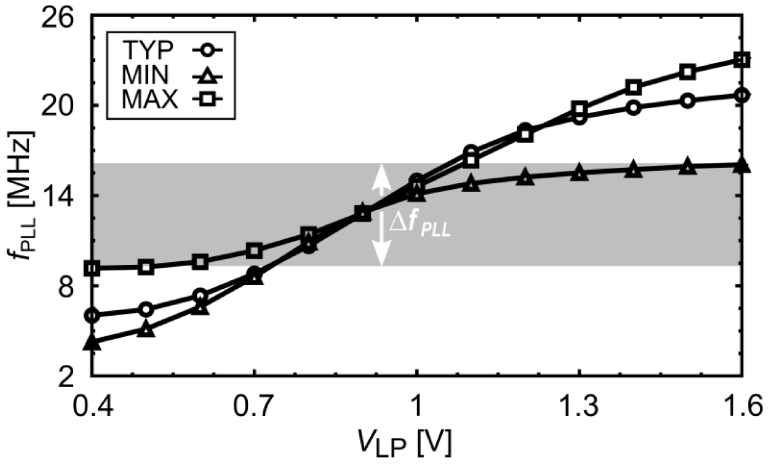



Fig. 3.15. Simulated VCO tuning range at typical, minimum and maximum corners.

Fig. 3.16 depicts the simulated transient response of the PLL to a step from 12.8 MHz to 14.5 MHz of the input reference frequency (i.e., $f^*_{CK}$) to verify the stability of the PLL loop. The frequency of output signal perfectly follows

the frequency variation of input signal, while the PLL control voltage shows the typical exponential response of a closed-loop with a phase margin of 60°.

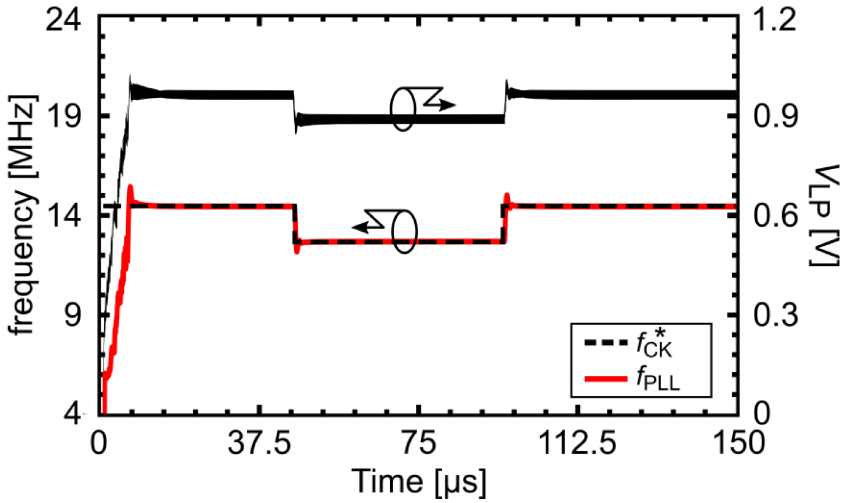



Fig. 3.16. Transient response of the PLL to a step from 12.8 MHz to 14.5 MHz of $f^*_{CK}$.

Finally, the complete control loop was simulated and the steady-state waveforms are stacked in Fig. 3.17.

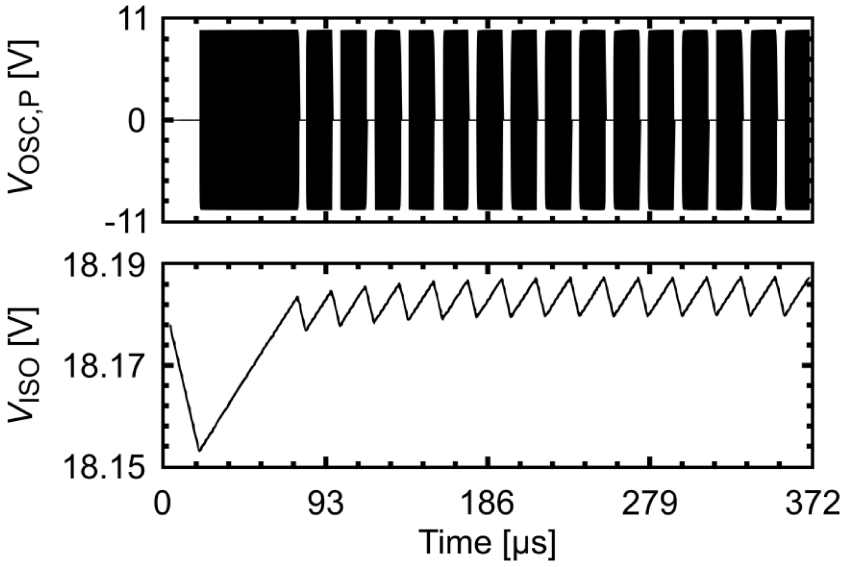



Fig. 3.17. Power voltage oscillation at primary winding and isolated output voltage in closed-loop condition.

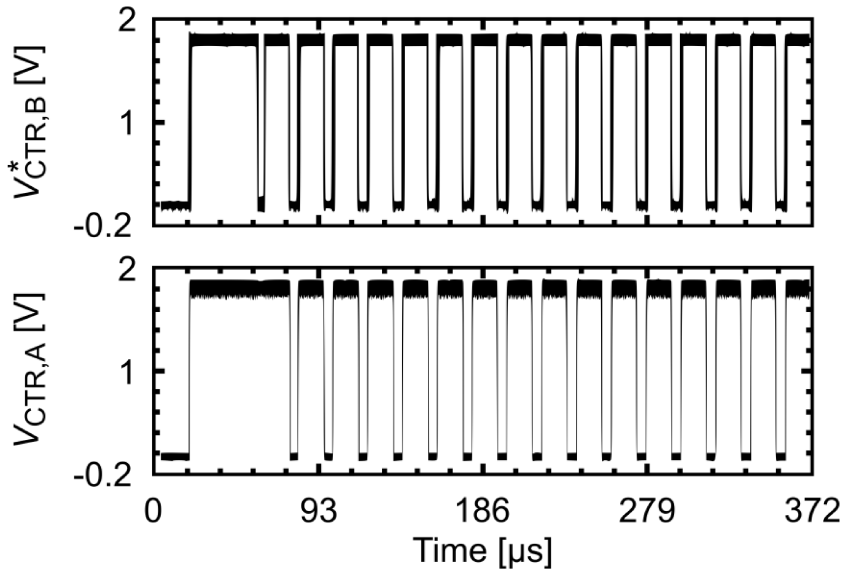



Fig. 3.18. Recovered data $V^*_{CTR,B}$ and PWM control signal $V_{CTR,A}$.

$V_{REF,OUT}$ of 18 V and $R_L$ of 2.5 kΩ were imposed, which set the steady-state output power to 130 mW and the duty cycle of the PWM control signal to 75%, as also apparent in Fig. 3.18 that compares the recovered data $V^*_{CTR,B}$ with the on-off signal $V_{CTR,A}$. The value of output capacitance was 4 μF which involves about 10 mV of ripple on $V_{ISO}$. The simulation was performed by pre-charging the output voltage close to the final value, thus obtaining simulation results in reasonable calculation times. However, complete system simulations were performed by means of Verilog-A models which are reported in appendix.

Fig. 3.19 shows the ASK modulation on power signal at the drain terminals of the n-MOS cross-coupled transistors $M_{1,2}$ (see Fig. 3.4). Specifically, the figure reports the oscillation voltage $V_{OSC,P}$ of Fig. 3.17 which is zoomed in the time range 271 μs – 275 μs. The modulation index is about 5% thus preserving power conversion efficiency. Moreover, it can be noticed that

during the on-phase of the power oscillator only bits-1 are transmitted while few bits-0 are used to turn off the power oscillator. Therefore, thanks to the PWM coding, the power signal takes the maximum value most of the on-time thus maximizing efficiency performance.

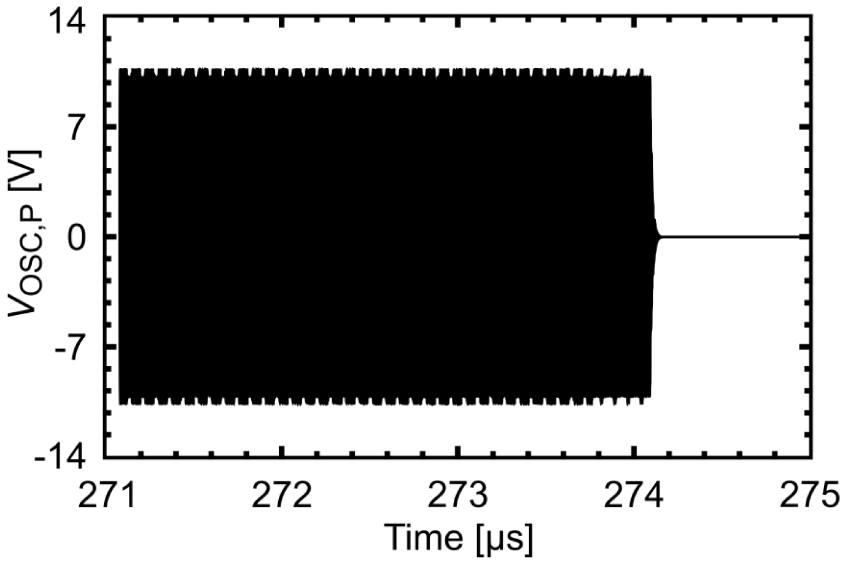



Fig. 3.19. ASK modulation on power voltage oscillation.

# Chapter 4.

# Dc-dc converter with data communication exploiting a single isolated link

## 4.1. Introduction

The architecture in [44] provides an efficient solution to minimize the number of isolated links while guaranteeing all power and data functionalities, such as power transfer, bidirectional data communication and output power regulation. However, the minimum number of isolated links has been achieved in [28] and [45] which exploit only one isolated channel but at the cost of waiving power regulation [28] or data transmission [45]. In this chapter a new patented solution [46] which makes compliant both power and

data functionalities on the same isolated link will be presented. The proposed architecture is based on the simplified scheme in Fig. 4.1 and consists of a unique isolation component (i.e., the isolation transformer) that performs both power and control signal transfer, while providing data transmission of N multiplexed data channels.

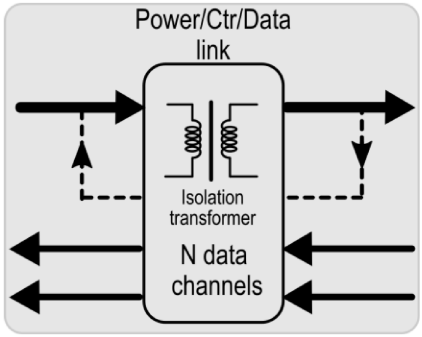



Fig. 4.1. Architecture of a galvanically isolated dc-dc converter with data communication using a single isolated link

The implementation of a single-channel galvanically isolated dc-dc converter with data communication poses several design challenges since power and data functionalities have contrasting requirements. For instance, highly efficient power transfer needs large isolation transformer (i.e., low winding resistivity and high *Q*-factor), which involves high parasitic capacitance between primary and secondary transformer windings thus increasing the injected currents due to CMTs. Therefore, performances such as CMTI and power conversion efficiency must be traded off. Moreover, data communication on the same channel of power transfer is not compliant with an on/off control scheme that is typically adopted for efficient power regulation. Indeed, data transmission exploits the power oscillation as the

carrier signal, which is not available during the off-phase, thus leading data bit losses.

Following these considerations, the proposed architecture is able to implement both data communication and control feedback loop on the same isolated link used for power transfer, regardless CMTI performance. Specifically, it delivers a regulated output power up to 50 mW with a power efficiency of 15.6% and provides data communication of 3 multiplexed data channels with a data rate up to 8 Mb/s. This performance makes the proposed system very suitable for sensor interface applications. Furthermore, this solution does not depend on the isolation component technology, as well as the architecture in [45], and can be implemented with two or three chips.

The chapter is organized as follows. Section 4.2 deals with system description and technology. The power/ctr/data link is presented in Section 4.3, while simulation results are shown in Section 4.4.

## 4.2. System Description

The simplified block diagram of the proposed system is depicted in 4.2. The converter is based on a patented architecture [46], which consists of a single isolated link used for power transfer, control signal feedback loop and data communication of N multiplexed data channels. The regulated output power is delivered to the external load, $R_L$-$C_L$, across the galvanic barrier thanks to a power-data-ctr link, which is made up of a power oscillator operated at 400 MHz, an isolation transformer, $T$, and a power rectifier. Differently from the widely adopted on/off control scheme, the dc output power, $P_{ISO}$, is regulated by means of a continuous-time feedback loop that

avoids the power oscillator shut-down, thus allowing power signal to be exploited for data communication. To this purpose, the power oscillator takes advantage of a controlled-current topology whose oscillation amplitude is set by the bias current, $I_{CTR}$.

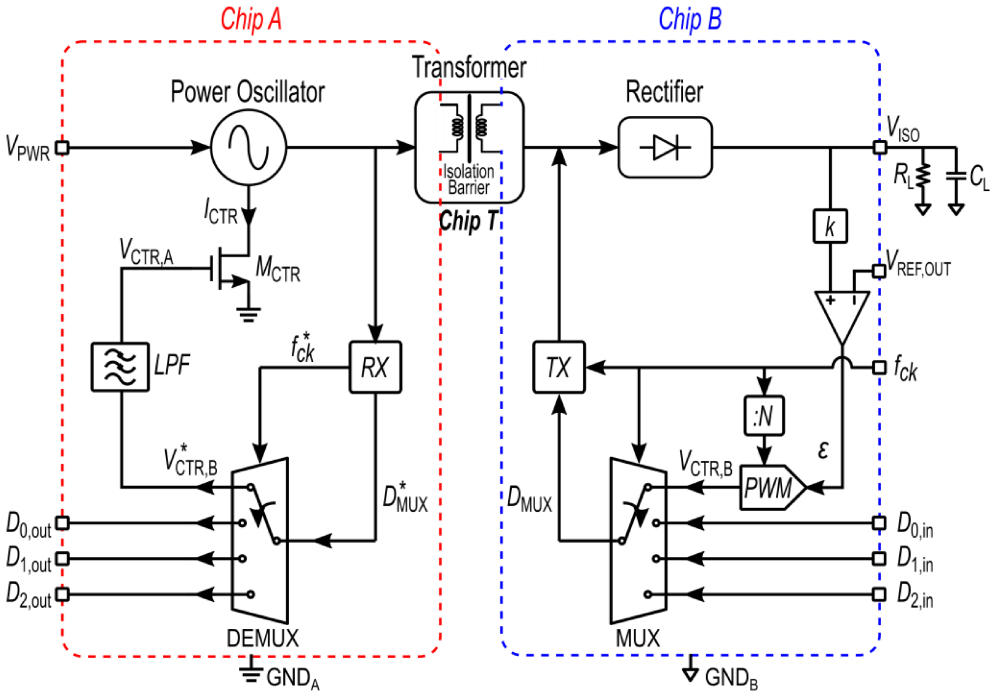



Fig. 4.2. Simplified block diagram of the dc-dc converter with data communication exploiting a single isolated link.

Specifically, the isolated output voltage, $V_{ISO}$, is compared with a reference voltage, $V_{REF,OUT}$, thus producing an error signal, ε, that changes according to the output power imposed by reference voltage $V_{REF,OUT}$ and load resistance $R_L$. The PWM block, which works as an 1-bit ADC, converts ε into a square wave voltage, $V_{CTR,B}$, whose duty cycle, $DC_{(VCTR,B)}$, depends on the dc value of ε, while the frequency is set according to an external reference clock, $f_{CK}$,

properly divided by an N factor. The reference clock, $f_{CK}$, is also used as master clock for the multiplexer which collects the input signals into a single digital word. The bitstream at the output of the MUX drives the transmitter which performs data transmission across the galvanic barrier by means of amplitude modulation of the power signal. The receiver on the oscillator side, recovers both data and clock, $f^*_{CK}$, signals which drive the demultiplexer. The latter splits up the recovered bitstream on the correspondent channels, thus providing the data bits to the output data channels (i.e., $D_{0\text{-}2,OUT}$) and the recovered control signal $V^*_{CTR,B}$ to a low-pass filter. The dc component, $V_{CTR,A}$, of $V^*_{CTR,B}$ drives the current generator $M_1$, thus providing the bias current, $I_{CTR}$, which set the oscillation amplitude of the power signal. Note that $I_{CTR}$ is related on the control signal ε, thus properly performing the output power regulation.

Similarly of the dc-dc converter presented in Chapter 3 [45], the proposed system was fabricated exploiting three different technologies. The isolation transformer (i.e., Chip T) was implemented in post-processed technology, as described in Chapter 1. The power oscillator chip (i.e., Chip A) takes advantage of the 0.18-µm BCD technology which provides high-voltage, high-power LDMOS. Finally, the 0.13-µm standard CMOS process was used to implement the power rectifier chip (i.e., Chip B) which exploits high-voltage Schottky diodes with sub-GHz operation capability for high rectifying efficiency.

## 4.3. Power-Data-Ctr Link

This Section focuses on the analysis of the isolated link with a detailed description of the main building blocks. The power-data-ctr link is the unique isolated channel of the proposed architecture and guarantees galvanic isolation between Chip A and Chip B, while performing both data and control signal transmission on the power signal used to provide the isolated supply voltage. The power link was designed to deliver a dc output power, $P_{ISO}$, around 50 mW at a nominal output voltage, $V_{ISO}$, of 3.3 V with a 5-V power supply, $V_{PWR}$. The control signal for output power regulation is multiplexed with N data channels which are transmitted across the galvanic barrier by properly modulating the power oscillation voltage. The output power is regulated by controlling the bias current of the power oscillator which is operated in B class. Typically, a D-class power oscillator along with an on/off control scheme are used in galvanically isolated dc-dc converters to achieve the maximum theoretical power conversion efficiency. However, the on/off control scheme does not allow data communication on power signal, while D-class topology suffers of CMTs noises. In such a condition, the B-class power oscillator was preferred since it provides a simpler solution both for continuous-time power regulation and CMTs rejection than the D-class topology. Fig. 4.3(a) and Fig. 4.4(a) depict the simplified schematics of the power link with oscillator operated in D class and B class, respectively, which have been used to compare the CMT performance of the two topologies. A voltage ramp, $V_{CM}$, is applied between the grounds of Chip A and Chip B, thus producing common-mode currents, $I_{CM}$, through the parasitic capacitances of the transformer. It can be notice that D-class oscillator

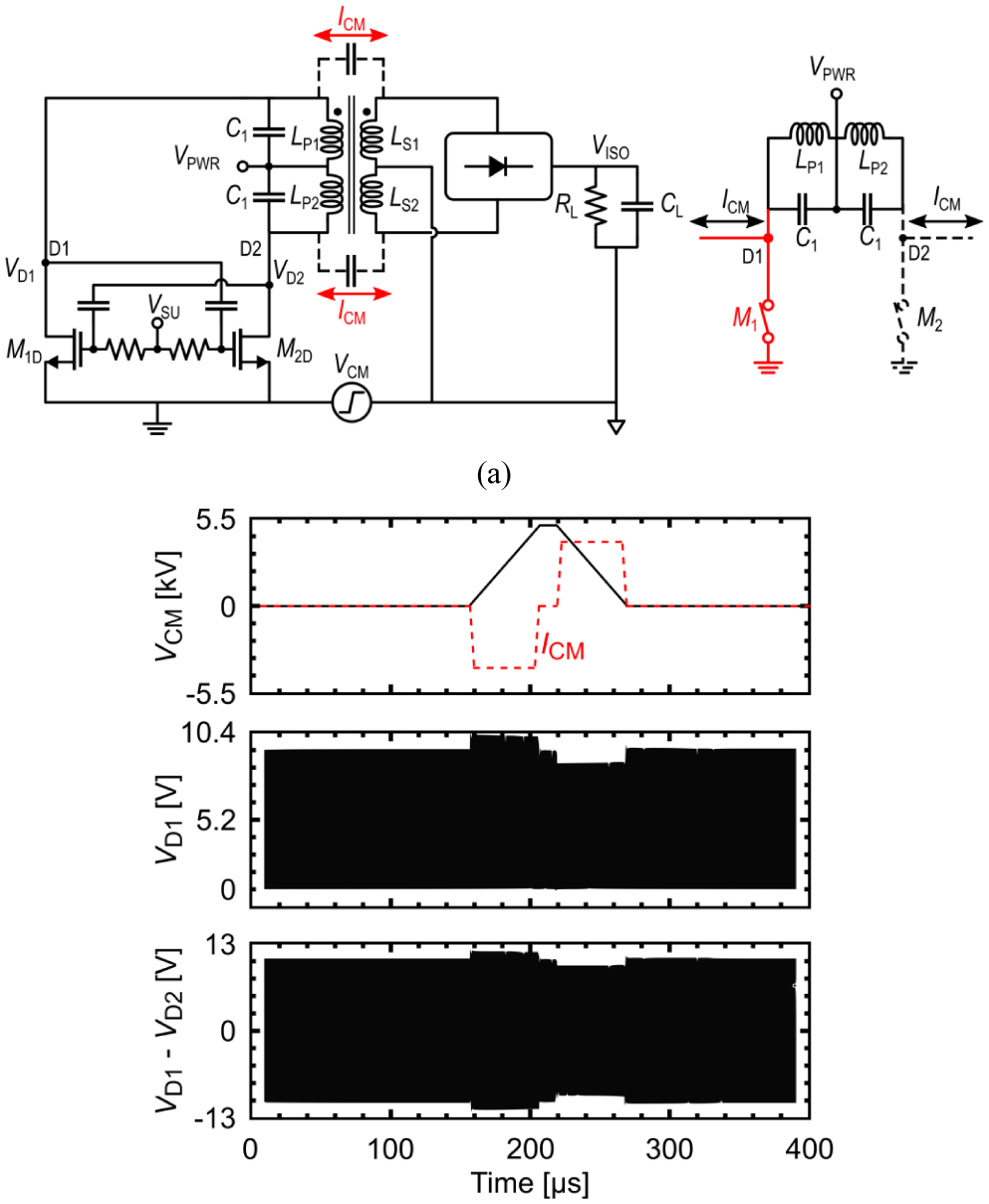
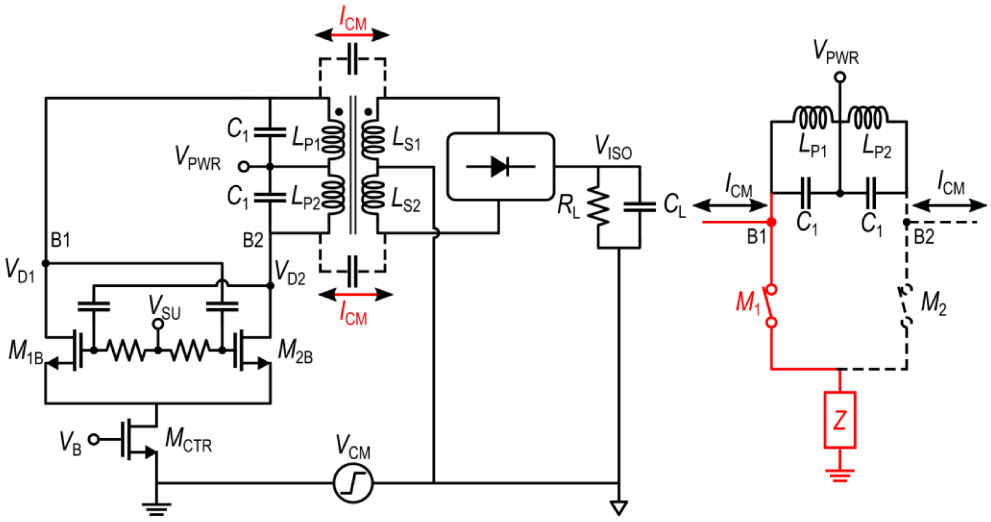
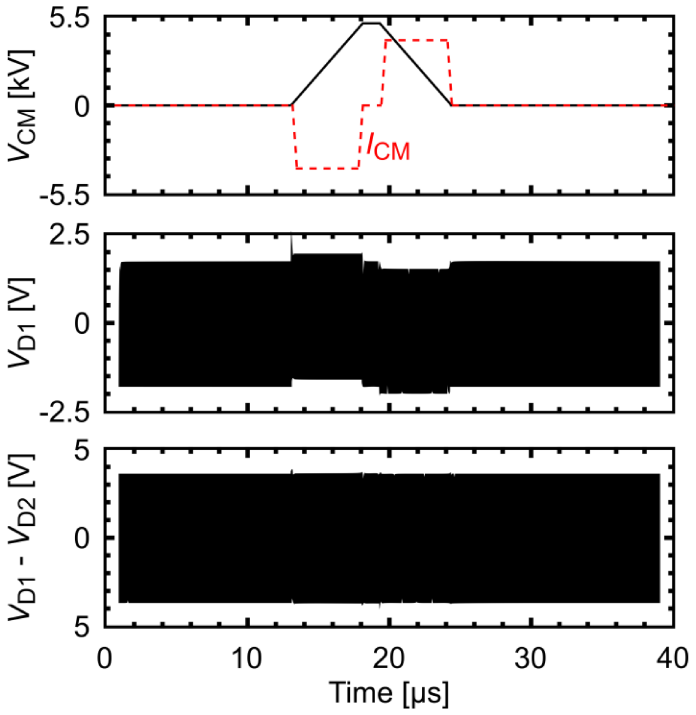



Fig. 4.3. CMT on power link with oscillator operation in D class: (a) simplified schematic, (b) simulated waveforms.




(a)




(b)

Fig. 4.4. CMT on power link with oscillator operation in B class: (a) simplified schematic, (b) simulated waveforms.

produces a differential signal when the CMT occurs, as shown Fig. 4.3(b). Specifically, if $M_{1D}$ is on (see Fig. 4.3(a)), the node D1 is connected to ground (i.e., low impedance) while D2 is connected to high impedance being $M_{2D}$ an off-switch. Therefore, the noise on D1 is different than the noise on D2 and the common-mode currents produce a differential-mode noise which affects data communication (the signal $V_{D1} - V_{D2}$ in Fig. 4.3(b) presents CMT noise). On the other hand, the B-class topology (see Fig. 4.4(a)) provides high impedance both on B1 and B2, thanks to the output impedance of the current generator $M_{CTR}$, thus producing a common-mode noise which can removed by common-mode filtering [44], without affecting data communication (the signal $V_{D1} - V_{D2}$ in Fig. 4.4(b) rejects the CMT noise).

The description of the power link is reported in Section 4.3.1, whereas the data communication and the control loop are described in Section 4.3.2 and Section 4.3.3, respectively.

### 4.3.1. Power Link

A simplified schematic of the power link is shown in Fig. 4.5. The architecture consists of a transformer-based power oscillator and a Schottky diodes rectifier, which perform dc-ac and ac-dc conversions, respectively. The power oscillator is based on a B-class topology which allows the control of the oscillation amplitude by properly setting the bias current, $I_{CTR}$. The regulation of $I_{CTR}$ is provided by the current generator $M_R$ whose control voltage, $V_{CTR,A}$, is directly related on the error signal ε, thus achieving output power regulation. The active core of the power oscillator is made up of LDMOS transistors, $M_{1,2}$, whose gate-source capacitances along with coupling capacitors $C_B$ perform a capacitive partition of the oscillation

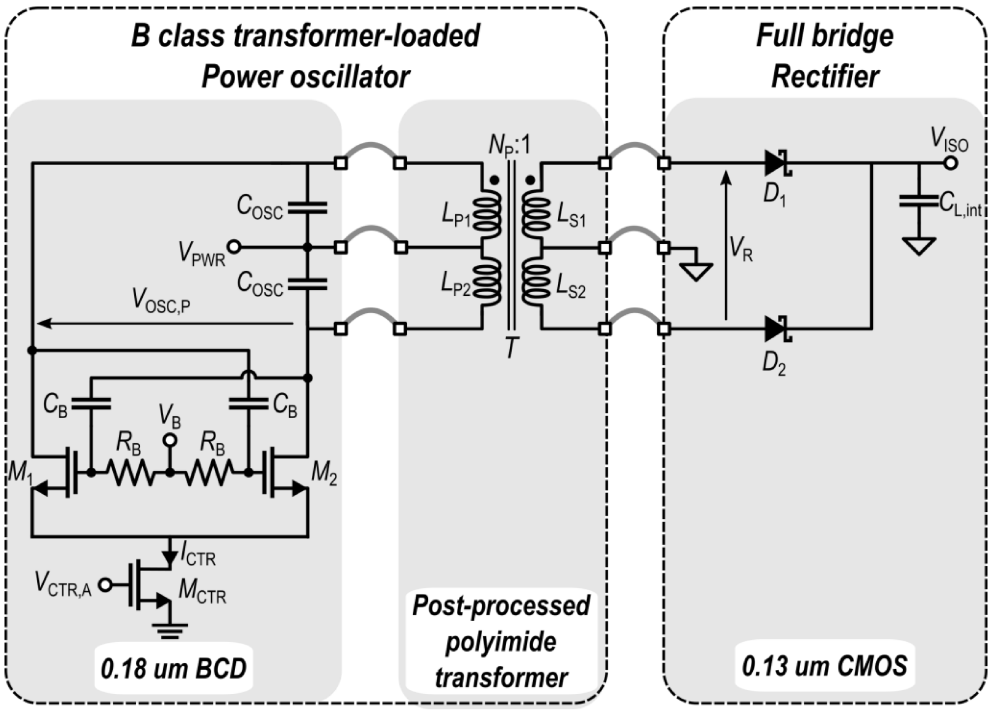



Fig. 4.5. Schematic of the power link.

voltage thus preventing the gate-oxide breakdown.

The resonant tank of the oscillator consists of capacitors $C_{OSC}$ and isolation transformer $T$. The geometrical structure of the transformer is shown in Fig. 4.6, while geometrical parameters of half of the transformer coils are summarized in Table 4.1. The isolation transformer was manufactured in a dedicated post-processed technology and presents the same differential stacked configuration of the power transformer used in [44] and [45].

Differently from common solutions based on a full-bridge rectifier, the proposed architecture takes advantage of a half-bridge topology, which achieves the same power conversion efficiency of the full-bridge rectifier but providing half of the input capacitance.

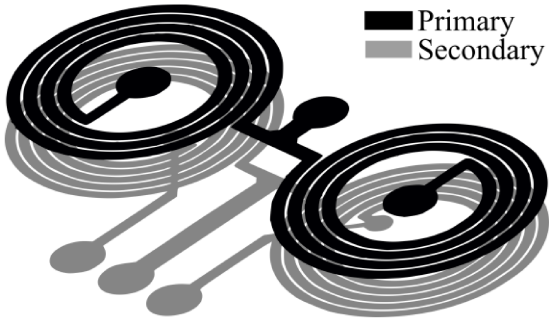



Fig. 4.6. Structure of the power isolation transformer.

TABLE 4.1
GEOMETRICAL PARAMETERS OF THE POWER-DATA-CRT TRANSFORMER.

| **Parameters** | **Primary Coil (half structure)** | **Secondary Coil (half structure)** |
|---|---|---|
| Number of turns ($n$) | 3.75 | 5 |
| Width ($w$) [µm] | 27.5 | 19.5 |
| Spacing (s) [µm] | 9.5 | 9.5 |
| Internal diameter ($d_{IN}$) [µm] | 320 | 310 |
| Outer diameter ($d_{OUT}$) | 617 | 606 |

TABLE 4.2
DESIGN PARAMETERS OF THE POWER LINK.

| **Block** | **Parameter** | **Value** | **Unit** |
|---|---|---|---|
| Power oscillator active core | $W_{1,2}$ | 460 | [µm] |
| | $C_B$ | 2.6 | [pF] |
| | $C_{OSC}$ | 5.6 | [pF] |
| | $f_P$ | 400 | [MHz] |
| Isolation transformer, $T_P$ | $L_{P1,2}$ \| $L_{S1,2}$ | 17.65 \| 30 @ $f_P$ | [nH] |
| | $Q_{P1,2}$ \| $Q_{S1,2}$ | 13 \| 10.6 @ $f_P$ | |
| | $k_P$ | 0.74 | |
| Rectifier | $M$ | 30 | |

The reduction of the rectifier impedance improves the performance of the dc-ac converter since the impedance of transformer-loaded power oscillator increase. Moreover, a lower capacitance partition is achieved at the input rectifier, thus providing a higher signal to the ac-dc converter.

For the sake of completeness, the design parameters of the overall power link are summarized in Table 4.2.

### 4.3.2. Data Link

The simplified schematic of the data link is shown in Fig. 4.7. A data communication from Chip B to Chip A is provided by means of ASK modulation of the power signal. Both N data channels, $D_{0\text{-}2,IN}$, and control signal, $V_{CTR,B}$, are multiplexed into a digital word which consists of a bitstream, $D_{MUX}$, at the output of the MUX. This bitstream drives the TX which performs the data transfers by means of impedance mismatch at secondary windings ($L_{S1,2}$) of transformer $T$. To this purpose, capacitors $C_{TX1,2}$ and ON/OFF switch resistances, which are implemented by MOS transistors $M_{TX1,2}$, are used. A Manchester coding is adopted to improves the robustness of data communication. Indeed, this type of coding maintains constant the average value of the envelop signal also if a long sequence of bits 0 or bits 1 occurs, thus avoiding a reduction of the noise margin of the detector. After the galvanic barrier, a receiver block, which is made up of a detector and decoder, recovers both data and sampling clock that are split in the correspondent channels by means of a DEMUX. The synchronization between MUX and DEMUX is mandatory to properly guarantee both data communication and power regulation. There are different solutions in

literature that performs the synchronization [66] by adding one or more synchronization bits (i.e., framing bits) to the beginning of the bitstream, as shown in Fig. 4.7. Alternatively, a start-up training phase can be exploited to perform the synchronization.

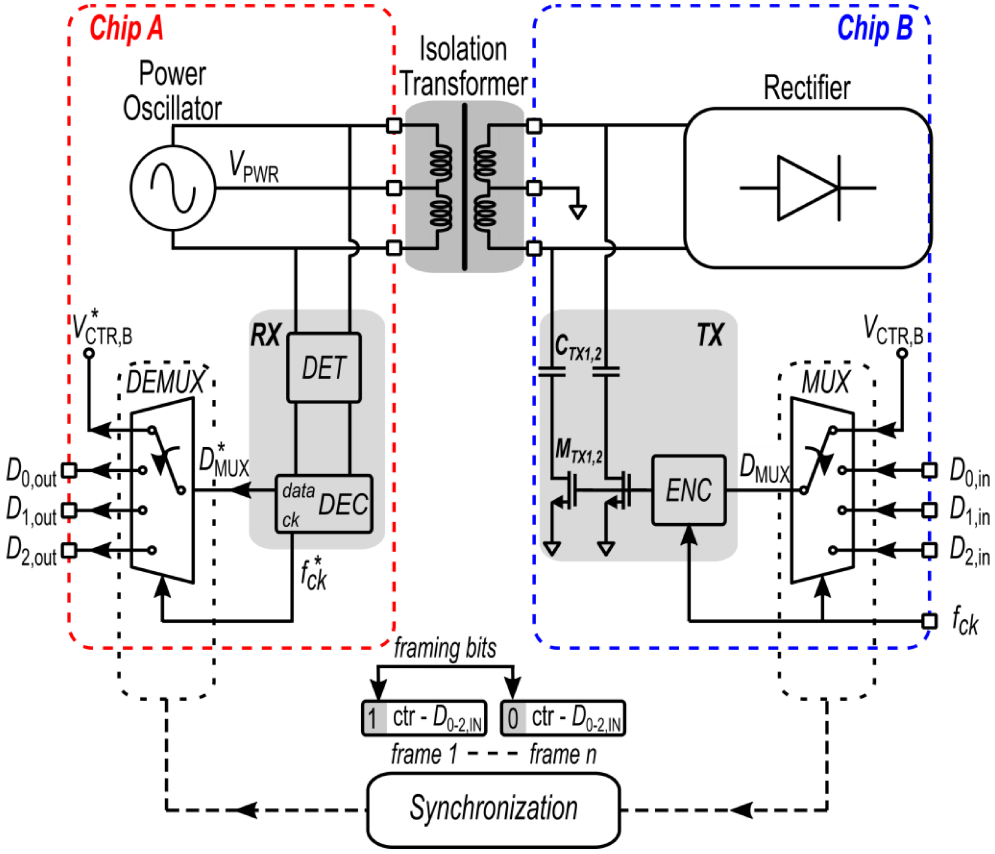



Fig. 4.7. Simplified schematic of data link with an example of synchronization.

The data transmission on power signal poses a big challenge on performing high CMT rejection. Indeed, the power transformer presents primary-to-secondary winding capacitances higher to the ones of a typical data transformer, thus involving higher common-mode currents during the CMTs.

Therefore, the power transfer performance is usually traded off with the CMTI requirements to be compliant with data communication. In any case, the proposed architecture is suitable with the CMT rejection circuit proposed in [44], which performs a common-mode filtering without affecting either data communication and power transfer performance. Thanks to both CMT rejection circuit and the higher robustness to CMT noise of the B-class power oscillator, state-of-the art CMTI performance can be easily achieved.

### 4.3.3. Control Link

A simplified schematic of the control loop is sketched in Fig. 4.8. For the sake of simplicity, the multiplexer and demultiplexer are not shown, although the control signal is multiplexed and transmitted along with data bits.

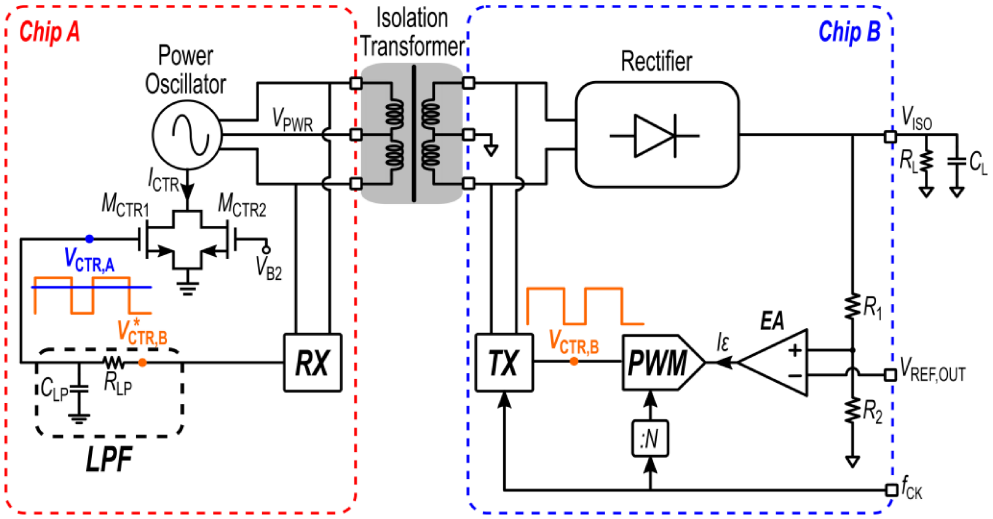



Fig. 4.8. Simplified schematic of the control link.

Output voltage $V_{ISO}$ is reduced by the resistive partition, $R_1$ and $R_2$ (i.e., $k$ in Fig. 4.2), and then compared with the reference voltage, $V_{REF,OUT}$, by means

of an error amplifier which is implemented by an operational transconductance amplifier. The output signal, $I\varepsilon$, of the error amplifier drives the PWM block thus providing a PWM signal, $V_{CTR,B}$, whose duty cycle is related to $I\varepsilon$, as in the PWM block of the system in [45] (see Chapter 3). The PWM signal $V_{CTR,B}$ is then transmitted across the galvanic barrier by means of a data communication from Chip B to Chip A. After the galvanic barrier, the low-pass filter (i.e., $R_{LP}$-$C_{LP}$) provides the dc component, $V_{CTR,A}$, of the recovered data, $V^*_{CTR,B}$, to the current generator $M_{CTR1}$ thus tuning the bias current of the power oscillator, $I_{CTR}$, according to the output power level to be provided. Moreover, $I_{CTR}$ consists of an additional component which is set by $M_{CTR2}$ and provides the minimum bias current for proper operation of the power link. Specifically, the expression of $I_{CTR}$ is given in equation (4.1)

$$I_{CTR} = I_{CTR1} + I_{CTR2} \tag{4.1}$$

where $I_{CTR2}$ is provided by $M_{CTR2}$ according to the bias voltage, $V_{B2}$, while $I_{CTR1}$ is the control variable provided by $M_{CTR1}$ and related to the error signal by equation (4.2)

$$I_{CTR1} = gm_{CTR,1}[(V_H - V_L) \cdot DC(I_\varepsilon)] \tag{4.2}$$

being $gm_{CTR,1}$ the transconductance of $M_{CTR,1}$, $V_H$ and $V_L$ the minimum and maximum value, respectively, of $V^*_{CTR,B}$, and DC is the duty cycle provided by the PMW block as function of the error signal, which is reported in equation (3.3).

Finally, the loop stability analysis was carried out considering a single pole approximation for each block of the control loop. By referring to the simplified model in Fig. 4.9, the open loop gain, $T_O$, can be written as

$$T_0 \cong k \cdot A_{EA} \cdot A_{CTR} \cdot A_{TX/RX} \cdot A_{LPF} \cdot A_P \tag{4.3}$$

where $k$ is the resistive partition, $A_{\mathrm{EA}}$ is the error amplifier gain and $A_{\mathrm{CTR}}$, is the gain of the PWM block, which are the transfer factors from isolated output voltage $V_{\mathrm{ISO}}$ to the duty cycle of the PWM signal $V_{\mathrm{CTR,B}}$ on Chip B. Finally, $A_{\mathrm{TX/RX}}$, $A_{\mathrm{LPF}}$ and $A_{\mathrm{P}}$ are the transfer functions of the TX/RX block, low-pass filter and power link, respectively.

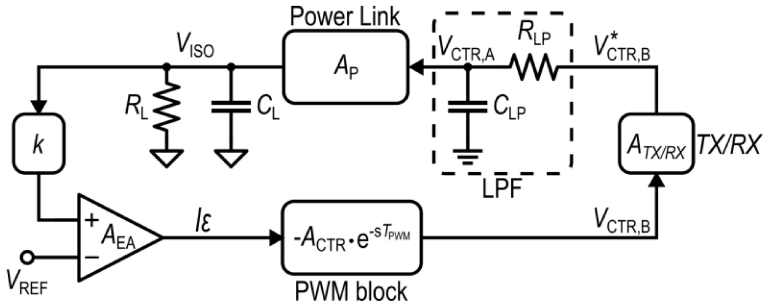



Fig. 4.9. Simplified model of the control link for stability analysis.

The expression of the gains which compose the control loop are reported from equation (4.4) to (4.8).

$$A_{EA} = \frac{dI_\varepsilon}{d(V_{ISO}/k)} = G_M \tag{4.4}$$

$$A_{CTR} = \frac{dDC_{(V_{CTR,B})}}{dI_\varepsilon} = -\frac{NDC^2_{(V_{CTR,B})}}{f_{ck}(V_{COMP} - V_{GND})C_I} \tag{4.5}$$

$$A_{TX/RX} = \frac{dDC_{(V_{CTR,A})}}{dDC_{(V_{CTR,B})}} \cong 1 \tag{4.6}$$

$$A_{LPF} = \frac{dV_{CTR,A}}{dDC_{(V_{CTR,A})}} = V_H - V_L \tag{4.7}$$

$$A_P = \frac{dV_{ISO}}{dV_{CTR,A}} = gm_{CTR,1} \frac{2}{\pi} R_{TR} \sqrt{\frac{L_S}{L_P}} k_C \frac{2}{\pi} \tag{4.8}$$

being $G_M$ the transconductance of the error amplifier, $DC_{(VCTR,B)}$ and $DC_{(VCTR,A)}$ the duty cycle of $V_{CTR,B}$ and $V_{CTR,A}$, respectively, $R_{TR}$ the equivalent resistance at the primary winding of the transformer and $k_C$ the magnetic coupling factor of the transformer.

An expression of the loop gain transfer function, $T(s)$, was evaluated by considering the two main low frequency contributions, i.e. the pole of the power link at the output (i.e., $R_L$-$C_L$), and the pole of the low-pass filter pole (i.e., $R_{LP}$-$C_{LP}$). Differently from (3.12), the delay introduced by the PWM block has been neglected since the period of the PWM control signal is set much lower than the time constant of the low-pass filter (i.e. $1/R_{LP}C_{LP} << 1/T_{PWM}$),

$$T(s) = T_O \frac{1}{(1 + sR_LC_L) \cdot (1 + sR_{LP}C_{LP})} \tag{4.9}$$

In the worst case, a maximum 40-dB open loop gain $T_O$ was set. Therefore, a dominant pole compensation can be easily achieved increasing the load capacitance, $C_L$, whose value can be evaluated from

$$C_L = \frac{T_O \cdot R_{LP} \cdot C_{LP}}{R_L \cdot \tan\left(\frac{\pi}{2} - PM\right)} \tag{4.10}$$

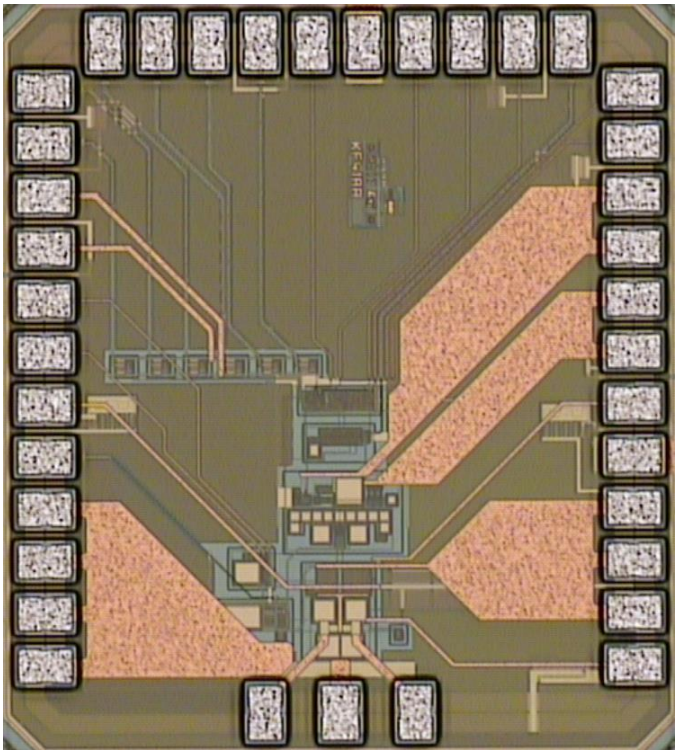
where *PM* is the required phase margin expressed in radians. As a result, to guarantee a phase margin of 60°, a few-microfarads is required. Such values provide adequate performance in terms of both output voltage ripple and transient responses.

## 4.4. Simulation Results

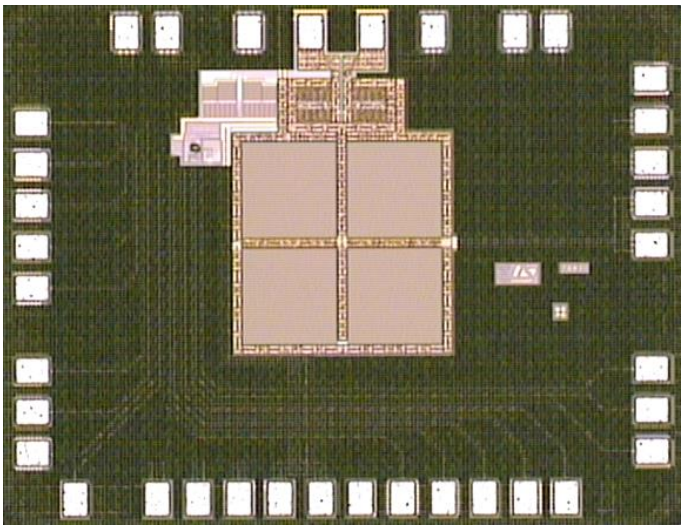
Fig. 4.10 shows the micrograph of the dc-dc converter (excluding the transformer which is shown in Fig. 4.6). The chip sizes are 1.97 mm × 1.78 mm and 1.8 mm × 1.45 mm for chip A and chip B, respectively. The system was designed to deliver up to 50 mW with a regulated output voltage of 3.3 V (i.e., load resistance $R_L \approx 220\ \Omega$). The power consumption of the control loop is negligible compared to the ones of the power link, thus avoiding any power efficiency degradation. The simulated current consumption of each building block of the control loop is reported in Table 4.3.

TABLE 4.3
SIMULATED CURRENT CONSUMPTION OF THE CONTROL LOOP.

| | **Block** | **Current consumption** | **Supply Voltage** |
|---|---|---|---|
| Chip A | RX | 370 µA | 1.8 V |
| | DEMUX | 30 µA | |
| Chip B | Error amplifier | 20 µA | 3.3 V |
| | PWM generator | 50 µA | |
| | TX | 200 µA | |
| | MUX | 20 µA | |



(a)



(b)

Fig. 4.10. Micrograph of the dc-dc converter: (a) Chip A, (b) Chip B.

The simulations were carried out by setting the frequency of the PWM control signal at the value of 1 MHz, while the master clock of the MUX was 32 MHz, thus multiplexing four channels of 8 Mb/s.

Fig. 4.11 shows the simulated waveforms in close-loop condition using a 1-µF output capacitance. $V_{REF,OUT}$ of 3.3 V and $R_L$ of 220 Ω were imposed, which set the steady-state output power to 50 mW. Specifically, the control voltage, $V_{CTR,A}$, at the output of the low-pass filter and the isolated output voltage, $V_{ISO}$, are depicted. The simulation was performed by pre-charging the output voltage close to the final value, thus obtaining simulation results in reasonable calculation times. However, complete system simulations were performed by means of Verilog-A models which are reported in appendix.

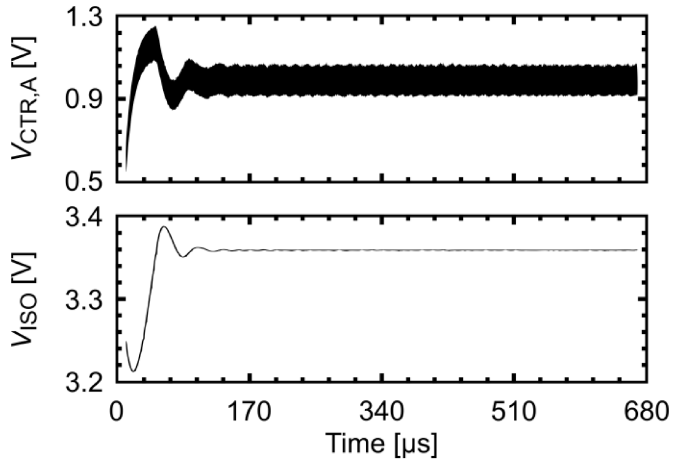



Fig. 4.11. Simulated control voltage, $V_{CTR,A}$, and isolated output voltage, $V_{ISO}$, in closed-loop condition.

Fig. 4.12 shows the power oscillation signal at the primary winding and the ASK modulation which performs data communication from Chip B to Chip A. Differently from [45], the modulation index is not crucial for power

efficiency performance since most of efficiency loss is due by the power oscillator operating in B class. Therefore, a modulation index of about 16% was chosen with the aim of increasing the noise margin of the detector.

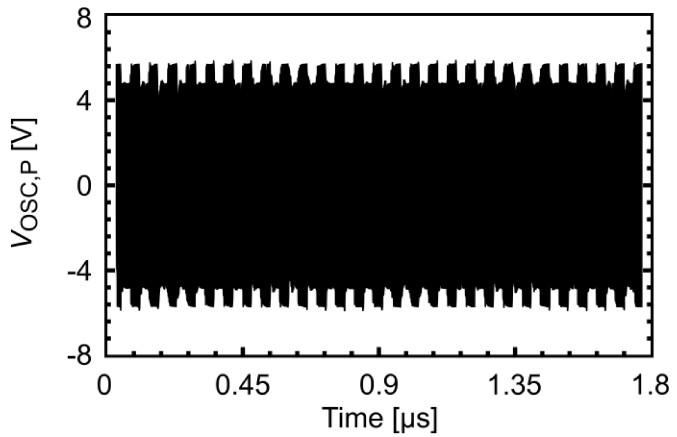



Fig. 4.12. ASK modulation on power voltage oscillation.

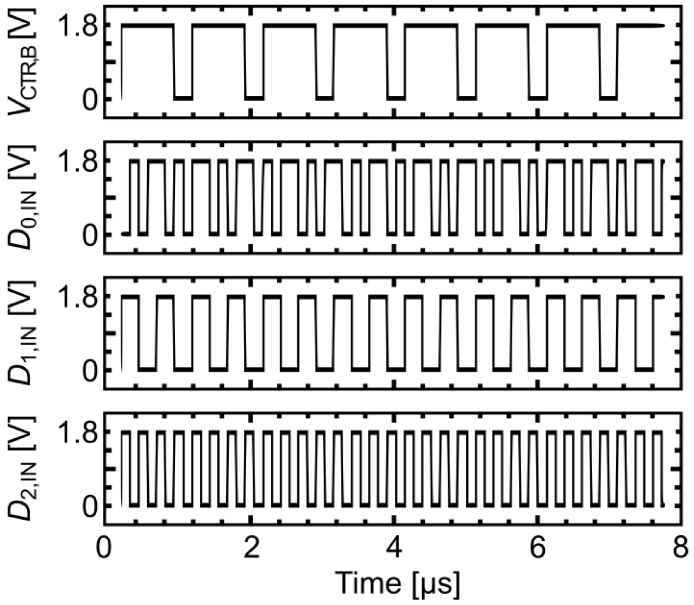



Fig. 4.13. Input signals of MUX.

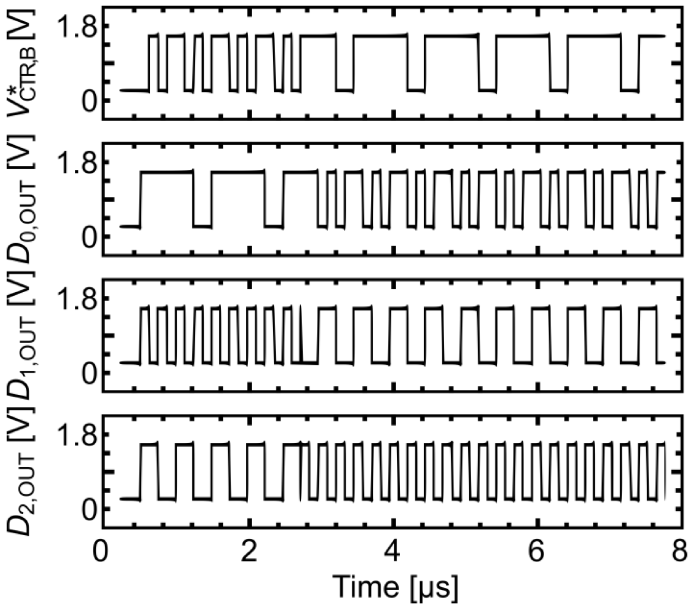



Fig. 4.14. Output signals of DEMUX.

Finally, data transmission of the control signal along with three data channels was checked. The input signals of the MUX and the output signals of the DEMUX are stacked in Fig. 4.13 and Fig. 4.14, respectively, which also show the start-up training phase of the MUX-DEMUX synchronization.

# APPENDIX A

## Verilog-A models for system simulations

## A. Introduction

This appendix presents the Verilog-A codes which have been used to carry out system simulations. The proposed architectures are made up of several circuital blocks and consist of a very complex transistor-level implementation. Moreover, the frequency-domain of the systems contains different operating frequencies thus involving a considerable calculation time, especially in transient simulations which are essential for closed-loop analysis of the control link. Following these considerations, the building blocks of the architectures in [45] and [46] have been modelled by using the modeling language Verilog-A which is compliant with *eldo* platform on cadence environment.

Fig. A.1and Fig. A.2 show the block diagram of the models which are used to simulate the control loop of the architectures in [45] and [46], respectively. The galvanic isolation between Chip A and Chip B is not included into the models, since the aim of these simulations is to verify the proper operation of output power control and analyze the feedback loop stability.

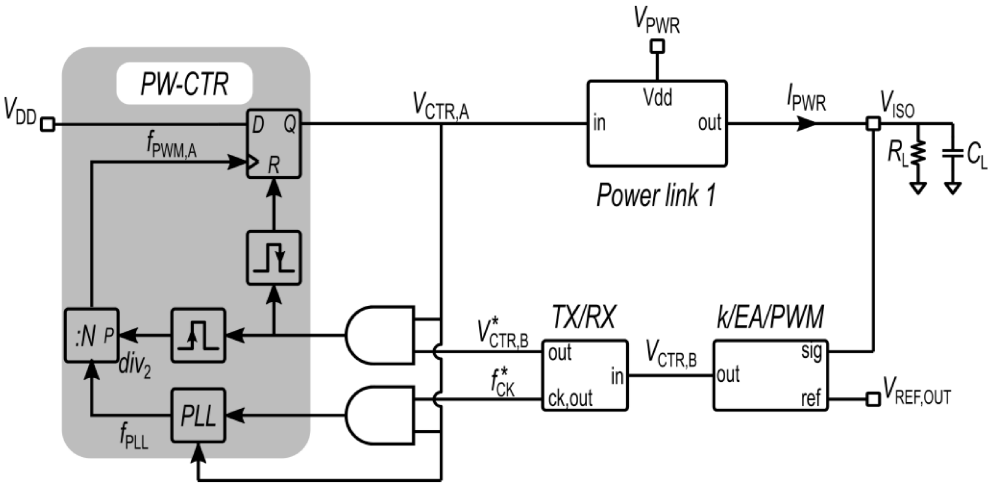



Fig. A.1. Model of architecture in [45].

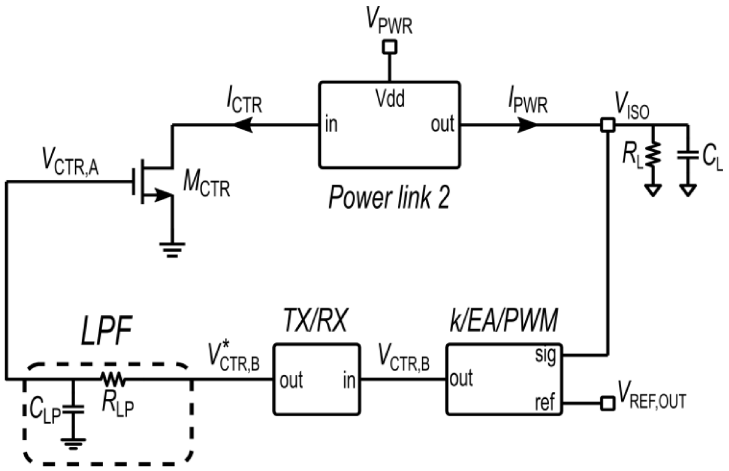



Fig. A.2. Model of architecture in [46].

The models exploit a mixed implementation of the systems which consists of both behavioral and transistor level circuital blocks. Specifically, the model of the architecture in [45] (see Fig. A.1), which refers to the schematic in Fig. 3.6, has been achieved by considering the transistor-level circuit of the PW-CTR and the behavioral modeling of the remaining blocks whose models are listed below. Moreover, the block diagram in Fig. A.1 includes AND gates which provide the recovered data and clock to the PW-CTR circuit during the on-state of the oscillator, while no recovered signals are provided during the off-state.

## B. Power link 1

The power transfer from chip A to chip B is performed by means of charge injection to the output load, $R_L$-$C_L$. Therefore, the power link behavior is similar to a current source. It can be notice that the delivered current, $I_{PWR}$, depends on $R_L$-$C_L$ thus leading $I_{PWR}$ to be expressed as function of the output voltage, $V_{ISO}$. Specifically, a second-order expression was chosen to implement the relationship between $I_{PWR}$ and $V_{ISO}$. Moreover, the on/off control is implemented by the digital input signal, $V_{CTR,A}$, that resets $I_{PWR}$ during the off-phase of the oscillator. The design modeling is described as followed:

```
‘include “constants.vams”
‘include “disciplines.vams”
module power_link_1(in, vdd, out, gnd);
```

```
    inout in, vdd, out, gnd;
    electrical in, vdd, out, gnd;
    parameter real a1 = -52µ;
    parameter real b1 = 1.4m;
    parameter real c1 = 1m;
    analog begin
    I(gnd, out) <+ V(in, gnd)*(a1*V(out,gnd)**2+b1*V(out,gnd)+c1);
    end
endmodule
```

## C. k/EA/PWM

This block provides the PWM signal, $V_{CTR,B}$. by means of modelling the behavior of the resistive partition, error amplifier and PWM circuit.

```
‘include “constants.vams”
‘include “disciplines.vams”
module k/EA/PWM(sig, ref, out);
    inout sig, ref, out;
    electrical sig, ref, out;
    parameter real gm = 50 µ; // transconductance of error amplifier.
    parameter real k = 13; // resistive partition.
    parameter real tck = 20µ; // reference frequency (i.e, fck/N).
    parameter real C = 1p; // integration capacitance C1 (see Fig. 3.6a).
    real vx;
```

```
    real vo = 0;
    real reset = 0;
    analog begin
    // voltage ramp:
        vx = idt(gm*k*V(sig, ref)/C, 0, reset); // charge phase of C_I.
    // comparator:
        @(cross(v(x)-1, +1)) begin
            vo = 0;
            reset = 1;
        end
    // reset of the voltage ramp for each clock period:
        @(timer(1n, tck)) begin
            reset = 0;
            vo = 1;
        end
    // pulse to reset the voltage ramp:
        @(timer(0, tck)) begin
            reset = 1;
        end
    v(out) <+ transition(vo, 0, 1n, 1n);
    end
endmodule
```

## D. TX/RX

The data transmission of control bits involves the sampling of the PWM signal, $V_{CTR,B}$, which is performed by the transmitter, TX, while the receiver, RX, recovers both data and clock. These operations are achieved by means of the TX/RX block whose design modeling is described as followed:

```
‘include “constants.vams”
‘include “disciplines.vams”
module TX/RX(in, out, ck_out);
    inout in, out, ck_out;
    electrical in, out, ck_out;
    parameter real del = 100n; //
    parameter real del_sample = 10n; //
    parameter real fck = 12.8M; // reference frequency (i.e, fck).
    real sample_x;
    real sample_y;
    real vy;
    real vck = 0;
    analog begin
        @(timer (del_sample+0.5/fck,1/fck))
            sample_x = v(in) > 0.5;
        v(x) <+ sample_x;
        @(timer (del_sample,1/fck))
            sample_y = v(x) > 0.5;
        @(timer (del_sample,1/(2*fck)))
            vck = !vck;
```

```
            v(y) <+ sample_y;
            vy = v(y);
            v(out) <+ transition(vy, del, 1n, 1n);
            v(ck_out) <+ transition(vck, del, 1n, 1n);
        end
    endmodule
```

Finally, the model of the architecture in [46] (see Fig. A.2), which refers to the schematic in Fig. 4.8, consists of transistor-level circuit for the current generator which biases the power oscillator and behavioral models for the remaining blocks. The description of the power link is provided below, while the Verilog-A codes of k/EA/PWM and TX/RX blocks are similar to the ones of the previous model with different values of frequency references. Specifically, fck/N = 1 MHz and fck = 32 MHz.

## E. Power link 2

The power link in [46] is based on a B-class topology for the power oscillator which allows output power regulation by adjusting the bias current, $I_{CTR}$. Therefore, the delivered output current, $I_{PWR}$; depends on $I_{CTR}$.. The design modeling is described as followed.

```
    ‘include “constants.vams”
    ‘include “disciplines.vams”
    module power_link_2(in, vdd, out, gnd);
        inout in, vdd, out, gnd;
```

```
    electrical in, vdd, out, gnd;
    parameter real Iout0 = -7m; //output short-circuit current.
    parameter real kiosc = 0.3; //dependence from the input current.
    parameter real kvout = -0.9m; //dependence from the output voltage.
    analog begin
    I(gnd, out) <+ Iout0 + kiosc*I(vdd, in) + kvout*V(out, gnd);
    end
endmodule
```

# APPENDIX B

## Test equipment

The experimental measurements have been carried out at the RF-ADC laboratory which has advanced tools for both on-wafer and on-board testing. Fig. A.1 shows the test bench used for the characterization of the dc-dc converter [44] in Chapter 2. The main tools and equipment exploited for the measurements are listed below:

- Agilent triple output DC power supply E3631A
- Agilent dual output DC power supply E3649A
- Agilent digital multimeter 34401A
- Agilent waveform generator 33250A
- Agilent EXG analog signal generator

- Agilent digital storage oscilloscope DS09104A
- Agilent multimeter U1272A
- InfiniiMax probe 1134A

Moreover, a Cascade-Microtech summit 12k probe station (Fig. B.2) is used for on-wafer measurements of test chips which include passive components. The probe station has also an optical microscope and a camera that performs the die micrographs.

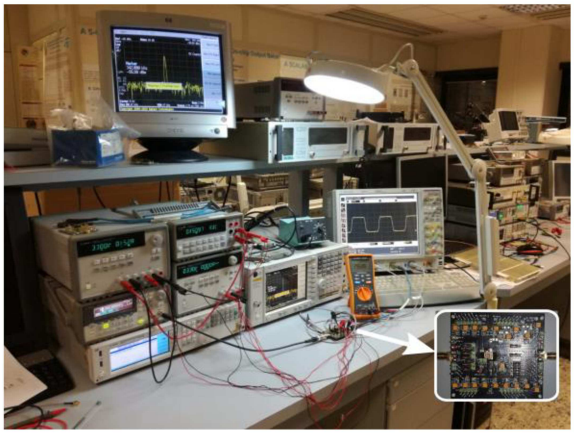


Fig. B.1. Photograph of the experimental setup for the dc-dc converter in Chapter 2.

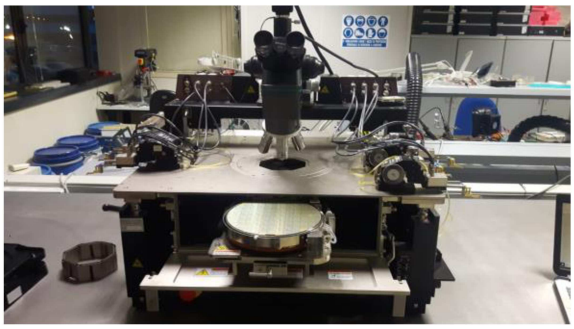


Fig. B.2. Cascade-Microtech probe station.

Similar equipment setup will be adopted for the experimental tests of the systems [45]-[46] presented in Chapter 3 and Chapter 4 whose integrated active cores are shown in Fig. B.3 and Fig. B.4. Specifically, Fig. B.3 displays the chip A of [45] (label A) and [46] (label B), whereas Fig. B.4 shows the chip B of [45] (label A) and [46] (label B).

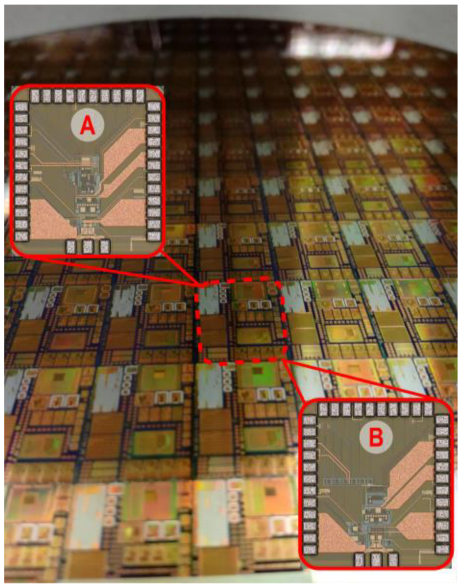



Fig. B.3. Photograph of the silicon wafer manufactured in BCD technology.

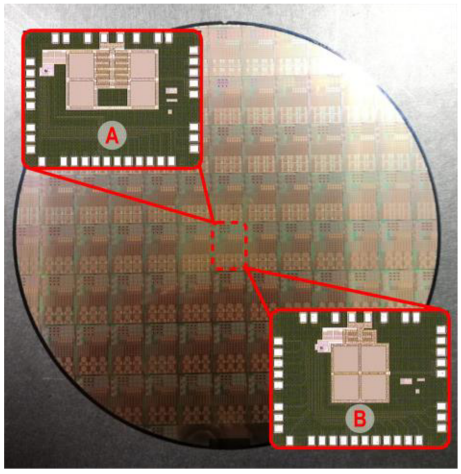



Fig. B.4. Photograph of the silicon wafer manufactured in CMOS technology.

# APPENDIX C

## Publications

## A. Patents

1. E. Ragonese, N. Spina, P. Lombardo, N. Greco, A. Parisi, G. Palmisano, “Galvanically isolated DC-DC converter with bidirectional data transmission,” U.S. Patent 9948193B2, granted 17 April 2018.
2. E. Ragonese, N. Spina, P. Lombardo, N. Greco, A. Parisi, G. Palmisano, “Galvanically isolated DC-DC converter with bidirectional data transmission,” U.S. Patent Appl. 15914257, filed 7 March 2018.

3. E. Ragonese, N. Spina, A. Parisi, P. Lombardo, N. Greco, G. Palmisano, “A galvanic isolation circuit, corresponding system and method,” US Patent Appl. 15468306, filed 24 Mar 2017.
4. E. Ragonese, N. Spina, A. Parisi, P. Lombardo, N. Greco, G. Palmisano, “A galvanic isolation circuit, corresponding system and method,” EU Patent Appl. 17161341.7, filed 16 Mar. 2017.
5. A. Parisi, N. Greco, N. Spina, E. Ragonese, G. Palmisano, “A galvanically isolated dc-dc circuit converter, with data communication, corresponding system and corresponding method,” IT Patent Appl. 102018000000830, filed 12 Jan. 2018.
6. A. Parisi, N. Greco, N. Spina, E. Ragonese, G. Palmisano, “A galvanic isolation circuit and system, corresponding method”, IT Patent Appl. 1020180000417, filed 3 April 2018.

# B. Conferences

1. N. Greco, A. Parisi, G. Palmisano, N. Spina and E. Ragonese, “Integrated transformer modelling for galvanically isolated power transfer systems,” in *13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Giardini Naxos, 2017, pp. 325–328.
2. A. Parisi, N. Greco, N. Spina, E. Ragonese and G. Palmisano, “Integrated power and data transfer systems with galvanic isolation,” in *49th Annual Meeting of the Associazione Società Italiana di Elettronica (SIE)*, Palermo, 2017, pp. 47–48.

3. N. Greco, A. Parisi, P. Lombardo, N. Spina, E. Ragonese and G. Palmisano, “A 100-mW fully integrated DC-DC converter with double galvanic Isolation,” in *43rd European Solid-State Circuits Conference (ESSCIRC)*, Leuven, 2017, pp 291-294.
4. E. Ragonese, A. Parisi, N. Spina and G. Palmisano, “Fully integrated galvanically isolated DC-DC converters based on inductive coupling,” *ApplePies*, Pisa, 2018, to be published).

# C. Peer-reviewed journal

1. A. Parisi, A. Finocchiaro, and G. Palmisano. “An accurate 1-V threshold voltage reference for ultra-low power applications,” *Microelectronics Journal* 63 (2017): 155-159.
2. E. Ragonese, N. Spina, A. Castorina, P. Lombardo, N. Greco, A. Parisi and G. Palmisano, “A fully integrated galvanically isolated DC-DC converter with data communication,” *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 65, no. 4, pp. 1432-1441, April 2018.
3. N. Greco, A. Parisi, G. Palmisano, N. Spina and E. Ragonese, “Integrated transformer modelling for galvanically isolated power transfer systems,” Elsevier, Integration, the VLSI Journal, Special Issue on PRIME and SMACD 2017, published on-line.
4. N. Greco, A. Parisi, P. Lombardo, N. Spina, E. Ragonese and G. Palmisano, “A double-isolated DC-DC converter based on integrated LC resonant barriers,” *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 65, no. 12, pp. 4423-4433, June 2018.

5. A. Parisi, A. Finocchiaro, G. Papotto and G. Palmisano, “Nano-power CMOS voltage reference for RF-powered systems,” *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 65, no. 10, pp. 1425-1429, July 2018.

# Conclusion

Novel architectures for power and data transfer systems with galvanic isolation have been proposed. They provide efficient solutions to minimize the number of isolated links while performing power and data functionalities. The size of isolated systems is mainly due to the area occupation of the isolation components. Therefore, a reduction of exploited channels is greatly demanding to decrease both complexity and costs of the overall application. In Chapter 1, an overview of the available state-of-the-art solutions for both isolated data and power transfer has been presented. Several efforts have been made to implement power and data functionalities by sharing the same isolation component.

This thesis deals with the analysis and design of three dc-dc converters for low power applications. In Chapter 2 a 100-mW dc-dc converter with

bidirectional half duplex data communication has been presented. Galvanic isolation up to 6 kV is performed by the integrated transformer thanks to the thick oxide layer of the BCD technology back-end. The proposed architecture exploits the isolated power control link to transfer bidirectional half duplex data, thus reducing the overall silicon area and package size. Therefore, only two isolated components have been exploited which are the control/data link and the power link. The latter delivers up to 93 mW output power and output voltage ranging from 2.4 V to 3.3 V thus providing an efficient solution for many applications both in medical and consumer environments. The dc-dc converter presents significant advantages not only over traditional solutions [50], [43], but also over recently published isolated data/power transfer system [28], [40]. Indeed, it is able to provide high regulated power levels, up to 93 mW, and data rates, up to 50 Mb/s, while improving the integration level with respect to the state of the art. Moreover, differently from the architecture in [28], the proposed solution has no theoretical limits in the maximum achievable data rate and do not require performance trade-off between power efficiency and CMTI.

Chapter 3 presents a dc-dc converter which performs both power transfer and control feedback loop by exploiting a single isolated link. Differently from [29], [30], this architecture includes a control loop to regulate output power/voltage. Typically, a dc-dc converter consists at least of two isolated channels as in [40] and [44]. Thanks to a novel architecture, only one isolated link is adopted. Specifically, the error signal for power regulation is converted into a PWM signal which is sampled and transmitted across the galvanic isolation barrier by means of ASK modulation of the power signal. After the isolation barrier, control bits and sampling clock are recovered to recontract

the PWM control signal. The big design challenge was to make compliant on/off control scheme for output power regulation with data transmission on the power signal. Indeed, the on/off control scheme maximizes the efficiency performance but involves the shutdown of the power oscillator thus disabling data communication. To this purpose, a novel technique is proposed which provides the proper PWM control signal to the power oscillator even during the off-phase. The proposed architecture is based on a phase-locked loop which exploits a sample and hold operation on the recovered clock signal used for data transmission. The PLL operation is essential to properly achieve the control feedback loop since it provides an extremely accurate reference clock for the PWM control signal without additional external components. Moreover, the output signal of the PLL guarantees the turning on of the power oscillator after the off-phase, thus avoiding the off steady-state condition. A regulated output power higher than 100 mW with an output voltage of about 20 V and power efficiency around 25 % are achieved, thus addressing this system towards gate driver applications.

Finally, the minimum number of isolated links is definitely achieved by the architecture presented in Chapter 4. The control signal is multiplexed along with N data channels which are transmitted across the isolation barrier by means of ASK modulation of the power signal. Therefore, a single isolated link is exploited thus drastically reducing system complexity and manufacturing costs. Differently from common dc-dc converters which are based on an on/off control scheme, the output power is regulated by adjusting the biasing current of the power oscillator operating in class-B. The converter is able to deliver up to 50 mW with 3.3-V output power and power efficiency

of about 16 %, thus making this system very suitable for sensor applications. Table C.1 summarizes the performance of the proposed systems.

Additional improvements can be done to make the proposed systems more appealing, especially concerning power efficiency performances. The bottleneck for the overall power link efficiency is represented by the isolation components which features poor *Q*-factors. The research interests are growing towards the realization of high-quality micro-transformer that can be implemented by adopting thin-film magnetic layers. This technology improves both efficiency and EMI performance [67] but leads to high implementation costs.

TABLE C.1
SUMMARIZED PERFORMANCE OF THE PROPOSED SYSTEMS

| | **[44]** | **[45]** | **[46]** |
|---|---|---|---|
| **Application** | General purpose | Gate Driver | Sensor interfaces |
| **Supply voltage* [V]** | 3.3 | 5 | 5 |
| **Isolated output voltage [V]** | 2.4 – 3.3 | 18 | 3.3 |
| **Isolated output power [mW]** | 10 – 93 | 130 | 50 |
| **Power efficiency [%]** | 19 | 25 | 16 |
| **Power&data funtionalities**** | PT – PR<br>DT (bidirectional) | PT - PR | PT – PR<br>DT (from B to A) |
| **Control scheme** | PWM | PWM | Continuous-time |
| **Number of isolated links** | 2 | 1 | 1 |
| **Isolation technology** | Integrated SiO2 transformers with standard metals | Post–processed polyimide transformer with thick Au metals | |
| **Silicon technology** | 0.35-µm BCD | 0.18-µm BCD, 0.13-µm CMOS | |

*Power oscillator regulation **PT = power transfer, DT =data transmission, PR = power

# Bibliography


[1] A. Parisi, A. Finocchiaro, and G. Palmisano. “An accurate 1-V threshold voltage reference for ultra-low power applications,” *Microelectronics Journal* 63 (2017): 155-159.

[2] A. Parisi, A. Finocchiaro, G. Papotto and G. Palmisano, “Nano-power CMOS voltage reference for RF-powered systems,” *IEEE Trans. Circuits and Systems II: Express Briefs*, to be published.

[3] David Lohbeck. (2004, Sep.) *Safety isolation protects users and electronic instruments*. [Online]. Available: http://www.edn.com/design/test-and-measurement/4329915/Safety-isolation-protects-users-and-electronic-instruments

[4] John G. Webster, “Medical Instrumentation. Application and Design. IV ed.”, John Wiley & Sons, Inc.

[5] Surging Across the Barrier: Digital Isolators Set the Standard for Reinforced Insulation. Analog Devices. [Online]. Available: http://www.analog.com/media/en/technical-documentation/technical-articles/MS-2341.pdf

[6] Mark Cantrell. Reinforced Isolation in Data Couplers. Analog Devices. [Online]. Available: http://www.analog.com/media/en/technical-documentation/technical-articles/MS-2242.pdf

[7] A. S. Kamath and K. Soundarapandian. High-voltage reinforced isolation: Definitions and test methodologies. Texas Instruments. [Online]. Available: http://www.ti.com/lit/wp/slyy063/slyy063.pdf

[8] Texas Instruments. ISO7841x High-Performance, 8000-VPK reinforced quad-channel digital isolator. [Online]. Available: http://www.ti.com

[9] (2015, Aug.) Isolator High Voltage Safety Standards . NVE Corporation. [Online]. Available: https://www.nve.com/Downloads/ab2.pdf

[10] Scott Wayne. Digital Isolators protect RS-232, RS-485, and CAN Buses. Analog Devices. [Online]. Available: http://www.analog.com/en/analog-dialogue/articles/digitalisolators-protect-rs232-bus.html

[11] Sean Clark. iCoupler® Isolation in RS-485 Applications. Analog Devices. [Online]. Available: http://www.analog.com/media/en/technicaldocumentation/application-notes/AN-727.pdf

[12] Nikolas Ledoux. Breaking Ground Loops with Functional Isolation to Reduce Data Transmission Errors. Analog Devices. [Online]. Available: http://www.analog.com/media/en/technical-documentation/technical-articles/MS-2256.pdf

[13] Maxim Integrated. MAX13223E ±70V Fault-Protected, 3.0V to *5.5V, 2Tx/2Rx RS-232 Transceiver*. [Online]. Available: https: //datasheets.maximintegrated.com/en/ds/MAX13223E.pdf

[14] Texas Instruments. SN65HVD1781A-Q1 Fault-Protected RS-485 *Transceivers With 3.3-V to 5-V Operation*. [Online]. Available: http://www.ti.com/lit/ds/symlink/sn65hvd1781a-q1.pdf

[15] SN65HVD233-HT 3.3-V CAN Transceiver. [Online]. Available: http://www.ti.com/lit/ds/symlink/sn65hvd233-ht.pdf

[16] (2016) Global EV Outlook2016 - Beyond one million electric *cars*. International Energy Agency. [Online]. Available: https://www.iea.org/publications/freepublications/publication/Global_EV_Outlook_2016.pdf

[17] S. Ziegler, R. C. Woodward, H. H. C. Iu, and L. J. Borle, "Current sensing techniques: A review," *IEEE Sensors J.*, vol. 9, no. 4, pp. 354-376, April 2009.

[18] O'Sullivan and N. O'Byrne. *Gate Driver and Current Feedback Signal Isolation in Industrial Motor Drives*. Analog Devices. [Online]. Available: http://www. analog.com/media/en/technical-documentation/technical-articles/Gate-Drive-and-Current-Feedback-Signal-Isolation-in-Industrial-Motor-Drives.pdf

[19] R. Schnell. Powering the Isolated Side of Your Half-Bridge *Configuration*. Analog Devices. [Online]. Available: http://www.analog.com/media/en/technical-documentation/technical-articles/Powering-the-Isolated-Side-of-Your-Half-Bridge-Configuration-MS-2663-1.pdf

[20] STMicroelectronics. *STGAP1AS - Automotive galvanically isolated advanced single gate driver*. [Online]. Available: http://www.st.com/content/ccc/resource/technical/document/datasheet/group3/da/00/41/bb/73/4e/4c/14/DM00295193/files/DM00295193.pdf/jcr:content/translations/en.DM00295193.pdf

[21] Texas Instruments. UCC27212A-Q1 - Automotive 120-V Boot, 4-*A Peak, High-Frequency High-Side and Low-Side Driver*. [Online].Available: http://www.ti.com/lit/ds/symlink/ucc27212a-q1.pdf

[22] STMicroelectronics. STGW35HF60WDI - 35 A, 600 V ultrafast *IGBT with low drop diode*. [Online]. Available: http://www.st.com/content/ccc/resource/technical/document/datasheet/12/37/07/8e/6a/dc/40/bc/CD00243925.pdf/files/CD00243925.pdf/jcr:content/translations/en.CD00243925.pdf

[23] N. Spina, G. Girlando, S. Smerzi, and G. Palmisano, "Integrated galvanic isolator using wireless transmission," Jan. 2013, u.S. Patent 8 364 195.

[24] A. Krone, T. Tuttle, J. Scott, J. Hein, T. Dupuis, and N. Sooch, "A CMOS direct access arrangement using digital capacitive isolation," in 2001 IEEE Int. Solid-State Circuits Conf. Dig. of Techn. Papers *(ISSCC)*, Feb. 2001, pp. 300–301.

[25] R. Kliger, "Integrated transformer-coupled isolation," *IEEE Instrum. Meas. Mag.*, vol. 6, no. 1, pp. 16–19, March 2003.

[26] S. Kaeriyama, S. Uchida, M. Furumiya, M. Okada, T. Maeda, and M. Mizuno, "A 2.5 kv isolation 35 kv/us cmr 250 mbps digital isolator in standard cmos with a small transformer driving technique," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 435–443, Feb 2012.

[27] O. Deleage, J. C. Crebier, M. Brunet, Y. Lembeye, and H. T. Manh, "Design and realization of highly integrated isolated dc/dc microconverter," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 930–938, March 2011.

[28] P. Lombardo, V. Fiore, E. Ragonese, and G. Palmisano, "A fullyintegrated half-duplex data/power transfer system with up to 40Mbps data rate, 23mW output power and onchip 5kV galvanic isolation," in *IEEE* Int. Solid-State Circuits Conf. Tech. Dig. (ISSCC), Feb. 2016, pp. 300–301.

[29] N. Spina, V. Fiore, P. Lombardo, E. Ragonese, and G. Palmisano, "Current-Reuse Transformer-Coupled Oscillators With Output Power Combining for Galvanically Isolated Power Transfer Systems," *IEEE Trans. Circuits and Syst. I: Reg. Papers*, vol. 62, no. 12, pp. 2940–2948, Dec. 2015.

[30] V. Fiore, E. Ragonese, and G. Palmisano, "A Fully Integrated Watt-Level Power Transfer System With On-Chip Galvanic Isolation in Silicon Technology," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1984–1995, Mar. 2017.

[31] V. Ching. Use Dynamic Common-Mode Rejection Test To Evaluate Industrial Isolator Performance.

[32] Silicon Labs. CMOS Digital Isolators Supersede Optocouplers in Industrial Applications .

[33] Y. Moghe, A. Terry, and D. Luzon, "Monolithic 2.5kv rms, 1.8v-3.3v dual-channel 640mbps digital isolator in 0.5$\mu$m sos," in *2012 IEEE Int. SOI Conference (SOI)*, Oct 2012, pp. 1–2.

[34] S. Marwat. *Digital isolators compliance to IEC 61010-1 edition 3.0 safety requirements*. Texas Instruments. [Online]. Available: http://www.ti.com/lit/wp/slyy055/slyy055.pdf

[35] L. Chen, J. Sankman, R. Mukhopadhyay, M. Morgan, and D. B. Ma, "A 50.7% peak efficiency subharmonic resonant isolated capacitive power transfer system with 62mWoutput power for low-power industrial sensor interfaces," in *2017 IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb 2017, pp. 428–429.

[36] *iCoupler thecnology*. Analog Devices. [Online]. Available: http://www.analog.com/iCoupler

[37] B. Chen, "Fully integrated isolated dc-dc converter using microtransformers," in *Twenty-Third Annual IEEE Applied Power Electronics Conf. and Expo. (APEC)*, Feb. 2008, pp. 335–338.

[38] *isoPower thecnology*. Analog Devices. [Online]. Available: http://www.analog.com/isoPower

[39] Z. Tan, M. Mueck, X. H. Du, L. Getzin, M. Guidry, F. Zhao, and B. Chen, "A fully isolated delta-sigma ADC for shunt based current sensing," in *IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2015, pp. 1–4.

[40] Z. Tan, M. Mueck, X. H. Du, L. Getzin, M. Guidry, S. Keating, X. Xing, F. Zhao, and B. Chen, "A Fully Isolated Delta-Sigma ADC for Shunt Based Current Sensing," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2232–2240, Oct. 2016.

[41] V. Palumbo, G. Ghidini, E. Carollo, and F. Toia, "Integrated transformer," Jun. 2015, U.S. Patent App. 14/733,009, filed.

[42] F. Pulvirenti, G. Cantone, G. Lombardo, and M. Minieri, “Dispositivi con isolamento galvanico integrato (in Italian),” in *Convegno Annuale 2014 dalla ricerca all’impresa: necessità di un trasferimento più efficace (AEIT)*, Sep. 2014, ISBN 9788887237252.

[43] Analog Devices, ADuM6201 - Dual-channel, 5 kV isolators with integrated DC-to-DC converter datasheet, [Online]. Available: http://www.analog.com.

[44] E. Ragonese, N. Spina, A. Castorina, P. Lombardo, N. Greco, A. Parisi and G. Palmisano, “A fully integrated galvanically isolated DC-DC converter with data communication,” *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 65, no. 4, pp. 1432-1441, April 2018.

[45] A. Parisi, N. Greco, N. Spina, E. Ragonese, G. Palmisano, “A galvanic isolation circuit and system, corresponding method”, IT Patent Appl. 1020180000417, filed 3 April 2018.

[46] A. Parisi, N. Greco, N. Spina, E. Ragonese, G. Palmisano, “A galvanically isolated dc-dc circuit converter, with data communication, corresponding system and corresponding method,” IT Patent Appl. 102018000000830, filed 12 Jan. 2018.

[47] E. Ragonese, N. Spina, P. Lombardo, N. Greco, A. Parisi, G. Palmisano, “Galvanically isolated DC-DC converter with bidirectional data transmission,” U.S. Patent App. 15178822, filed 10 June 2016.

[48] B. Chen, *iCoupler® products with isoPower™ technology: signal and power transfer across isolation barrier using microtransformers, Technical Article, Analog Devices, USA,* [Online]. Avalaible: http://www.analog.com/media/cn/technical-documentation/technical-articles/isoPower.pdf?doc=CN0185.pdf.

[49] B. Chen, “Microtransformer isolation benefits digital control,” *Power Electronics Technology*, pp. 20-25, Oct. 2008.

[50] B. Chen, “Fully integrated isolated dc-dc converter using micro-transformers,” in *Proc. IEEE Applied Power Electronics Conf. and Expo., (APEC)*, pp. 335-338, Feb. 2008.

[51] B. Chen, “Isolated half-bridge gate driver with integrated high-side supply,” *Proc. IEEE Power Electronics Specialists Conf. (PESC)* pp. 3615-3618, Jun. 2008.

[52] B. Chen, “High frequency power converter based on transformers,” U.S. patent 7,983,059 B2, Jul. 19, 2011.

[53] B. Chen, *iCoupler® products with isoPower™ technology: signal and power transfer across isolation barrier using microtransformers, Technical Article, Analog Devices, USA*, [Online]. Avalaible: http://www.analog.com/media/cn/technical-documentation/technical-articles/isoPower.pdf?doc=CN0185.pdf.

[54] L. Fanori, P. Andreani, “Class-D CMOS Oscillators,” *IEEE J. Solid-State Circuits*, vol. 48, pp. 3105-3119, Dec. 2013.

[55] S. S. Hashemi, M. Sawan, and Y. Savaria, “A high-efficiency low-voltage CMOS rectifier for harvesting energy in implantable devices,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, pp. 326-335, Aug. 2012.

[56] F. Carrara, A. Italia, E. Ragonese, and G. Palmisano, “Design methodology for the optimization of transformer loaded RF circuits,” *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 53, pp. 761-768, April 2006.

[57] N. Spina, G. Girlando, S. Smerzi, G. Palmisano, “Integrated galvanic isolator using wireless transmission,” U.S. Patent 8364195 B2, Jan. 2013.

[58] G. Lombardo, S. Giombanco, M. Grande, S. Tumminaro, F. Marino, “Receiver for signal communication apparatus and related signal communication apparatus,” U.S. 8576930 B2, Nov. 2013.

[59] B. Nhamidipati, *et al.*, “Galvanic isolator,” U.S. App. 14/050,984, filed 10 Oct. 2013.

[60] S. Sankaran *et al.*, “An efficient and resilient ultra-high speed galvanic data isolator leveraging broad-band multi resonant tank electro-magnetic coupling,” in *Proc. IEEE Symp. on VLSI Circuits*, June 2015, pp. 210-211,.

[61] E. Ragonese, N. Spina, P. Lombardo, N. Greco, A. Parisi, G. Palmisano, “A galvanic isolation circuit, corresponding system and method,” IT Patent App. 10201600008820, filed 30 Aug. 2016.

[62] V. Fiore, *et. al.*, “A 13.56MHz RFID tag with active envelope detection in an organic complementary TFT technology,” in *Proc. IEEE Int. Solid-State Circuits Conf. Tech. Dig.,* Feb. 2014, pp. 492-493.

[63] V. Fiore, “Fully integrated systems with on-chip galvanic isolation in silicon technology,” Ph.D. dissertation, DIEEI, University of Catania, Catania, Italy, 2015.

[64] V. Fiore, E. Ragonese and G. Palmisano, “Low-power ASK detector for low modulation indexes and rail-to-rail input range,” in *IEEE Trans. Circuits and Syst. II, Exp. Briefs*, vol. 63, pp. 458-462, May 2016.

[65] N. Greco, A. Parisi, G. Palmisano, N. Spina and E. Ragonese, “Integrated transformer modelling for galvanically isolated power

transfer systems," Elsevier, Integration, the VLSI Journal, Special Issue on PRIME and SMACD 2017, published on-line.

[66] *Multiplexing, framing and some solutions* (SPRING 2007), [Online]. Available: http://inst.eecs.berkeley.edu/~ee122/sp07/Mux_Fram.pdf

[67] Z. Tianting, Z. Yue, and C. Baoxing, "An isolated dc-dc converter with fully integrated magnetic core transformer," in *2017 IEEE Custom Integrated Circuits Conf. (CICC)*, April 2017, pp. 1–4.